



Tutorial para realizar simulaciones en lenguaje VHDL utilizando ISE Project Navigator

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Ejemplo 1:

Simulación de combinacionales

- a) Crear un proyecto en lenguaje VHDL, compilarlo y reparar los errores de sintaxis que se tenga.
- b) Mostrar la simulación de la compuerta or.



Compilación.



ISE Project Navigator (P.20131013) - C:\Users\NORMA\Desktop\Cor\cor\cor.xise - [cor.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementación Simulación

Hierarchy

- cor
 - xc3s100e-5cp132
 - cor - Behavioral (cor.vhd)

No Processes Running

Processes: cor - Behavioral

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Sc...
 - Check Syntax**
 - Generate Post-Synt...
- Implement Design
- Generate Programming...
- Configure Target Device

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6
7
8 entity cor is
9     Port ( A : in  STD_LOGIC;
10          B : in  STD_LOGIC;
11          SOR : out STD_LOGIC);
12 end cor;
13
14 architecture Behavioral of cor is
15
16 begin
17     SOR <= A OR B;
18
19 end Behavioral;
20
21
```

Design Summary

Errors

Errors Warnings Find in Files Results

Ln 21 Col 1

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12:24 p. m. 20/05/2020

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Crear un archivo de simulación y cambiar a modo simulación seleccionando VHDL test.

Poniendole nombre distinto al que tenemos en la entidad.



ISE Project Navigator (P.20131013) - C:\Users\NORMA\Desktop\Cor\cor\cor.xise - [cor.vhd]

File Edit View Project Source Process Tools Window Layout Help



Design

View: Implementation Simulation

Behavioral

Hierarchy

- cor
- xc3s100e-5cp132
- cor - Behavioral (cor.vhd)

No Processes Running

No single design module is selected.

Design Utilities

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6
7
8 entity cor is
9     Port ( A : in
10           B : in
11           SOR : o
12 end cor;
13
14 architecture Behav
15
16 begin
17 SOR <= A OR B;
18
19 end Behavioral;
20
21
```

New Source Wizard

Select Source Type

Select source type, file name and its location.

- BMM File
- ChipScope Definition and Connection File
- Implementation Constraints File
- IP (CORE Generator & Architecture Wizard)
- MEM File
- Schematic
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench**
- Embedded Processor

File name: COR_TB

Location: C:\Users\NORMA\Desktop\Cor\cor

Add to project

More Info Next > Cancel

Design Files Libraries cor.vhd

Errors

Errors Warnings Find in Files Results



- 1.- Abrir el simulador, verificar sintaxis.
- 2.- Dar valores a las entradas en ciertos periodos de tiempo



ISE Project Navigator (P.20131013) - C:\Users\NORMA\Desktop\Cor\cor\cor.xise - [COR_TB.vhd]

File Edit View Project Source Process Tools Window Layout Help



Design

View: Implementation Simulation

Behavioral

Hierarchy

- cor
 - xc3s100e-5cp132
 - SANAND_TB - behavior (COR_TB.vhd)
 - cor - Behavioral (cor.vhd)

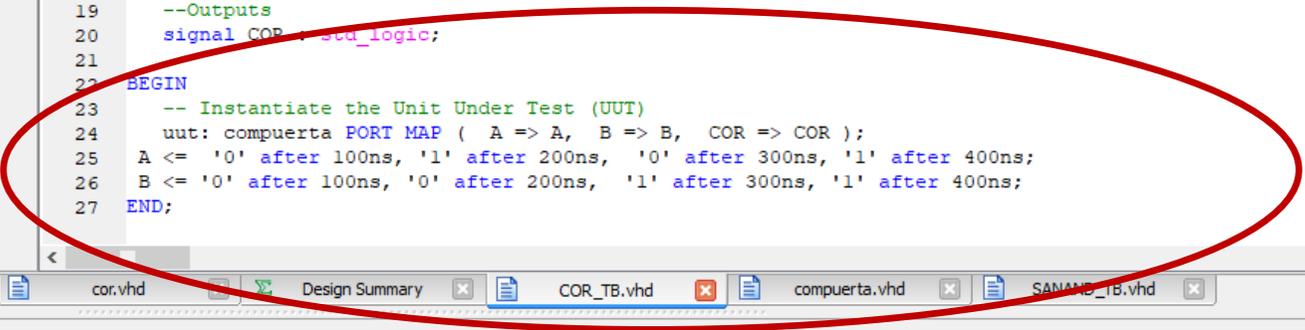
No Processes Running

Processes: SANAND_TB - behavior

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

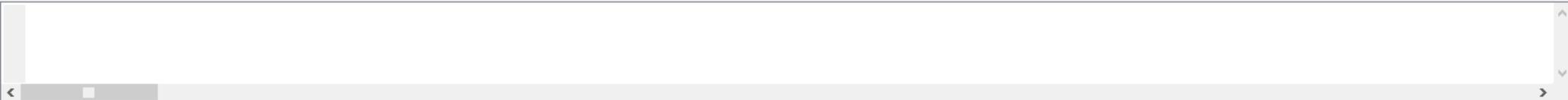
Design Files Libraries

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4
5 ENTITY SANAND_TB IS
6 END SANAND_TB;
7
8 ARCHITECTURE behavior OF SANAND_TB IS
9     COMPONENT compuerta
10    PORT( A : IN std_logic;
11          B : IN std_logic;
12          COR : OUT std_logic );
13    END COMPONENT;
14
15    --Inputs
16    signal A : std_logic := '0';
17    signal B : std_logic := '0';
18
19    --Outputs
20    signal COR : std_logic;
21
22 BEGIN
23    -- Instantiate the Unit Under Test (UUT)
24    uut: compuerta PORT MAP ( A => A, B => B, COR => COR );
25    A <= '0' after 100ns, '1' after 200ns, '0' after 300ns, '1' after 400ns;
26    B <= '0' after 100ns, '0' after 200ns, '1' after 300ns, '1' after 400ns;
27 END;
```



cor.vhd Design Summary COR_TB.vhd compuerta.vhd SANAND_TB.vhd

Errors



Errors Warnings Find in Files Results

Escribe aquí para buscar

Ln 8 Col 1 | VHDL

12:41 p. m. 20/05/2020

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Hacer click en el botón de simular



ISE Project Navigator (P.20131013) - C:\Users\NORMA\Desktop\Cor\cor\cor.xise - [COR_TB.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Behavioral

Hierarchy

- cor
 - xc3s100e-5cp132
 - SANAND_TB - behavior (COR_TB.vhd)
 - cor - Behavioral (cor.vhd)

No Processes Running

Processes: SANAND_TB - behavior

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model**

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
3
4
5 ENTITY SANAND_TB IS
6 END SANAND_TB;
7
8 ARCHITECTURE behavior OF SANAND_TB IS
9     COMPONENT compuerta
10        PORT( A : IN std_logic;
11             B : IN std_logic;
12             COR : OUT std_logic );
13     END COMPONENT;
14
15     --Inputs
16     signal A : std_logic := '0';
17     signal B : std_logic := '0';
18
19     --Outputs
20     signal COR : std_logic;
21
22 BEGIN
23     -- Instantiate the Unit Under Test (UUT)
24     uut: compuerta PORT MAP ( A => A, B => B, COR => COR );
25     A <= '0' after 100ns, '1' after 200ns, '0' after 300ns, '1' after 400ns;
26     B <= '0' after 100ns, '0' after 200ns, '1' after 300ns, '1' after 400ns;
27 END;
```

Design Files Libraries

cor.vhd Design Summary COR_TB.vhd compuerta.vhd SANAND_TB.vhd

Errors

Errors Warnings Find in Files Results

Ln 8 Col 1 VHD

Escribe aquí para buscar

12:45 p. m. 20/05/2020



Se genera una nueva ventana que se requiere abrir para analizar

The screenshot displays the Microsoft PowerPoint 2013 interface in Spanish. The title bar reads "Tutoria_simulacion.ppt [Modo de compatibilidad] - PowerPoint (Error de activación de productos)". The ribbon includes tabs for ARCHIVO, INICIO, INSERTAR, DISEÑO, TRANSICIONES, ANIMACIONES, PRESENTACIÓN CON DIAPOSITIVAS, REVISAR, VISTA, and Foxit PDF. The slide area shows two logos: the Universidad Nacional Autónoma de México logo on the left and the Ingeniería logo on the right. The taskbar at the bottom shows the Windows Start button, a search bar, and several application icons. A red arrow points to the ISim application window icon in the taskbar. The ISim window is titled "ISim (P.20131013) - [Default.wcfg]" and displays a simulation interface with a grid and various data points.



Hacer click en el botón de vista completa



The screenshot shows the ISim software interface. The main window displays a simulation waveform for three signals: 'a', 'b', and 'cor'. The time axis is labeled '1,000,000 ps'. A tooltip 'Zoom to Full View' is visible over the waveform. The toolbar at the top contains various icons, with the 'Zoom to Full View' icon (a magnifying glass with a square) circled in red. The interface also includes a console window at the bottom with the following text:

```
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

The Windows taskbar at the bottom shows the system tray with the time 12:46 p. m. and date 20/05/2020.



Analizar el comportamiento de la compuerta OR en el simulador



sim (Default.wcfg)

File Edit View Simulation Window Layout Help



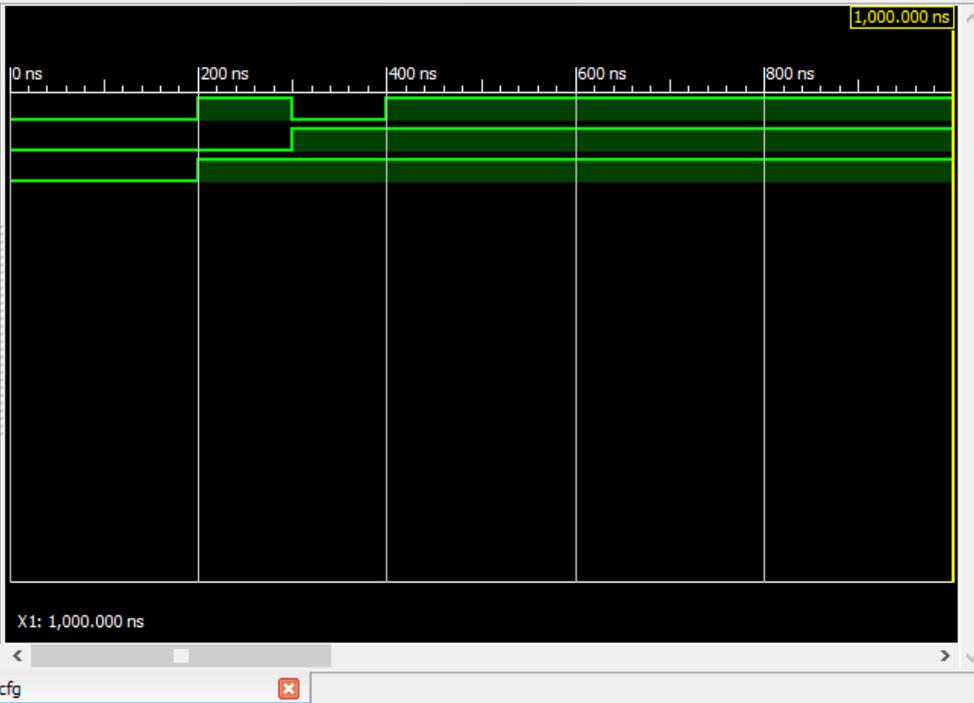
Instances and Processes

| Instance and Process Name | D |
|---------------------------|----|
| sanand_tb | st |
| std_logic_1164 | st |
| std_logic_arith | st |
| std_logic_unsigned | st |

Objects

| Object Name | Value |
|-------------|-------|
| a | 1 |
| b | 1 |
| cor | 1 |

| Name | Value |
|------|-------|
| a | 1 |
| b | 1 |
| cor | 1 |



Console

```
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
```

Console Compilation Log Breakpoints Find in Files Results Search Results

Sim Time: 1,000,000 ps



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Ejemplo2: Simulación de secuenciales.

- a) Crear un proyecto en lenguaje VHDL, compilarlo y reparar los errores de sintaxis que se tenga.
- b) Mostrar la simulación de un sistema secuencial.



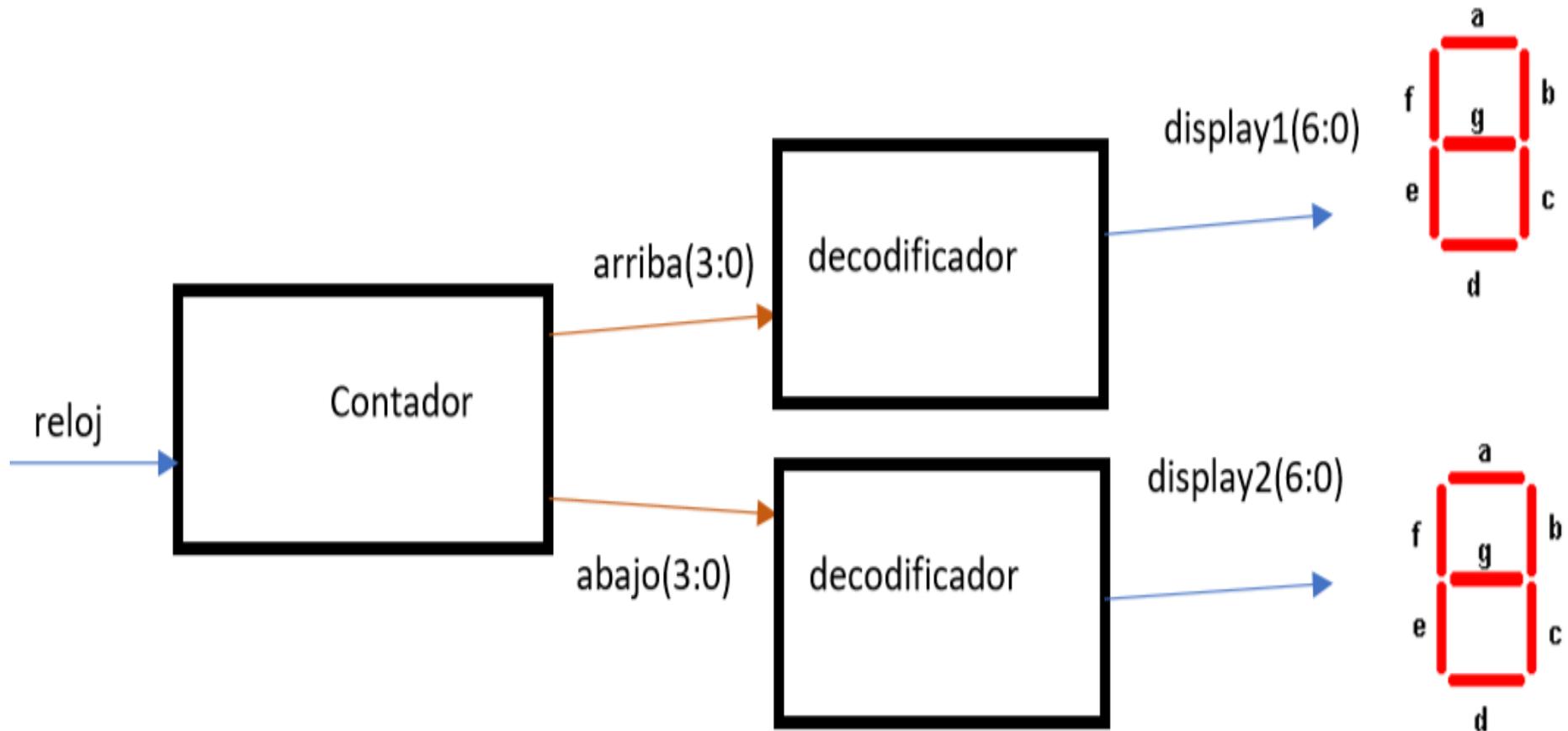
Especificaciones.



Simular la función de dos contadores, el primero deberá contar de 3 en 3, inicia en 0 y llega al 9, posteriormente resta de 3 en 3 hasta el 3 y vuelve a subir al 9, regresando al punto inicial en 0 y el segundo contador va del 0 al 8 y del 0 al 4. Este último iniciará en 4, seguirá en 4 un ciclo más, luego baja a 2, sube a 6, inicia en 0 y ahora desde 8 baja hasta el



Diagrama de bloques.





Código en lenguaje VHDL.



```
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
use IEEE.STD_LOGIC_ARITH.ALL;  
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

Bibliotecas



Código en lenguaje VHDL.



```
entity contadores is
```

```
    Port ( CLK : in STD_LOGIC;
```

```
          display1,display2: out std_logic_vector(6 downto 0));
```

```
End contadores;
```

Entidad



Código en lenguaje VHDL.



```
architecture Behavioral of contadores is
signal arriba : std_logic_vector(3 downto 0):= "0000";
signal abajo : std_logic_vector(3 downto 0):= "1001";
begin
cuentaArriba: process(CLK)
begin
    if (rising_edge(CLK)) then
        if arriba = "1000" then
            arriba <= "0000";
        else
            arriba <= arriba+1;
        end if; end if;
    end process;
```

Arquitectura



Código en lenguaje VHDL.



```
cuentaAbajo: process(CLK)
begin
    if (rising_edge(CLK)) then
        if abajo = "0000" then
            abajo <= "1001";
        else
            abajo <= abajo-1;
        end if; end if;
    end process;
```

Arquitectura



Código en lenguaje VHDL.



```
with arriba select
```

```
display1 <= "1000000" when "0000", --Para el valor de 0  
            "0110000" when "0001", --Para el valor de 3  
            "0000010" when "0010", --Para el valor de 6  
            "0010000" when "0011", --Para el valor de 9  
            "0000010" when "0100", --Para el valor de 6  
            "0110000" when "0101", --Para el valor de 3  
            "0000010" when "0110", --Para el valor de 6  
            "0010000" when "0111", --Para el valor de 9  
            "1000000" when others;
```

Arquitectura



Código en lenguaje VHDL.



```
with abajo select
```

```
    display2 <= "1000000" when "0000", --Para el valor de 0  
               "0100100" when "0001", --Para el valor de 2  
               "0011001" when "0010", --Para el valor de 4  
               "0000010" when "0011", --Para el valor de 6  
               "0000000" when "0100", --Para el valor de 8  
               "1000000" when "0101", --Para el valor de 0  
               "0000010" when "0110", --Para el valor de 2  
               "0100100" when "0111", --Para el valor de 4  
               "0011001" when others;
```

```
end behavioral;
```

Arquitectura



Código simulación.



```
LIBRARY ieee;  
USE ieee.stc_logic_1164.ALL;  
  
-- Uncomment the following library declaration if using  
-- arithmetic functions with Signed or Unsigned values  
--USE ieee.numeric_std.ALL;  
  
ENTITY Contest IS  
END Contes;
```



Código simulación.



```
ARCHITECTURE behavior OF Contest IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT Contadores

PORT(

    CLK : IN std_logic;

    display1 : OUT std_logic_vector(6 downto 0);

    display2 : OUT std_logic_vector(6 downto 0)

);

END COMPONENT;
```



Código simulación.



--Inputs

```
signal CLK: std_logic := '0';
```

--Outputs

```
signal display1 : std_logic_vector(6 downto 0);
```

```
signal display2 : std_logic_vector(6 downto 0);
```

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name



Código simulación.



```
BEGIN

    -- Instantiate the Unit Under Test (UUT)
    uut: Contadores PORT MAP (
        CLK => CLK,
        display1 => display1,
        display2 => display2
    );

END;
```



Diagrama de tiempos simulación.

Al iniciar la simulación nos muestra el primer término, debemos forzar al reloj "CLK"

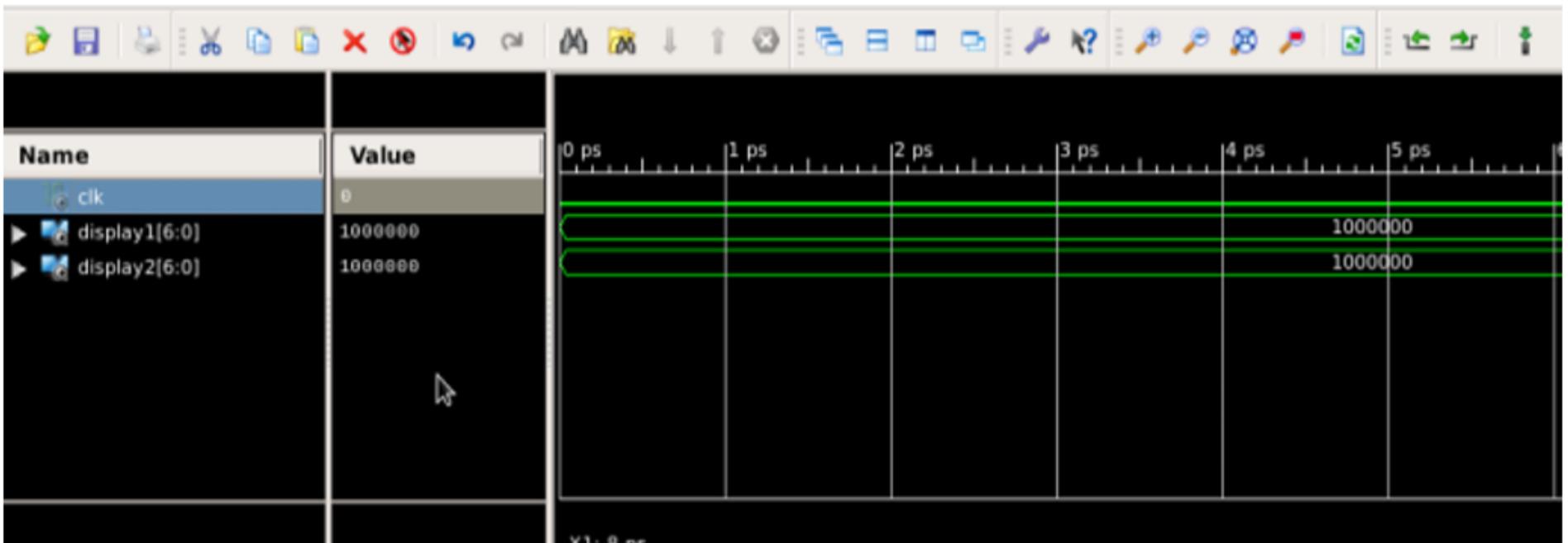




Diagrama de tiempos simulación.

1 000 000 ns

Define Clock

Enter parameters below to force the signal to an alternating pattern (clock). Assignments made from within HDL code or any previously applied constant or clock force will be overridden

Signal Name:

Value Radix

Leading Edge Value:

Trailing Edge Value:

Starting at Time Offset:

Cancel after Time Offset:

Duty Cycle (%):

Period



Diagrama de tiempos simulación.

Hacemos que el reloj vaya de '0' a '1' para activar los contadores, y el periodo que tendrá será igual al inicial (1000ns)

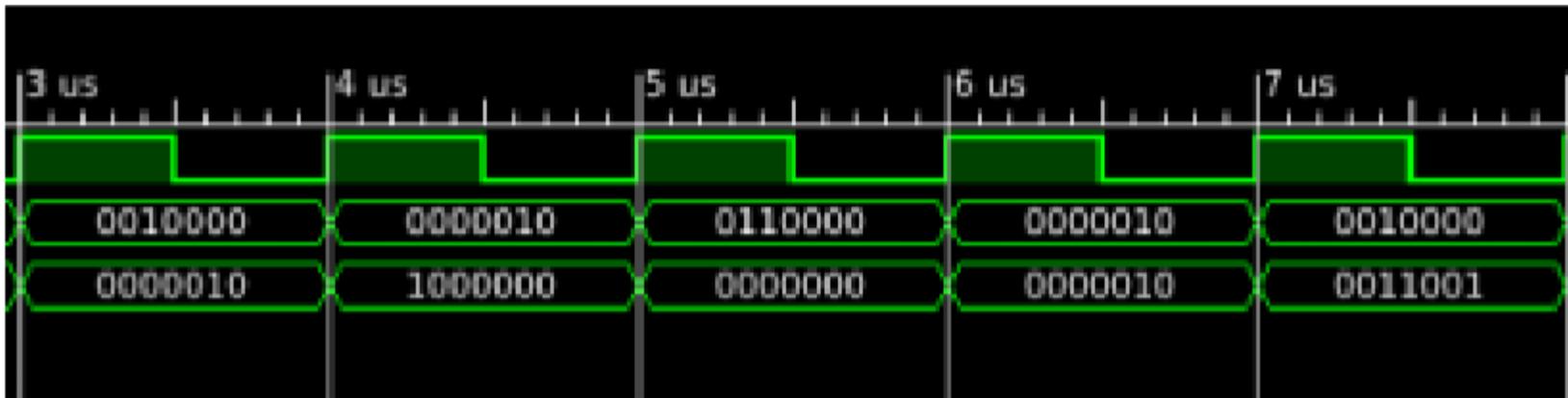
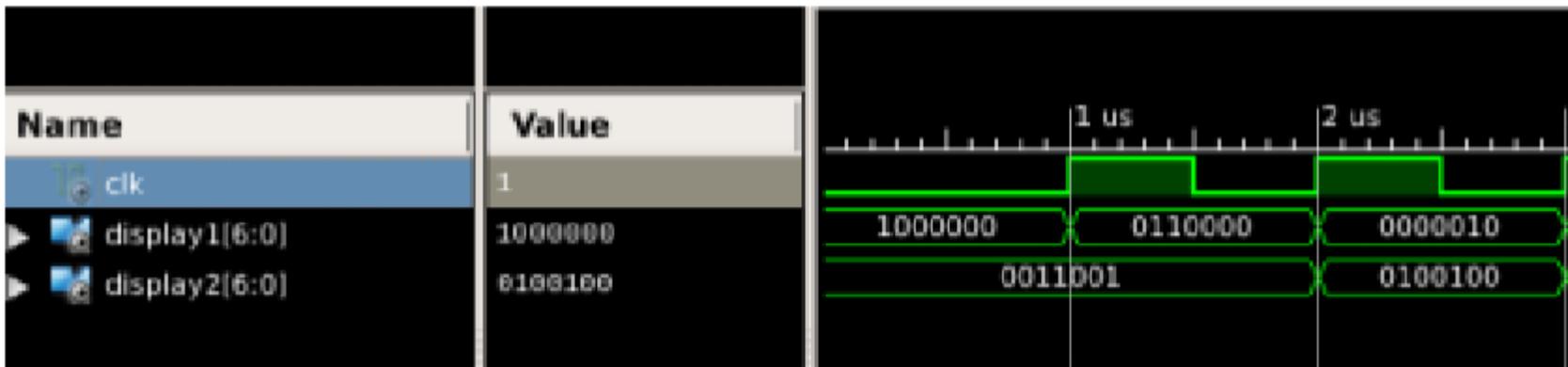




Diagrama de tiempos simulación.

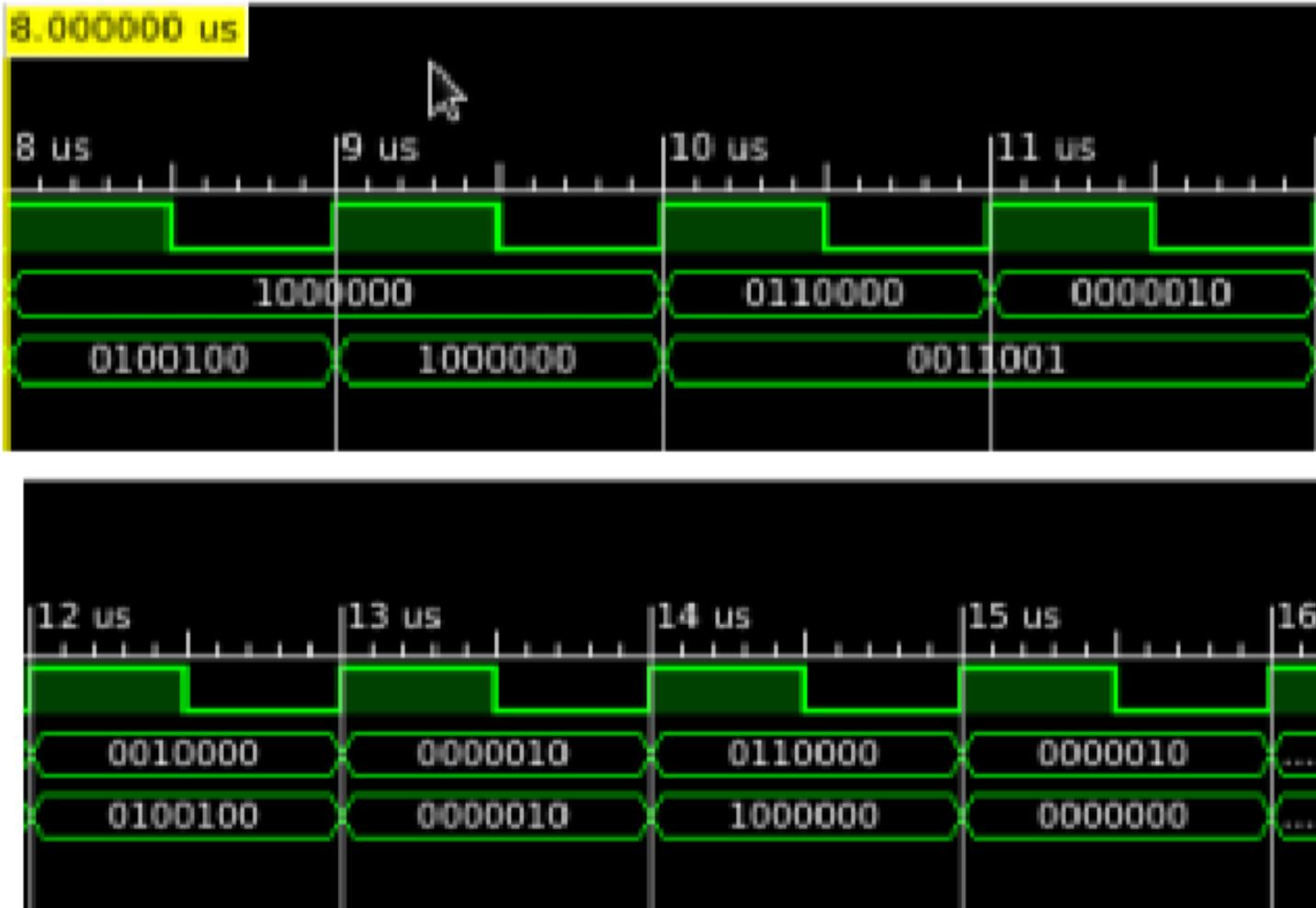




Diagrama de tiempos simulación.

