

Tarjeta lite

Table 3-2 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
ADC_CLK_10	PIN_N5	10 MHz clock input for ADC (Bank 3B)	3.3-V LVTTTL
MAX10_CLK1_50	PIN_P11	50 MHz clock input(Bank 3B)	3.3-V LVTTTL
MAX10_CLK2_50	PIN_N14	50 MHz clock input(Bank 3B)	3.3-V LVTTTL

Table 3-3 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY0	PIN_B8	Push-button[0]	3.3 V SCHMITT TRIGGER"
KEY1	PIN_A7	Push-button[1]	3.3 V SCHMITT TRIGGER"

Table 3-4 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW0	PIN_C10	Slide Switch[0]	3.3-V LVTTTL
SW1	PIN_C11	Slide Switch[1]	3.3-V LVTTTL
SW2	PIN_D12	Slide Switch[2]	3.3-V LVTTTL
SW3	PIN_C12	Slide Switch[3]	3.3-V LVTTTL
SW4	PIN_A12	Slide Switch[4]	3.3-V LVTTTL
SW5	PIN_B12	Slide Switch[5]	3.3-V LVTTTL
SW6	PIN_A13	Slide Switch[6]	3.3-V LVTTTL
SW7	PIN_A14	Slide Switch[7]	3.3-V LVTTTL
SW8	PIN_B14	Slide Switch[8]	3.3-V LVTTTL
SW9	PIN_F15	Slide Switch[9]	3.3-V LVTTTL

Table 3-5 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR0	PIN_A8	LED [0]	3.3-V LVTTTL
LEDR1	PIN_A9	LED [1]	3.3-V LVTTTL
LEDR2	PIN_A10	LED [2]	3.3-V LVTTTL
LEDR3	PIN_B10	LED [3]	3.3-V LVTTTL
LEDR4	PIN_D13	LED [4]	3.3-V LVTTTL
LEDR5	PIN_C13	LED [5]	3.3-V LVTTTL
LEDR6	PIN_E14	LED [6]	3.3-V LVTTTL
LEDR7	PIN_D14	LED [7]	3.3-V LVTTTL
LEDR8	PIN_A11	LED [8]	3.3-V LVTTTL
LEDR9	PIN_B11	LED [9]	3.3-V LVTTTL

Table 3-6 Pin Assignment of 7-segment Displays

Signal Name	FPGA Pin No.	Description	I/O Standard
HEX00	PIN_C14	Seven Segment Digit 0[0]	3.3-V LVTTTL
HEX01	PIN_E15	Seven Segment Digit 0[1]	3.3-V LVTTTL
HEX02	PIN_C15	Seven Segment Digit 0[2]	3.3-V LVTTTL
HEX03	PIN_C16	Seven Segment Digit 0[3]	3.3-V LVTTTL
HEX04	PIN_E16	Seven Segment Digit 0[4]	3.3-V LVTTTL
HEX05	PIN_D17	Seven Segment Digit 0[5]	3.3-V LVTTTL
HEX06	PIN_C17	Seven Segment Digit 0[6]	3.3-V LVTTTL
HEX07	PIN_D15	Seven Segment Digit 0[7], DP	3.3-V LVTTTL
HEX10	PIN_C18	Seven Segment Digit 1[0]	3.3-V LVTTTL
HEX11	PIN_D18	Seven Segment Digit 1[1]	3.3-V LVTTTL
HEX12	PIN_E18	Seven Segment Digit 1[2]	3.3-V LVTTTL
HEX13	PIN_B16	Seven Segment Digit 1[3]	3.3-V LVTTTL

HEX14	PIN_A17	Seven Segment Digit 1[4]	3.3-V LVTTTL
HEX15	PIN_A18	Seven Segment Digit 1[5]	3.3-V LVTTTL
HEX16	PIN_B17	Seven Segment Digit 1[6]	3.3-V LVTTTL
HEX17	PIN_A16	Seven Segment Digit 1[7] , DP	3.3-V LVTTTL
HEX20	PIN_B20	Seven Segment Digit 2[0]	3.3-V LVTTTL
HEX21	PIN_A20	Seven Segment Digit 2[1]	3.3-V LVTTTL
HEX22	PIN_B19	Seven Segment Digit 2[2]	3.3-V LVTTTL
HEX23	PIN_A21	Seven Segment Digit 2[3]	3.3-V LVTTTL
HEX24	PIN_B21	Seven Segment Digit 2[4]	3.3-V LVTTTL
HEX25	PIN_C22	Seven Segment Digit 2[5]	3.3-V LVTTTL
HEX26	PIN_B22	Seven Segment Digit 2[6]	3.3-V LVTTTL
HEX27	PIN_A19	Seven Segment Digit 2[7] , DP	3.3-V LVTTTL

HEX30	PIN_F21	Seven Segment Digit 3[0]	3.3-V LVTTTL
HEX31	PIN_E22	Seven Segment Digit 3[1]	3.3-V LVTTTL
HEX32	PIN_E21	Seven Segment Digit 3[2]	3.3-V LVTTTL
HEX33	PIN_C19	Seven Segment Digit 3[3]	3.3-V LVTTTL
HEX34	PIN_C20	Seven Segment Digit 3[4]	3.3-V LVTTTL
HEX35	PIN_D19	Seven Segment Digit 3[5]	3.3-V LVTTTL
HEX36	PIN_E17	Seven Segment Digit 3[6]	3.3-V LVTTTL
HEX37	PIN_D22	Seven Segment Digit 3[7] , DP	3.3-V LVTTTL
HEX40	PIN_F18	Seven Segment Digit 4[0]	3.3-V LVTTTL
HEX41	PIN_E20	Seven Segment Digit 4[1]	3.3-V LVTTTL
HEX42	PIN_E19	Seven Segment Digit 4[2]	3.3-V LVTTTL
HEX43	PIN_J18	Seven Segment Digit 4[3]	3.3-V LVTTTL
HEX44	PIN_H19	Seven Segment Digit 4[4]	3.3-V LVTTTL
HEX45	PIN_F19	Seven Segment Digit 4[5]	3.3-V LVTTTL
HEX46	PIN_F20	Seven Segment Digit 4[6]	3.3-V LVTTTL
HEX47	PIN_F17	Seven Segment Digit 4[7] , DP	3.3-V LVTTTL
HEX50	PIN_J20	Seven Segment Digit 5[0]	3.3-V LVTTTL
HEX51	PIN_K20	Seven Segment Digit 5[1]	3.3-V LVTTTL
HEX52	PIN_L18	Seven Segment Digit 5[2]	3.3-V LVTTTL
HEX53	PIN_N18	Seven Segment Digit 5[3]	3.3-V LVTTTL
HEX54	PIN_M20	Seven Segment Digit 5[4]	3.3-V LVTTTL
HEX55	PIN_N19	Seven Segment Digit 5[5]	3.3-V LVTTTL
HEX56	PIN_N20	Seven Segment Digit 5[6]	3.3-V LVTTTL
HEX57	PIN_L19	Seven Segment Digit 5[7] , DP	3.3-V LVTTTL