

FAST and LS TTL Data

Logic Integrated Circuits Division



1

**Selection Information
FAST/LS TTL**

2

Circuit Characteristics

3

**Design Considerations,
Testing and Applications
Assistance Form**

4

FAST Data Sheets

5

LS Data Sheets

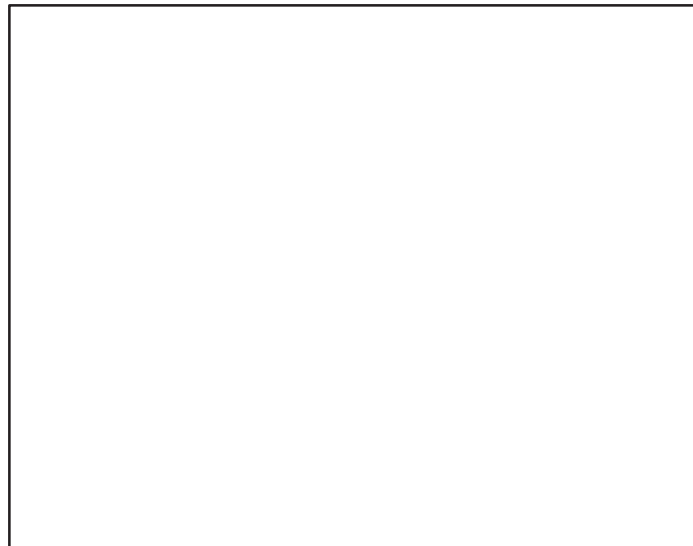
6

Reliability Data

7

**Package Information
Including
Surface Mount**

FAST AND LS TTL



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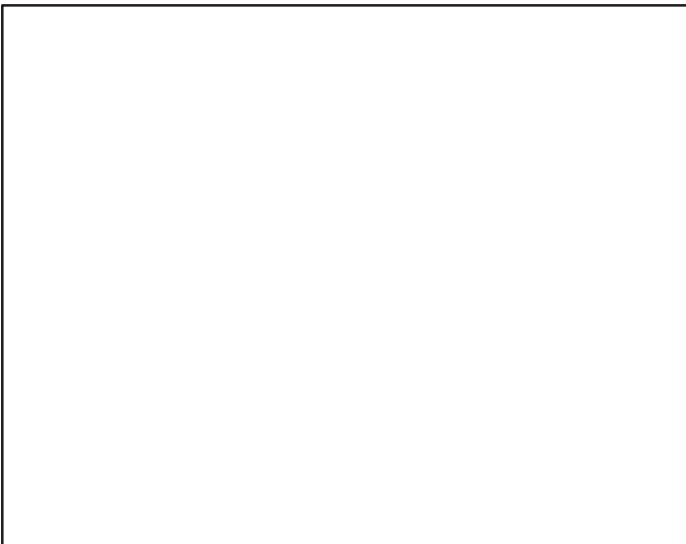
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7



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FAST AND LS TTL

Low Power Schottky (LSTTL) has become the industry standard logic in recent years, replacing the original 7400 TTL with lower power and higher speeds. In addition to offering the standard LS TTL circuits, Motorola offers the FAST Schottky and TTL family. Complete specifications for each of these families are provided in data sheet form. Functional selector guides not only provide an overview of already introduced devices but planned introduction dates of new products.

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CONTENTS

	Page
INDEX OF DEVICES	ii
CHAPTER 1 — SELECTION INFORMATION, FAST/LS TTL	1-1
CHAPTER 2 — CIRCUIT CHARACTERISTICS	2-1
Family Characteristics	2-2
FAST TTL	2-2
LS TTL	2-2
Circuit Features	2-2
Input Configuration	2-3
Input Characteristics	2-3
Output Configuration	2-4
Output Characteristics	2-4
AC Switching Characteristics	2-5
LS/FAST ESD Characteristics	2-6
CHAPTER 3 — DESIGN CONSIDERATIONS, TESTING AND APPLICATIONS ASSISTANCE FORM	3-1
DESIGN CONSIDERATIONS	3-2
Selecting TTL Logic	3-2
Noise Immunity	3-2
Power Consumption	3-2
Fan-In and Fan-Out	3-3
Wired-OR Applications	3-4
Unused Inputs	3-4
Input Capacitance	3-4
Line Driving	3-5
Output Rise and Fall Times	3-5
Interconnection Delays	3-5
Absolute Maximum Ratings	3-6
DEFINITION OF SYMBOLS AND TERMS	3-7
Currents	3-7
Voltages	3-7
AC Switching Parameters and Waveforms	3-8
TESTING	3-10
DC Test Circuits	3-10
AC Test Circuits	3-11
APPLICATIONS ASSISTANCE FORM	3-13
CHAPTER 4 — FAST DATA SHEETS	4-1
CHAPTER 5 — LS DATA SHEETS	5-1
CHAPTER 6 — RELIABILITY DATA	6-1
The "Better" Program	6-2
"RAP" Reliability Audit Program	6-2
CHAPTER 7 — PACKAGE INFORMATION INCLUDING SURFACE MOUNT	7-1

Device	Description	Page
MC54/74F00	Quad 2-Input NAND Gate	4-2
MC54/74F02	Quad 2-Input NOR Gate	4-4
MC54/74F04	Hex Inverter	4-6
MC54/74F08	Quad 2-Input AND Gate	4-8
MC54/74F10	Triple 3-Input NAND Gate	4-10
MC54/74F11	Triple 3-Input AND Gate	4-12
MC54/74F13	Dual 4-Input NAND Schmitt Trigger	4-14
MC54/74F14	Hex Inverter Schmitt Trigger	4-14
MC54/74F20	Dual 4-Input NAND Gate	4-17
MC54/74F21	Dual 4-Input AND Gate	4-19
MC54/74F32	Quad 2-Input OR Gate	4-21
MC74F37	Quad 2-Input NAND Buffer	4-23
MC74F38	Quad 2-Input NAND Buffer OC	4-25
MC74F40	Dual 4-Input NAND Buffer	4-27
MC54/74F51	2 Wide 2/3 Input AND/OR/INVERT Gate	4-29
MC54/74F64	4-2-3-2 Input AND/OR/INVERT Gate	4-31
MC54/74F74	Dual D Flip-Flop	4-33
MC54/74F85	4-Bit Magnitude Comparator	4-36
MC54/74F86	Quad Exclusive/OR Gate	4-40
MC54/74F109	Dual J-K Flip-Flop w/Preset	4-42
MC74F112	Dual J-K Negative Edge-Triggered Flip-Flop	4-45
MC54/74F125	Quad Buffer, 3-State	4-48
MC54/74F126	Quad Buffer, 3-State	4-48
MC54/74F132	Quad 2-Input NAND Schmitt Trigger	4-51
MC54/74F138	1-of-8 Decoder/Demultiplexer	4-53
MC54/74F139	Dual 1-of-4 Decoder	4-56
MC54/74F148	8-Line to 3-Line Priority Encoder	4-59
MC54/74F151	8-Input Multiplexer	4-62
MC54/74F153	Dual 4-Input Multiplexer	4-64
MC74F157A	Quad 2-Input Multiplexer	4-67
MC74F158A	Quad 2-Input Multiplexer	4-69
MC74F160A	Synchronous Presettable BCD Decade Counter (Asynchronous Master Reset)	4-71
MC74F161A	Synchronous Presettable Binary Counter (Asynchronous Master Reset)	4-75
MC74F162A	Synchronous Presettable BCD Decade Counter	4-71
MC74F163A	Synchronous Presettable Binary Counter	4-75
MC54/74F164	8-Bit Serial-In, Parallel-Out Shift Register	4-79
MC54/74F168	Up/Down Decade Counter	4-82
MC54/74F169	Up/Down Binary Counter	4-82
MC54/74F174	Hex D Flip-Flop, Master Reset	4-86
MC54/74F175	Quad D Flip-Flop	4-89
MC54/74F181	4-Bit ALU	4-92
MC54/74F182	Look Ahead Carry Generator	4-97
MC74F194	Universal Shift Register	4-101
MC74F195	4-Bit Parallel Access Shift Register	4-104
MC54/74F240	Octal Buffer/Line Driver/3-State	4-108
MC54/74F241	Octal Buffer/Line Driver/3-State	4-108
MC54/74F242	Quad Bus Transceiver	4-112
MC54/74F243	Quad Bus Transceiver	4-112
MC54/74F244	Octal Buffer/Line Driver/3-State	4-108
MC54/74F245	Octal Bidirectional Transceiver/3-State	4-115

Device	Description	Page
MC54/74F251	8-Input Multiplexer/3-State	4-117
MC54/74F253	Dual 4-Input Multiplexer/3-State	4-120
MC54/74F256	Dual 4-Bit Addressable Latch	4-123
MC74F257A	Quad 2-Input Multiplexer, Non-Inverting 3-State	4-127
MC74F258A	Quad 2-Input Multiplexer, Inverting 3-State	4-130
MC54/74F259	8-Bit Addressable Latch	4-133
MC74F269	8-Bit Bidirectional Binary Counter	4-138
MC54/74F280	9-Bit Parity Generator/Checker	4-143
MC54/74F283	4-Bit Full Adder	4-146
MC74F299	8-Bit Universal Shift/Storage Register with Common Parallel I/O Pins	4-150
MC74F323	8-Input Shift/Storage Register with Synchronous Reset and Common I/O Pins	4-154
MC54/74F350	4-Bit Shifter/3-State	4-157
MC54/74F352	Dual 4-Input Multiplexer	4-161
MC54/74F353	Dual 4-Input Multiplexer/3-State	4-164
MC54/74F365	Hex Buffer, Non-Inverting, 3-State	4-167
MC54/74F366	Hex Buffer, Inverting, 3-State	4-167
MC54/74F367	Hex Buffer, 2/4 Bit, Non-Inverting, 3-State	4-169
MC54/74F368	Hex Buffer, 2/4 Bit, Inverting, 3-State	4-169
MC54/74F373	Octal Transparent Latch/3-State	4-171
MC54/74F374	Octal D Flip-Flop/3-State	4-174
MC74F377	Octal D Flip-Flop with Enable	4-177
MC54/74F378	Parallel D Register, Enable	4-180
MC54/74F379	Quad Parallel Register, Enable	4-183
MC54/74F381	4-Bit ALU	4-186
MC54/74F382	4-Bit ALU	4-191
MC54/74F398	Quad 2-Port Register	4-196
MC54/74F399	Quad 2-Port Register	4-199
MC54/74F521	Octal Comparator	4-202
MC54/74F533	Octal Transparent Latch/3-State	4-205
MC54/74F534	Octal D Flip-Flop/3-State	4-207
MC54/74F537	1-of-10 Decoder with 3-State Outputs	4-210
MC54/74F538	1-of-8 Decoder with 3-State Outputs	4-213
MC54/74F539	Dual 1-of-4 Decoder with 3-State Outputs	4-216
MC74F543	Octal Registered Transceiver, Non-Inverting, 3-State	4-219
MC74F544	Octal Registered Transceiver, Inverting, 3-State	4-223
MC54/74F568	Decade Up/Down Counter/3-State	4-227
MC54/74F569	Binary Up/Down Counter/3-State	4-227
MC74F574	Octal D-Type Flip-Flop with 3-State Outputs	4-233
MC74F579	8-Bit Bidirectional Binary Counter (3-State)	4-236
MC74F620	Octal Bus Transceiver with 3-State Outputs (Inverting)	4-240
MC74F623	Octal Bus Transceiver with 3-State Outputs (Non-Inverting)	4-240
MC74F640	Octal Bus Transceiver Inverting with 3-State Outputs	4-245
MC54/74F646	Octal Transceiver/Register with 3-State Outputs	4-248
MC54/74F648	Octal Transceiver/Register with 3-State Outputs	4-248
MC74F657A	Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker, 3-State	4-254
MC74F657B	Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker, 3-State	4-254
MC74F779	8-Bit Bidirectional Binary Counter (3-State)	4-259
MC74F803	Clock Driver, Quad D-Type Flip-Flop	4-263
MC54/74F827	10-Bit Buffer, Line Driver, Non-Inverting, 3-State	4-266
MC54/74F828	10-Bit Buffer, Line Driver, Inverting, 3-State	4-266

Device	Description	Page
MC74F1245	Octal Bidirectional Transceiver with 3-State Inputs/Outputs	4-269
MC74F1803	Clock Driver (Quad D-Type Flip-Flop)	4-272
MC74F3893A	Quad Futurebus Backplane Transceiver (3-State and Open Collector)	4-276
SN54/74LS00	Quad 2-Input NAND Gate	5-2
SN54/74LS01	Quad 2-Input NAND Gate, Open-Collector	5-4
SN54/74LS02	Quad 2-Input NOR Gate	5-6
SN54/74LS03	Quad 2-Input NAND Gate, Open-Collector	5-8
SN54/74LS04	Hex Inverter	5-10
SN54/74LS05	Hex Inverter, Open-Collector	5-12
SN54/74LS08	Quad 2-Input AND Gate	5-14
SN54/74LS09	Quad 2-Input AND Gate, Open Collector	5-16
SN54/74LS10	Triple 3-Input NAND Gate	5-18
SN54/74LS11	Triple 3-Input AND Gate	5-20
SN54/74LS12	Triple 3-Input NAND Gate, Open-Collector	5-22
SN54/74LS13	Dual 4-Input Schmitt Trigger	5-24
SN54/74LS14	Hex Schmitt Trigger	5-24
SN54/74LS15	Triple 3-Input AND Gate, Open-Collector	5-27
SN54/74LS20	Dual 4-Input NAND Gate	5-29
SN54/74LS21	Dual 4-Input AND Gate	5-31
SN54/74LS22	Dual 4-Input NAND Gate, Open-Collector	5-33
SN54/74LS26	Quad 2-Input NAND Buffer, Open-Collector	5-35
SN54/74LS27	Triple 3-Input NOR Gate	5-37
SN54/74LS28	Quad 2-Input NOR Buffer	5-39
SN54/74LS30	8-Input NAND Gate	5-41
SN54/74LS32	Quad 2-Input OR Gate	5-43
SN54/74LS33	Quad 2-Input NOR Buffer, Open-Collector	5-45
SN54/74LS37	Quad 2-Input NAND Buffer	5-47
SN54/74LS38	Quad 2-Input NAND Buffer, Open-Collector	5-49
SN54/74LS40	Dual 4-Input NAND Buffer	5-51
SN54/74LS42	1-of-10 Decoder	5-53
SN54/74LS47	BCD to 7-Segment Decoder/Driver, Open-Collector	5-56
SN54/74LS48	BCD to 7-Segment Decoder/Driver	5-59
SN54/74LS51	Dual AND-OR-INVERT Gate	5-62
SN54/74LS54	3-2-2-3-Input AND-OR-INVERT Gate	5-64
SN54/74LS55	2-Wide 4-Input AND-OR-INVERT Gate	5-66
SN54/74LS73A	Dual J-K Flip-Flop	5-68
SN54/74LS74A	Dual D Flip-Flop	5-71
SN54/74LS75	4-Bit D Latch with Q and \bar{Q}	5-74
SN54/74LS76A	Dual J-K Flip-Flop	5-78
SN54/74LS77	4-Bit D Latch with Q	5-74
SN54/74LS83A	4-Bit Full Adder	5-80
SN54/74LS85	4-Bit Magnitude Comparator	5-83
SN54/74LS86	Quad Exclusive OR Gate	5-87
SN54/74LS90	Decade Counter	5-89
SN54/74LS92	Divide-by-12 Counter	5-89
SN54/74LS93	4-Bit Binary Counter	5-89
SN54/74LS95B	4-Bit Shift Register	5-95
SN54/74LS107A	Dual J-K Negative Edge-Triggered Flip-Flop	5-99
SN54/74LS109A	Dual J-K Edge-Triggered Flip-Flop	5-101
SN54/74LS112A	Dual J-K Edge-Triggered Flip-Flop	5-103

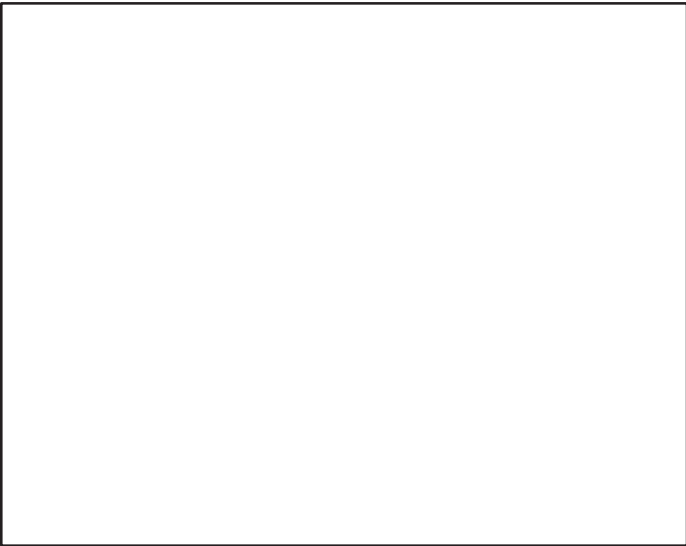
Device	Description	Page
SN54/74LS113A	Dual J-K Edge-Triggered Flip-Flop	5-105
SN54/74LS114A	Dual J-K Edge-Triggered Flip-Flop	5-107
SN54/74LS122	Retriggerable Monostable Multivibrator	5-109
SN54/74LS123	Retriggerable Monostable Multivibrator	5-109
SN54/74LS125A	Quad 3-State Buffer, Low Enable	5-117
SN54/74LS126A	Quad 3-State Buffer, High Enable	5-117
SN54/74LS132	Quad 2-Input Schmitt Trigger	5-120
SN54/74LS133	13-Input NAND Gate	5-123
SN74LS136	Quad Exclusive OR Gate, Open-Collector	5-125
SN54/74LS137	3-Line to 8-Line Decoder/Demultiplexer	5-127
SN54/74LS138	1-of-8 Decoder/Demultiplexer	5-130
SN54/74LS139	Dual 1-of-4 Decoder/Demultiplexer	5-133
SN54/74LS145	1-of-10 Decoder/Driver, Open-Collector	5-136
SN54/74LS147	10-Input to 4-Line Priority Encoder	5-139
SN54/74LS148	8-Input to 3-Line Priority Encoder	5-139
SN54/74LS151	8-Input Multiplexer	5-144
SN54/74LS153	Dual 4-Input Multiplexer	5-147
SN54/74LS155	Dual 1-of-4 Decoder/Demultiplexer	5-150
SN54/74LS156	Dual 1-of-4 Decoder/Demultiplexer, Open-Collector	5-150
SN54/74LS157	Quad 2-Input Multiplexer, Non-Inverting	5-154
SN54/74LS158	Quad 2-Input Multiplexer, Inverting	5-157
SN54/74LS160A	BCD Decade Counter, Asynchronous Reset (9310 Type)	5-160
SN54/74LS161A	4-Bit Binary Counter, Asynchronous Reset (9316 Type)	5-160
SN54/74LS162A	BCD Decade Counter, Synchronous Reset	5-160
SN54/74LS163A	4-Bit Binary Counter, Synchronous Reset	5-160
SN54/74LS164	8-Bit Shift Register, Serial-In/Parallel Out	5-166
SN54/74LS165	8-Bit Parallel-To-Serial Shift Register	5-170
SN54/74LS166	8-Bit Shift Register	5-174
SN54/74LS168	BCD Decade Counters	5-178
SN54/74LS169	Module 16 Binary, Bi-Directional Counters	5-178
SN54/74LS170	4 x 4 Register File, Open-Collector	5-184
SN54/74LS173A	4-Bit D-Type Register, 3-State	5-188
SN54/74LS174	Hex D-Type Flip-Flop with Clear	5-192
SN54/74LS175	Quad D-Type Flip-Flop with Clear	5-195
SN54/74LS181	4-Bit ALU	5-198
SN54/74LS190	Up/Down Decade Counter	5-205
SN54/74LS191	Up/Down Binary Counter	5-205
SN54/74LS192	Up/Down Decade Counter	5-213
SN54/74LS193	Up/Down Binary Counter	5-213
SN54/74LS194A	4-Bit Right/Left Shift Register	5-220
SN54/74LS195A	4-Bit Shift Register (9300 Type)	5-224
SN54/74LS196	Decade Counter	5-228
SN54/74LS197	4-Bit Binary Counter	5-228
SN54/74LS221	Dual Monostable Multivibrator	5-234
SN54/74LS240	Octal 3-State Driver, Inverting	5-239
SN54/74LS241	Octal 3-State Driver, Non-Inverting	5-239
SN54/74LS242	Quad Bus Transceiver, Inverting	5-243
SN54/74LS243	Quad Bus Transceiver, Non-Inverting	5-243
SN54/74LS244	Octal 3-State Driver, Non-Inverting	5-239
SN54/74LS245	Octal Bus Transceiver, 3-State, Non-Inverting	5-246

Device	Description	Page
SN54/74LS247	BCD to 7-Segment Decoder/Driver, Open-Collector	5-248
SN54/74LS248	BCD to 7-Segment Decoder/Driver	5-248
SN54/74LS249	BCD to 7-Segment Decoder/Driver, Open-Collector	5-248
SN54/74LS251	8-Input Multiplexer, 3-State	5-254
SN54/74LS253	Dual 4-Input Multiplexer, 3-State	5-258
SN54/74LS256	Dual 4-Bit Addressable Latch	5-261
SN54/74LS257B	Quad 2-Input Multiplexer, 3-State Outputs	5-265
SN54/74LS258B	Quad 2-Input Multiplexer, 3-State Outputs	5-265
SN54/74LS259	8-Bit Addressable Latch (9334)	5-269
SN54/74LS260	Dual 5-Input NOR Gate	5-273
SN54/74LS266	Quad Exclusive NOR Gate, Open-Collector	5-275
SN54/74LS273	Octal D-Type Flip-Flop with Clear	5-277
SN54/74LS279	Quad Set-Reset Latch	5-280
SN54/74LS280	9-Bit Odd/Even Parity Generator/Checker	5-282
SN54/74LS283	4-Bit Full Adder (Rotated LS83A)	5-284
SN54/74LS290	Decade Counter	5-288
SN54/74LS293	4-Bit Binary Counter	5-288
SN54/74LS298	Quad 2-Input Multiplexer with Output Register	5-293
SN54/74LS299	8-Bit Shift/Storage Register, 3-State	5-297
SN54/74LS322A	8-Bit Shift Register with Sign Extend	5-302
SN54/74LS323	8-Bit Universal Shift/Storage Register, 3-State	5-306
SN54/74LS348	8-Input to 3-Line Priority Encoder, 3-State	5-311
SN54/74LS352	Dual 4-Input Multiplexer	5-315
SN54/74LS353	Dual 4-Input Multiplexer, 3-State LS352	5-318
SN54/74LS365A	Hex Buffer with Common Enable, 3-State	5-322
SN54/74LS366A	Hex Inverter with Common Enable, 3-State	5-322
SN54/74LS367A	Hex Buffer, 4-Bit and 2-Bit, 3-State	5-322
SN54/74LS368A	Hex-Inverter, 4-Bit and 2-Bit, 3-State	5-322
SN54/74LS373	Octal Transparent Latch, 3-State	5-325
SN54/74LS374	Octal D-Type Flip-Flop, 3-State	5-325
SN54/74LS375	4-Bit D Latch with Q and \bar{Q}	5-330
SN54/74LS377	Octal D-Type Flip-Flop with Enable	5-333
SN54/74LS378	Hex D-Type Flip-Flop with Enable	5-333
SN54/74LS379	4-Bit D-Type Flip-Flop with Enable	5-333
SN54/74LS386	Quad Exclusive OR Gate	5-338
SN54/74LS390	Dual Decade Counter	5-340
SN54/74LS393	Dual 4-Bit Binary Counter	5-340
SN74LS395	4-Bit Shift Register, 3-State	5-345
SN54/74LS398	Quad 2-Input Multiplexer with Output Register	5-349
SN54/74LS399	Quad 2-Input Multiplexer with Output Register	5-349
SN54/74LS490	Dual Decade Counter	5-353
SN54/74LS540	Octal 3-State Driver, Inverting	5-356
SN54/74LS541	Octal 3-State Driver, Non-Inverting	5-356
SN54/74LS569A	Binary Up/Down Counter, 3-State	5-359
SN54/74LS623	Octal Transceiver with Storage, 3-State	5-364
SN54/74LS640	Octal Bus Transceiver with 3-State Output	5-367
SN54/74LS641	Octal Bus Transceiver, Open Collector	5-367
SN54/74LS642	Octal Bus Transceiver, Open Collector	5-367
SN54/74LS645	Octal Bus Transceiver with 3-State Output	5-367
SN54/74LS669	Synchronous 4-Bit Up/Down Counters	5-370

Device	Description	Page
SN54/74LS670	4 x 4 Register File, 3-State	5-374
SN54/74LS682	8-Bit Magnitude Comparator	5-378
SN54/74LS684	8-Bit Magnitude Comparator	5-378
SN54/74LS688	8-Bit Magnitude Comparator	5-378
SN54/74LS748	8-Input to 3-Line Priority Encoder (Glitchless)	5-139
SN54/74LS795	Octal Buffer (81LS95), 3-State	5-382
SN54/74LS796	Octal Buffer (81LS96), 3-State	5-382
SN54/74LS797	Octal Buffer (81LS97), 3-State	5-382
SN54/74LS798	Octal Buffer (81LS98), 3-State	5-382
SN54/74LS848	8-Input to 3-Line Priority Encoder, 3-State (Glitchless)	5-311

Selection Information
FAST/LS TTL

FAST AND LS TTL



GENERAL INFORMATION

TTL in Perspective

Since its introduction, TTL has become the most popular form of digital logic. It has evolved from the original gold-doped saturated 7400 logic, to Schottky-Clamped logic, and finally to the modern advanced families of TTL logic. The popularity of these TTL families stem from their ease of use, low cost, medium-to-high speed operation, and good output drive capability.

Motorola offers two modern TTL logic families — LS and FAST™. They are pin and functionally compatible and can easily be combined in a system to achieve maximum performance at minimum cost.

LS (Low Power Schottky) is currently the more popular and commands by far the largest share of the total TTL logic market. It is low-cost and provides moderate performance at low power.

FAST, the state-of-the-art, high-performance TTL family, is growing rapidly and gaining a significant share of the total TTL logic market. FAST offers a 20–30 percent improvement in performance over the older Standard Schottky family (74S) with a 75–80 percent reduction in power. When compared with the Advanced Schottky family (74AS), FAST offers nearly equal performance at a 25–50 percent savings in power.

FAST is manufactured on Motorola's MOSAIC (oxide-isolated) process. This process provides FAST with inherent speed/power advantages over the older junction-isolated 74S and 74LS families, allowing the FAST family to be designed and specified with improved noise margins, reduced input currents, and superior line driving capabilities in comparison to these earlier families. Additionally, FAST designs incorporate power-down circuitry on all three-state outputs, and buffered outputs on all storage devices.

Two further advantages of FAST are the load specifications and power supply specifications. FAST ac characteristics are specified at a heavier capacitive load than the earlier families (50 pF versus 15 pF) to more accurately reflect actual in-circuit performance. Motorola's dc and ac characteristics for FAST are specified over a full 10% supply voltage range — a significant improvement over the industry standard specifications for the earlier families (5% for dc, 0% for ac).

These design and specification improvements offered by the Motorola FAST family provide the user with better system performance, enhanced design flexibility, and more reliable system operation.

TTL Family Comparisons

General Characteristics for Schottky TTL Logic

(ALL MAXIMUM RATINGS)		LS		FAST		
Characteristic	Symbol	54LSxxx	74LSxxx	54Fxxx	74Fxxx	Unit
Operating Voltage Range	V _{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	Vdc
Operating Temperature Range	T _A	–55 to 125	0 to 70	–55 to 125	0 to 70	°C
Input Current	I _{IN} I _{IH}	20	20	20	20	μA
	I _{IL}	–400	–400	–600	–600	
Output Drive Standard Output	I _{OH}	–0.4	–0.4	–1.0	–1.0	mA
	I _{OL}	4.0	8.0	20	20	mA
	I _{SC}	–20 to –100	–20 to –100	–60 to –150	–60 to –150	mA
Buffer Output	I _{OH}	–12	–15	–12	–15	mA
	I _{OL}	12	24	48	64	mA
	I _{SC}	–40 to –225	–40 to –225	–100 to –225	–100 to –225	mA

Speed/Power Characteristics for Schottky TTL Logic(1)

(ALL TYPICAL RATINGS)

Characteristic	Symbol	LS	FAST	Unit
Quiescent Supply Current/Gate	I _G	0.4	1.1	mA
Power/Gate (Quiescent)	P _G	2.0	5.5	mW
Propagation Delay	t _p	9.0	3.7	ns
Speed Power Product	—	18	19.2	pJ
Clock Frequency (D-F/F)	f _{max}	33	125	MHz
Clock Frequency (Counter)	f _{max}	40	125	MHz

NOTES: 1. Specifications are shown for the following conditions:

a) V_{CC} = 5.0 Vdc (AC);

b) T_A = 25°C

c) C_L = 50 pF for FAST; 15 pF for LS

Functional Selection

Abbreviations

- S** = Synchronous
A = Asynchronous
B = Both Synchronous and Asynchronous

2S = 2-State Output
3S = 3-State Output
OC = Open-Collector Output

P = Planned (See FAST/LS Selector Guide, SG-60 for latest availability status)
X = Available

Inverters

Description	Type of Output	No.	LS	FAST
Hex	2S	04	X	X
	OC	05	X	

AND Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	08	X	X
	OC	09	X	
Triple 3-Input	2S	11	X	X
	OC	15	X	
Dual 4-Input	2S	21	X	X

NAND Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	00	X	X
	OC	01	X	
	OC	03	X	
Quad 2-Input, High Voltage	OC	26	X	
	2S	10	X	X
Triple 3-Input	OC	12	X	
	2S	20	X	X
Dual 4-Input	OC	22	X	
	2S	30	X	
8-Input	2S	30	X	
13-Input	2S	133	X	

OR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	32	X	X

NOR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	02	X	X
Triple 3-Input	2S	27	X	
Dual 5-Input	2S	260	X	

Exclusive OR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	2S	86	X	X
	OC	136	X	
	2S	386	X	

Exclusive NOR Gates

Description	Type of Output	No.	LS	FAST
Quad 2-Input	OC	266	X	

AND-OR-INVERT Gates

Description	Type of Output	No.	LS	FAST
Dual 2-Wide, 2-Input 3-Input	2S	51	X	X
4-Wide, 2-3-2-3-Input	2S	54	X	
2-Wide, 4-Input	2S	55	X	
4-Wide, 4-2-2-3-Input	2S	64		X

Schmitt Triggers

Description	Type of Output	No.	LS	FAST
Dual 4-Input NAND Gate	2S	13	X	X
Hex, Inverting	2S	14	X	X
Quad 2-Input NAND Gate	2S	132	X	X

SSI Flip-Flops

Description	Clock Edge	No.	LS	FAST
Dual D w/Set & Clear	Pos	74		X
Dual D w/Set & Clear	Pos	74A	X	
Dual JK w/Set	Neg	113A	X	
Dual JK w/Clear	Neg	73A	X	
Same as 73A with Different Pinout	Neg	107A	X	
Dual JK w/Set & Clear Individual J, K, C _p , S _D , C _D Inputs	Neg	76A	X	
Same as 76 with Different Pinout	Neg	112		X
Same as 76A with Different Pinout	Neg	112A	X	
Same as 112 with Different Pinout	Neg	114A	X	
Dual JK w/Set & Clear	Pos	109		X
Dual JK w/Set & Clear	Pos	109A	X	

Multiplexers

Description	Type of Output	No.	LS	FAST
Quad 2-to-1, Non-Inverting	2S	157	X	
	2S	157A		X
	3S	257A		X
	3S	257B	X	
Quad 2-to-1, Inverting	2S	158	X	
	2S	158A		X
	3S	258A		X
	3S	258B	X	
Dual 4-to-1, Non-Inverting	2S	153	X	X
	3S	253	X	X
Dual 4-to-1, Inverting	2S	352	X	X
	3S	353	X	X
8-to-1	2S	151	X	X
	3S	251	X	X
	2S	298	X	
Quad 2-to-1 with Output Register 398 — Positive edge triggered, Q/O Outputs	2S	398	X	X
	2S	399	X	X

Encoders

Description	Type of Output	No.	LS	FAST
10-to-4-Line BCD	2S	147	X	
8-to-3-Line Priority Encoder	2S	148	X	X
	3S	348	X	
	2S	748	X	
	3S	848	X	

Register Files

Description	Type of Output	No.	LS	FAST
4 x 4	OC	170	X	
	3S	670	X	

Shift Registers

Description	No. of Bits	Type of Output	Mode*				No.	LS	FAST
			SR	SL	Hold	Reset			
Serial In-Parallel Out	8	2S	X			A	164	X	X
Parallel In-Serial Out	8	2S	X			X	165	X	
	8	2S	X			X	166	X	
Parallel In-Parallel Out	4	2S	X			A	95B	X	
	4	2S	X	X	X	A	194		X
	4	2S	X	X	X	A	194A	X	
	4	2S	X			A	195		X
	4	2S	X			A	195A	X	
	4	3S	X			A	395	X	
	4	3S	X			A	395	X	
Parallel In-Parallel Out, Bidirectional	8	3S	X	X	X	A	299	X	X
	8	3S	X	X	X	S	323	X	X
Sign Extended Bidirectional	8	3S	X		X	A	322A	X	

* SR = Shift Right
SL = Shift Left

Decoders/Demultiplexers

Description	Type of Output	No.	LS	FAST
Dual 1-of-4	2S	139	X	X
	2S	155	X	
	OC	156	X	
1-of-8	3S	539		X
	2S	138	X	X
	3S	538		X
1-of-8 with Latch	2S	137	X	
1-of-10	2S	42	X	
	3S	537		X

Latches

Description	No. of Bits	Type of Output	No.	LS	FAST
Transparent, Non-Inverting	4	2S	77	X	
	8	3S	373	X	X
Octal, Non-Inverting	8	3S	573		
Transparent, Inverting	8	3S	533		X
Transparent, Q and Q Outputs	4	2S	75	X	
	4	2S	375	X	
Quad Set-Reset Latch	4	2S	279	X	
Addressable	8	2S	259	X	X
Dual 4-Bit Addressable	4	2S	256	X	X

Asynchronous Counters — Negative Edge-Triggered

Description	Load	Set	Reset	No.	LS	FAST
Decade (2/5)	X	X	X	90	X	
			X	196	X	
		X	X	290	X	
Dual Decade (2/5)			X	390	X	
Dual Decade		X	X	490	X	
Modulo 12 (2/6)			X	92	X	
4-Bit Binary (2/8)	X		X	93	X	
			X	197	X	
Dual 4-Bit Binary			X	293	X	
			X	393	X	

* The 716 and 718 are positive edge-triggered.

Display Decoders/Drivers with Open-Collector Outputs

Description	No.	LS	FAST
1-of-10	145	X	
BCD-to-7 Segment	47	X	
	48*	X	
	247	X	
	248*	X	
	249	X	

* The 48 and 248 have internal pull up resistors to V_{CC} on their outputs.

Cascadable Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.	LS	FAST
Decade	2S	S	A	160A	X	X
	2S	S	S	162A	X	X
Decade, Up/Down	2S	S		168	X	X
	2S	A		190	X	
	2S	A	A	192*	X	
	3S	S	B	568		X
4-Bit Binary	2S	S	A	161A	X	X
	2S	S	S	163A	X	X
4-Bit Binary, Up/Down	2S	S		169	X	X
	2S	A		191	X	
	2S	A	A	193*	X	
	3S	S	B	569		X
8 Bit Binary, Up/Down	3S	S	B	569A	X	
	2S	S		669	X	
	3S	S	S	579		X
	3S	S		779		X
	3S	S		269		X

* The 192 and 193 do not provide a clock enable for synchronous cascading.

MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.	LS	FAST
D-Type, Non-Inverting	4	3S	A	X	173A	X	
	4	2S		X	377	X	X
	6	2S	A		174	X	X
	6	2S		X	378	X	X
	8	2S	A		273	X	
	8	3S			374	X	X
	8	3S			574		X
	Quad 2-Port	4	2S	A	X	398	X
D-Type, Inverting	4	2S	A	X	399	X	X
	8	3S			534		X
D-Type, Q and \bar{Q} Outputs	8	3S			564		
	4	2S	A		175	X	X
	4	2S		X	379	X	X

Arithmetic Operators

Description	No.	LS	FAST
4-Bit Adder	83	X	
	283	X	X
4-Bit ALU	181	X	X
	381		X
	382		X
Look-Ahead Carry Generator	182		X
4-Bit Barrel Shifter	350		X

Magnitude Comparators

Description	Type of Output	P = Q	P > Q	P < Q	No.	LS	FAST
4-Bit	2S	X	X	X	85	X	X
8-Bit	2S	X	X		682	X	
	2S	X	X		684	X	
	2S	X			521		X
8-Bit with Output Enable	2S	X			688	X	

Parity Generators/Checkers

Description	No.	LS	FAST
9-Bit Odd Even Parity Generator Checker	280	X	X

VCOs and Multivibrators

Description	No.	LS	FAST
Retriggerable Monostable Multivibrator	122	X	
Dual 122	123	X	
Precision Non-Retriggerable Monostable Multivibrator	221	X	

Buffers/Line Drivers

Description	Type of Output	No.	LS	FAST
Quad 2-Input NOR	2S	28	X	
	OC	33	X	
Quad 2-Input NAND	2S	37	X	X
	OC	38	X	X
Dual 4-Input NAND	2S	40	X	X
Quad, Non-Inverting	3S	125		X
		125A	X	
	3S	126		X
		126A	X	
Hex, Non-Inverting	3S	365		X
		365A	X	
	3S	367		X
		367A	X	
Hex, Inverting	3S	366		X
		366A	X	
	3S	368		X
		368A	X	
Octal, Non-Inverting	3S	241	X	X
	3S	244	X	X
Bus Pinout	3S	541	X	
	3S	795	X	
	3S	797	X	
Octal, Inverting	3S	240	X	X
Bus Pinout	3S	540	X	
	3S	796	X	
	3S	798	X	
10-Bit	3S	827		X
		828		X

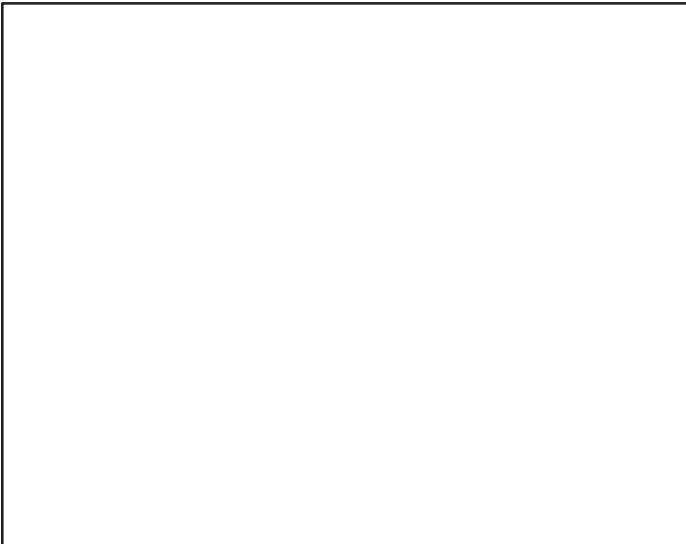
Transceivers

Description	Type of Output	No.	LS	FAST
Quad, Non-Inverting	3S	243	X	X
Quad, FutureBus	3S	3893A		X
Quad, Inverting	3S	242	X	X
Octal, Non-Inverting	3S	245	X	X
	3S	645	X	
	3S	623	X	X
	OC	641	X	
	3S	1245		X
Octal, Inverting	3S	620		X
	3S	640	X	X
	OC	642	X	
Octal, Non-Inverting Register	3S	646		X
Latch	3S	543		X
Octal, Inverting Register	3S	544		X
Octal w/ Parity Gen/Checker	3S	657A		X
		657B		X

Clock Drivers

Description	No.	LS	FAST
Quad Matched Propagation Delays	803		X
Clock Driver	1803		X

FAST AND LS TTL



CIRCUIT CHARACTERISTICS

FAMILY CHARACTERISTICS

LS TTL

The Low Power Schottky (LSTTL) family combines a current and power reduction improvement over standard 7400 TTL by a factor of 5. This is accomplished by using Schottky diode clamping to prevent saturation and advanced processing.

FAST TTL

The FAST Schottky TTL family provides a 75–80% power reduction compared to standard Schottky (54/74S) TTL and yet offers a 20–40% improvement in circuit performance over the standard Schottky due to the MOSAIC process. Also, FAST circuits contain additional circuitry to provide a flatter power/frequency curve. The input configuration of FAST uses a lower input current which translates into higher fanout.

CIRCUIT FEATURES

Circuit features of LS and FAST are best understood by examining the TTL 2-input NAND gate of each family (Figures 2-1a, b). The input/output circuits of other functions are almost identical.

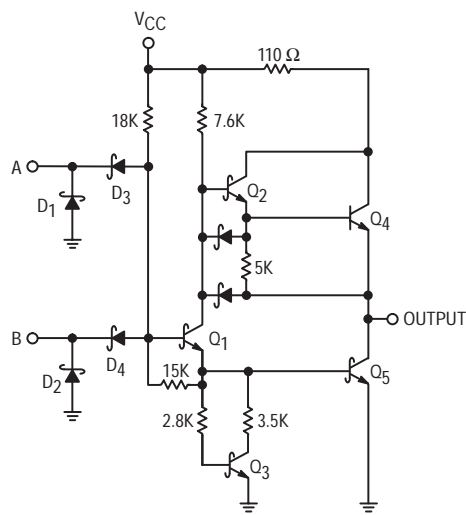


Figure 2-1a. LS00 — 2-Input NAND Gate

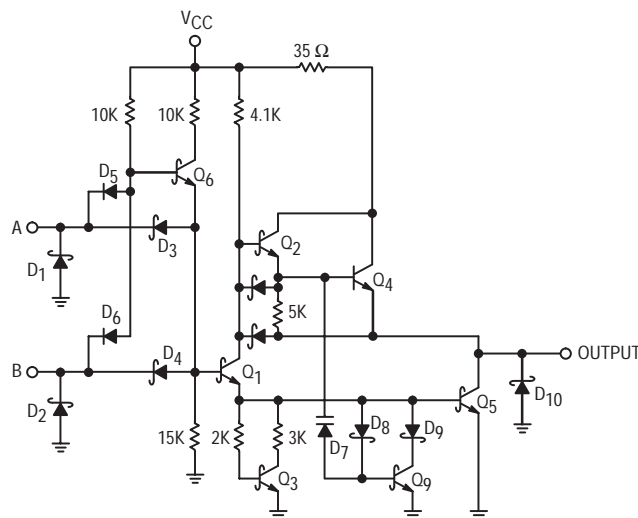


Figure 2-1b. F00 — 2-Input NAND Gate

INPUT CONFIGURATION. Motorola LSTTL circuits do not use the multi-emitter input structure that originally gave TTL its name. Most LS elements use a DTL type input circuit with Schottky diodes to perform the AND function, as exemplified by D3 and D4 in Figure 2-1a. Compared to the classical multi-emitter structure, this circuit is faster and increases the input breakdown voltage. Inputs of this type are tested for leakage with an applied input voltage of 7.0 V and the input breakdown voltage is typically 15 V or more.

The F00 input configuration utilizes a PN diode (D5 and D6) rather than the PNP transistor. This is required due to the high speed response of FAST™ logic. The PNP transistor, a relatively large device in current bipolar logic technology, has an associated capacitance large enough to make the gate input susceptible to ac noise. The PN diode results in much better ac noise immunity at the expense of increased input current.

Another input arrangement often used in LS MSI has three diodes connected as shown in Figure 2-2. This configuration gives a slightly higher input threshold than that of Figure 2-1a. A third input configuration that is sometimes used in LS TTL employs a vertical PNP transistor as shown in Figure 2-3. This arrangement also gives a higher input threshold and has the additional advantage of reducing the amount of current that the signal source must sink. Both the diode cluster arrangement and the PNP input configuration have breakdown voltage ratings greater than 7.0 V.

All inputs are provided with clamping diodes, exemplified by D1 and D2 in Figure 2-1a, b. These diodes conduct when an input signal goes negative, which limits undershoot and helps to control ringing on long signal lines following a HIGH-to-LOW transition. These diodes are intended only for the suppression of transient currents and should not be used as steady-state clamps in interface applications. A clamp current exceeding 2.0 mA and with a duration greater than 500 ns can activate a parasitic lateral NPN transistor, which in turn can steal current from internal nodes of an LS circuit and thus cause logic errors.

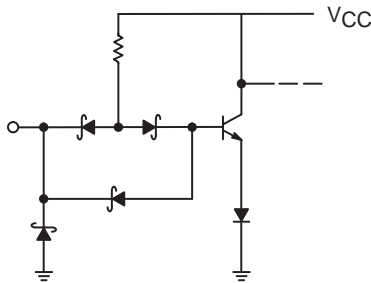


Figure 2-2. Diode Cluster Input

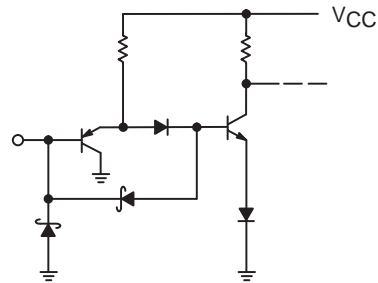


Figure 2-3. PNP Input

INPUT CHARACTERISTICS — Figure 2-4 shows the typical input characteristics of LS and FAST™. Typical transfer characteristics can be found in Figure 2-5 and input threshold variation with temperature information is provided in Table 2-1.

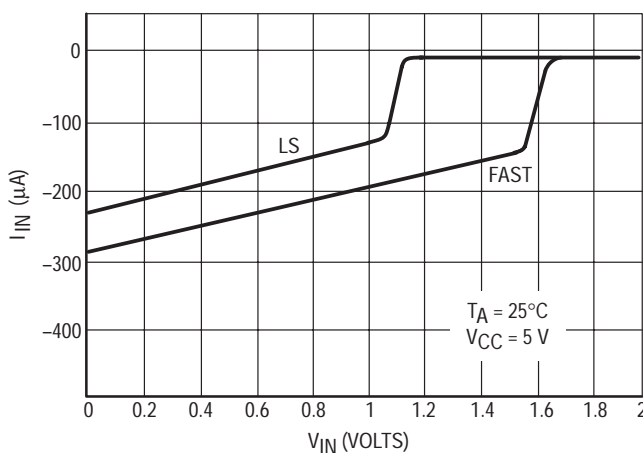


Figure 2-4. Typical Input Current versus Input Voltage

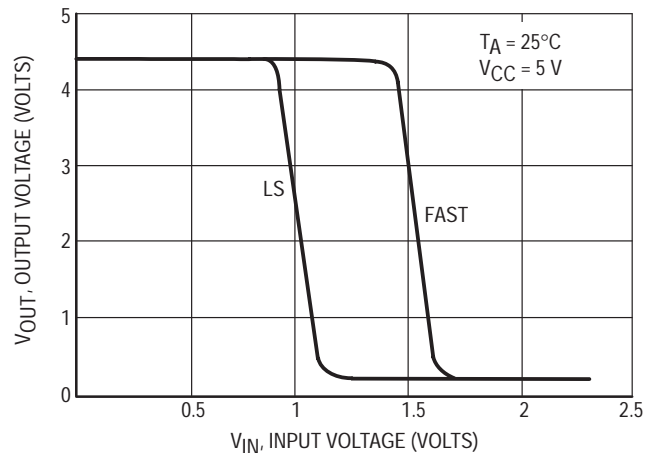


Figure 2-5. Typical Output versus Input Voltage Characteristic

Table 2.1
Typical Input Threshold Variation
With Temperature

	-55°C	+25°C	+125°C
FAST	1.8	1.5	1.3
ALS	1.8	1.5	1.3
S	1.5	1.3	1.1
LS	1.2	1.0	0.8

OUTPUT CONFIGURATION. The output circuitry of LSTTL has several features not found in conventional TTL. A few of these features are discussed below.

Referring to Figures 2-1 a, b, the base of the pull-down output transistor Q5 is returned to ground through Q3 and a pair of resistors instead of through a simple resistor. This arrangement is called a squaring network since it squares up the transfer characteristics (Figure 2-5) by preventing conduction in the phase splitter Q1 until the input voltage rises high enough to allow Q1 to supply base current to Q5. The squaring network also improves the propagation delay by providing a low resistance path to discharge capacitance at the base of Q5 during turn-off.

The output pull-up circuit is a 2-transistor Darlington circuit with the base of the output transistor returned through a 5.0K resistor to the output terminals, unlike 74H and 74S where it is returned to ground which is a more power consuming configuration. This configuration allows the output to pull up to one V_{BE} below V_{CC} for low values of output current.

The F00 output includes clamping diodes to limit undershoot and control ringing on long signal lines. As with the input diode clamps, these diodes are intended for transient suppression only and should not be used as steady-state clamps.

The F00 output configuration also includes additional circuitry to improve the rise time and decrease the power consumption at high operating frequencies. This circuit, which consists of Q9, D7, D8, and D9 causes Q5 to off more quickly on LOW to HIGH output transitions.

Figure 2-6 shows the extra circuitry used to obtain the "high Z" condition in 3-state outputs. When the Output Enable signal is HIGH, both the phase splitter and the Darlington pull-up are turned off. In this condition the output circuitry is non-conducting, which allows the outputs of two or more such circuits to be connected together in a bus application wherein only one output is enabled at any particular time.

FAST™ 3-state outputs have some additional circuitry due to the nature of the environment in which they are used. The effective capacitive load of a 3-state output tends to increase at high bus rates. The addition of Q10 reduces this effect by clamping the base of Q5 low when the device is in the high impedance state. In the high Z state, the output capacitance is about 5.0 pF for 24 mA outputs and about 12 pF for 64 mA outputs.

An additional feature of many FAST™ 3-state devices is the incorporation of power-up circuitry to guarantee that the output will not sink current if the device is disabled during the application or removal of power.

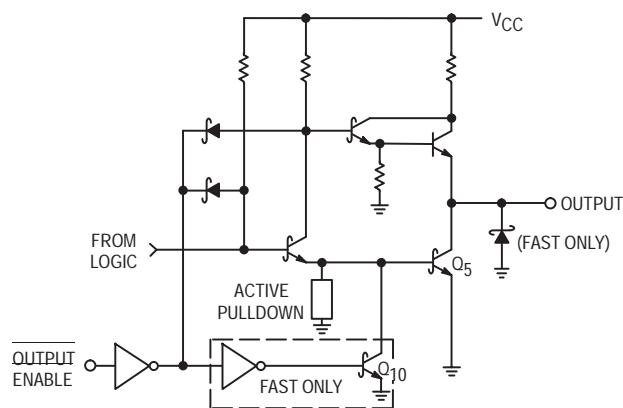


Figure 2-6. Typical 3-State Output Control

OUTPUT CHARACTERISTICS. Figure 2-7 shows the LOW-state output characteristics for LS and FAST™. For LOW I_{OL} values, the pull-down transistor is clamped out of deep saturation to shorten the turn-off delay. Figure 2-8 shows the HIGH-state output characteristics.

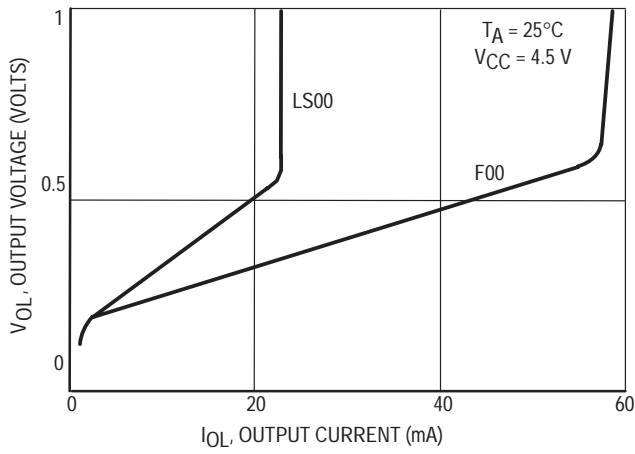


Figure 2-7a. Output Low Characteristic

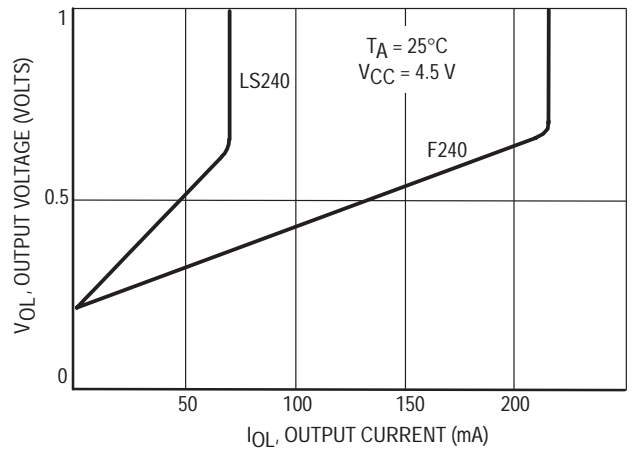


Figure 2-7b. Output Low Characteristic

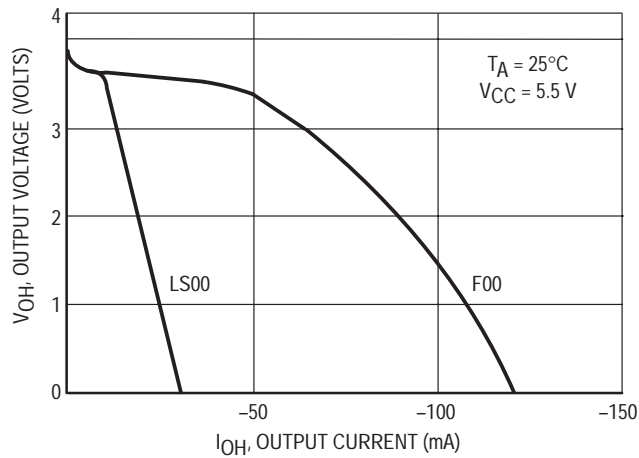


Figure 2-8a. Output High Characteristic

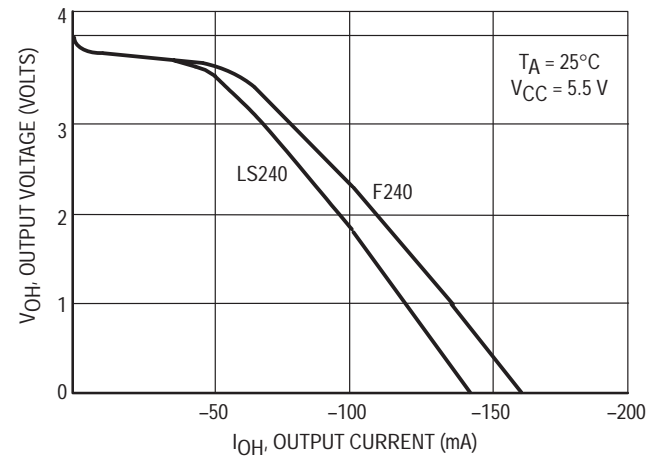


Figure 2-8b. Output High Characteristic

AC SWITCHING CHARACTERISTICS. The propagation through a logic element depends on power supply voltage, ambient temperature, and output load. The effect of each of these parameters on ac propagation is shown in Figures 2-9 through 2-11.

Propagation delays are specified with only one output switching, the delay through a logic-element will increase to some extent when multiple outputs switch simultaneously due to inductance internal to the IC package. This effect can be seen by comparing Figures 2-11c and 2-11d.

For LS TTL, limits are guaranteed at 25°C, $V_{CC} = 5.0$ V, and $C_L = 15$ pF (normally, resistive load has minimal effect on propagation delay) FAST™ and TTL limits are guaranteed over the commercial or military temperature and supply voltage ranges and with $C_L = 50$ pF.

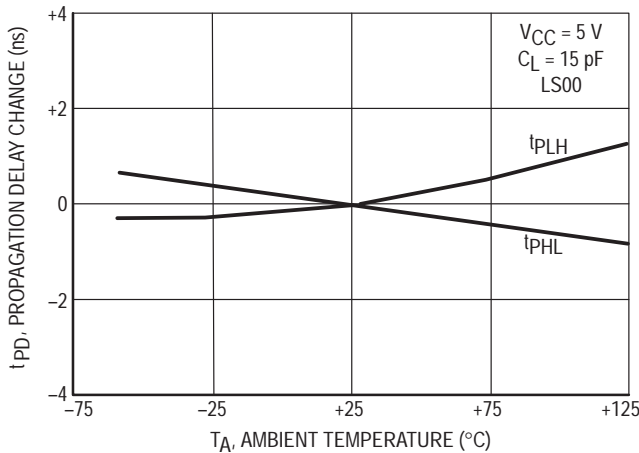


Figure 2-9

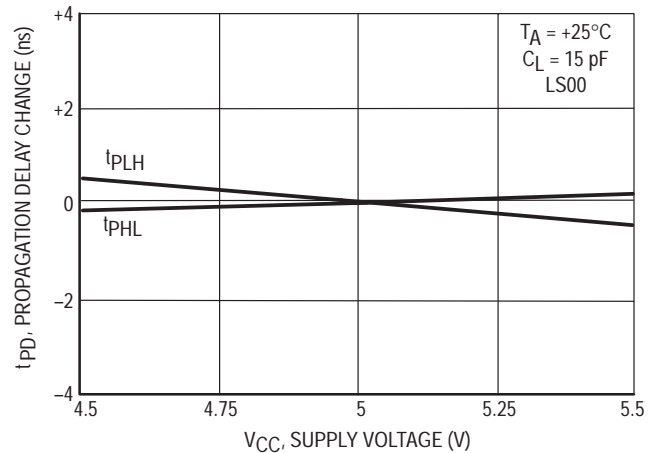


Figure 2-10

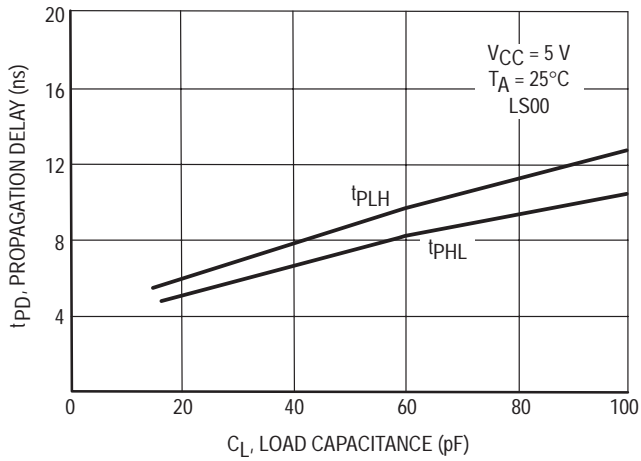


Figure 2-11a*

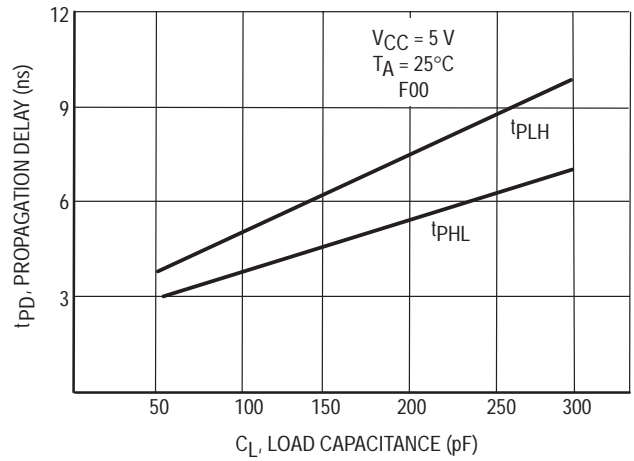


Figure 2-11b*

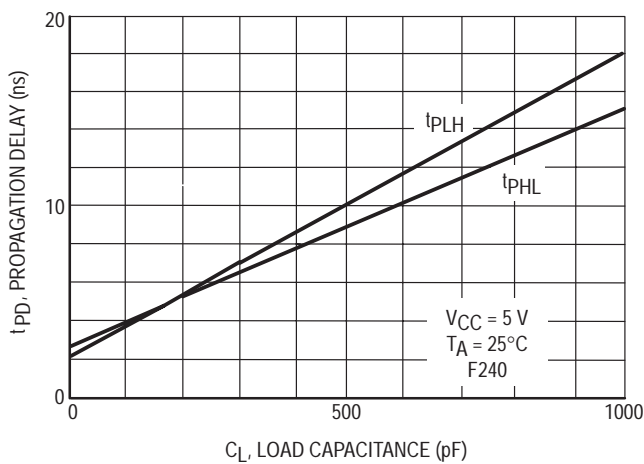


Figure 2-11c*

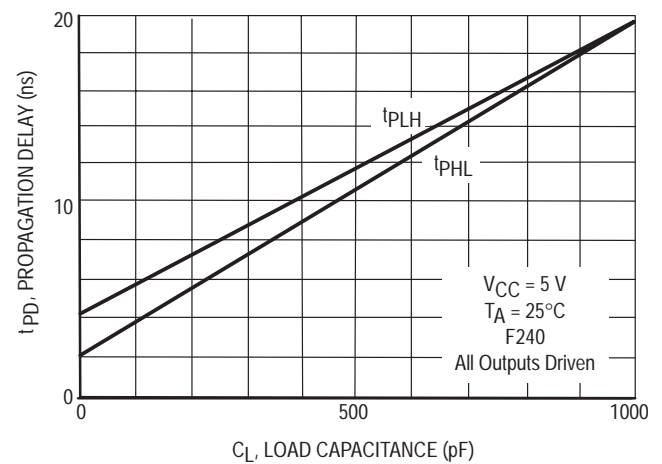


Figure 2-11d*

*Data for Figures 2-11a through 2-11c was taken with only one output switching at a time. Figure 2-11d data was taken with all 8 inputs of the F240 tied together.

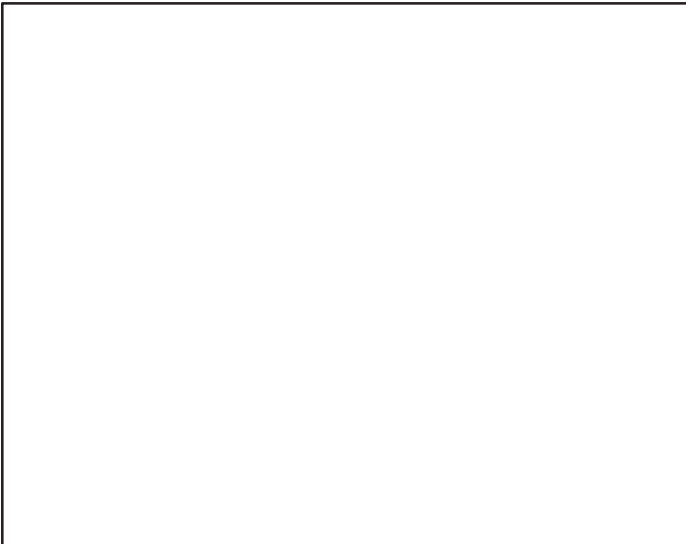
LS/FAST ESD CHARACTERISTICS. Electrostatic Discharge (ESD) sensitivity for Motorola TTL is characterized using several methodologies (HBM, MM, CDM). It is extremely important to understand that ESD sensitivity values alone are not sufficient when comparing devices. In an attempt to reduce correlation problems between various pieces of test equipment, all of which meet Mil-Std-883C requirements, tester specific information as well as actual device ESD hardness levels are given in controlled documents and are available upon request. The continuing improvements of ESD sensitivity through redesigns of Motorola TTL has resulted in minimum ESD levels for all new products and redesigns of >4000 volts for FAST and >3500 volts for LS. For device specific values reference the following specifications:

LS: 12MRM 93831A
 FAST: 12MRM 93830A

Design Considerations, Testing and Applications Assistance Form

3

FAST AND LS TTL



DESIGN CONSIDERATIONS

SELECTING TTL LOGIC. TTL Families may be mixed in a system for optimum performance. For instance, in new designs, ALS would commonly be used in non-critical speed paths to minimize power consumption while FAST™ TTL would be used in high speed paths. The ratio of ALS to FAST™ will depend on overall system design goals.

NOISE IMMUNITY. When mixing TTL families it is often desirable to know the guaranteed noise immunity for both LOW and HIGH logic levels. Table 3.1 lists the guaranteed logic levels for various TTL families and can be used to calculate noise margin. Table 3.2 specifies these noise margins for systems containing LS, S, ALS and/or FAST™ TTL. Note that Table 3.2 represents “worst case” limits and assumes a maximum power supply and temperature variation across the IC’s which are interconnected, as well as maximum rated load. Increased noise immunity can be achieved by designing with decreased maximum allowable operating ranges.

Table 3.1
Worst Case TTL Logic Levels

Electrical Characteristics

	TTL Families	Military (–5 to +125°C)				Commercial (0 to 70°C)				Unit
		V _{IL}	V _{IH}	V _{OL}	V _{OH}	V _{IL}	V _{IH}	V _{OL}	V _{OH}	
TTL	Standard TTL 9000, 54/74	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
HTTL	High Speed TTL 54/74H	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LP TTL	Low Power TTL 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
STTL	Schottky TTL 54/74S, 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LS TTL	Low Power Schottky TTL 54/74LS	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V
ALS TTL (5% V _{CC})	Advanced LS TTL, 54/74ALS					0.8	2.0	0.5	2.75	V
(10% V _{CC})		0.8	2.0	0.4	2.5	0.8	2.0	0.5	2.5	V
FAST TTL (5% V _{CC})	Advanced S TTL, 54/74F					0.8	2.0	0.5	2.7	V
(10% V _{CC})		0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.5	V

V_{OL} and V_{OH} are the voltages generated at the output V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate levels. The numbers given above are guaranteed worst-case values.

Table 3.2a
LOW Level Noise Margins (Military)

From	To	LS	S	ALS	FAST	Unit
LS		300	400	400	400	mV
S		200	300	300	300	mV
ALS		300	400	400	400	mV
FAST™		200	300	300	300	mV

From “V_{OL}” to “V_{IL}”

Table 3.2b
HIGH Level Noise Margins (Military)

From	To	LS	S	ALS	FAST	Unit
LS		500	500	500	500	mV
S		500	500	500	500	mV
ALS		500	500	500	500	mV
FAST™		500	500	500	500	mV

From “V_{OH}” to “V_{IH}”

Table 3.2c
LOW Level Noise Margins (Commercial)

From	To	LS	S	ALS	FAST	Unit
LS		300	300	300	300	mV
S		300	300	300	300	mV
ALS		300	300	300	300	mV
FAST™		300	300	300	300	mV

From “V_{OL}” to “V_{IL}”

Table 3.2d
HIGH Level Noise Margins (Commercial)

From	To	LS	S	ALS	FAST	Unit
LS		700	700	700	700	mV
S		700	700	700	700	mV
ALS (5% V _{CC})		750	750	750	750	mV
FAST (5% V _{CC})		700	700	700	700	mV
ALS (10% V _{CC})		500	500	500	500	mV
FAST (10% V _{CC})		500	500	500	500	mV

From “V_{OH}” to “V_{IH}”

POWER CONSUMPTION. With the exception of ECL, all logic families exhibit increased power consumption at high frequencies. Care must be taken when switching multiple gates at high frequencies to assure that their combined dissipation does not exceed package and/or device capabilities. TTL devices are more efficient at high frequencies than CMOS.

FAN-IN AND FAN-OUT. In order to simplify designing with Motorola TTL devices, the input and output loading parameters of all families are normalized to the following values:

1 TTL Unit Load (U.L.) = 40 μ A
in the HIGH state (Logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (Logic "0")

Input loading and output drive factors of all products described in this handbook are related to these definitions.

EXAMPLES — INPUT LOAD

1. A 7400 gate, which has a maximum I_{LL} of 1.6 mA and I_{IH} of 40 μ A is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 74LS95B which has a value of I_{LL} = 0.8 mA and I_{IH} of 40 μ A on the CP terminal, is specified as having an input LOW load factor of:

$$\frac{0.8 \text{ mA}}{1.6 \text{ mA}} \text{ or } 0.5 \text{ U.L.} \quad \text{and an input HIGH load factor of} \quad \frac{40 \mu\text{A}}{40 \mu\text{A}} \quad \text{or } 1 \text{ U.L.}$$

3. The 74LS00 gate which has an I_{LL} of 0.4 mA and an I_{IH} of 20 μ A, has an input LOW load factor of:

$$\frac{0.4 \text{ mA}}{1.6 \text{ mA}} \text{ or } 0.25 \text{ U.L.} \quad \text{an input HIGH load factor of} \quad \frac{20 \mu\text{A}}{40 \mu\text{A}} \quad \text{or } 0.5 \text{ U.L.}$$

EXAMPLES — OUTPUT DRIVE

1. The output of the 7400 will sink 16 mA in the LOW (logic "0") state and source 800 μ A in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore:

$$\frac{16 \text{ mA}}{1.6 \text{ mA}} = 10 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{800 \mu\text{A}}{40 \mu\text{A}} \text{ or } 20 \text{ U.L.}$$

2. The output of the 74LS00 will sink 8.0 mA in the LOW state and source 400 μ A in the HIGH state. The normalized output LOW drive factor is:

$$\frac{8.0 \text{ mA}}{1.6 \text{ mA}} = 5 \text{ U.L.}$$

and the output HIGH drive factor is

$$\frac{400 \mu\text{A}}{40 \mu\text{A}} \text{ or } 10 \text{ U.L.}$$

Relative load and drive factors for the basic TTL families are given in Table 3.3.

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
74LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
74 ALS	0.5 U.L.	0.0625 U.L.	10 U.L.	5 U.L.
74 FAST	0.5 U.L.	0.375 U.L.	25 U.L.	12.5 U.L.

Table 3.3

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

WIRED-OR APPLICATIONS. Certain TTL devices are provided with an “open” collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

MINIMUM AND MAXIMUM PULL-UP RESISTOR VALUES

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \cdot 1.6 \text{ mA}} \qquad R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \cdot I_{OH} + N_2(HIGH) \cdot 40 \mu\text{A}}$$

where:

- R_x = External Pull-up Resistor
- N_1 = Number of Wired-OR Outputs
- N_2 = Number of Input Unit Loads (U.L.) being Driven
- $I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
- I_{OL} = LOW Level Fan-out Current of Driving Element
- V_{OL} = Output LOW Voltage Level (0.5 V)
- V_{OH} = Output HIGH Voltage Level (2.4 V)
- V_{CC} = Power Supply Voltage

Example: Four 74LS03 gate outputs driving four other LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25 \text{ V} - 0.5 \text{ V}}{8.0 \text{ mA} - 1.6 \text{ mA}} = \frac{4.75 \text{ V}}{6.4 \text{ mA}} = 742 \Omega$$

$$R_{X(MAX)} = \frac{4.75 \text{ V} - 2.4 \text{ V}}{4 \cdot 100 \mu\text{A} + 2 \cdot 40 \mu\text{A}} = \frac{2.35 \text{ V}}{0.48 \text{ mA}} = 4.9 \text{ k}\Omega$$

where:

- N_1 = 4
- N_2 (HIGH) = 4 • 0.5 U.L. = 2 U.L.
- N_2 (LOW) = 4 • 0.25 U.L. = 1 U.L.
- I_{OH} = 100 μA
- I_{OL} = 8.0 mA
- V_{OL} = 0.5 V
- V_{OH} = 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 k Ω can be used. The lower values yield the fastest speeds while the higher values yield the lowest power dissipation.

UNUSED INPUTS. For best noise immunity and switching speed, unused TTL inputs should not be left floating, but should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC} , LS and FAST™ TTL inputs have a breakdown voltage >7.0 V and require, therefore no series resistor.
2. Connect the unused input to the output of an unused gate that is forced HIGH.

CAUTION: Do not connect an unused LS or FAST™ input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

INPUT CAPACITANCE. As a rule of thumb, LS and FAST™ TTL inputs have an average capacitance of 5.0 pF for DIP packages. For an input that serves more than one internal function, each additional function adds approximately 1.5 pF.

LINE DRIVING — Because of its superior capacitive drive characteristics, TTL logic is often used in line driving applications which require various termination techniques to maintain signal integrity. Parameters associated with this application are listed in Table 3.4.

It is also often necessary to construct load lines to determine reflection waveforms in line driving applications. The input and output characteristics graphs of section 3 (Figs. 2-4, 2-7 and 2-8) can be very useful for this purpose.

OUTPUT RISE AND FALL TIMES provide important information in determining reflection waveforms and crosstalk coefficients. Typical rise and fall times are approximately 6 ns for LS and about 2.0 ns for FAST™ with a 50 pF load (measured 10–90%). Output rise and fall times become longer as capacitive load is increased.

INTERCONNECTION DELAYS. For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. These range from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 100 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, e.g., if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

(ALL MAXIMUM RATINGS)		LS		FAST		
Characteristic	Symbol	54LSxxx	74LSxxx	54Fxxx	74Fxxx	Unit
Operating Voltage Range	V _{CC}	5 ± 10%	5 ± 5%	5 ± 10%	5 ± 10%	Vdc
Output Drive: Standard Output	I _{OH}	–0.4	–0.4	–1.0	–1.0	mA
	I _{OL}	4.0	8.0	20	20	mA
	I _{SC}	–20 to –100	–20 to –100	–60 to –150	–60 to –150	mA
Buffer Output	I _{OH}	–12	–15	–12	–15	mA
	I _{OL}	12	24	48	64	mA
	I _{SC}	–40 to –225	–40 to –225	–100 to –225	–100 to –225	mA

Table 3.4
Output Characteristics for Schottky TTL Logic

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-case situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Functional operation under these conditions is not implied.

CHARACTERISTIC	LS	FAST
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V	-0.5 V to +7.0 V
*Input Voltage (dc) Diode Inputs	-0.5 V to 15 V	-0.5 V to 7.0 V
*Input Current (dc)	-30 mA to +5.0 mA	-30 mA to +5.0 mA
Voltage Applied to Open Collector Outputs (Output HIGH)	-0.5 V to +10 V	-0.5 V to +5.5 V
High Level Voltage Applied to Disabled 3-State Output	5.5 V	5.5 V
Current Applied to Output in Low State (Max)	Twice Rated I _{OL}	Twice Rated I _{OL}

*Either input voltage limit or input current limit is sufficient to protect the inputs — Circuits with 5.5 V maximum limits are listed below.

Device types having inputs limited to 5.5 V are as follows:

- SN74LS242/243, SN74LS245 — Inputs connected to outputs.
- SN74LS640/641/642/645 — Inputs connected to outputs.
- SN74LS299/322A/323 — Certain Inputs.
- SN74LS151/251 — Multiplexer Inputs.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA BOOK

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply Current** — The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** — The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{IL} **Input LOW current** — The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{OH} **Output HIGH current.** The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** — The current flowing into an output which is in the LOW state.

I_{OS} **Output short-circuit current** — The current flowing out of an output which is in the HIGH state when that output is short circuit to ground (or other specified potential).

I_{OZH} **Output off current HIGH** — The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off current LOW** — The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES — All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, -10 V is greater than -1.0 V).

V_{CC} **Supply voltage** — The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IK(MAX)} **Input clamp diode voltage** — The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** — The range of input voltages recognized by the device as a logic HIGH.

V_{IH(MIN)} **Minimum input HIGH voltage** — The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** — The range of input voltages recognized by the device as a logic LOW.

V_{IL(MAX)} **Maximum input LOW voltage** — The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

V_{OH(MIN)} **Output HIGH voltage** — The minimum guaranteed voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

V_{OL(MAX)} **Output LOW voltage** — The maximum guaranteed voltage at an output terminal sinking the maximum specified load current I_{OL}.

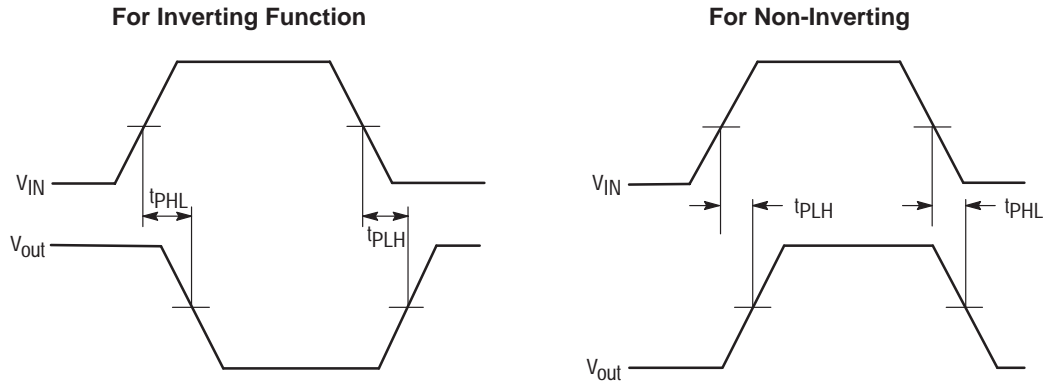
V_{T+} **Positive-going threshold voltage** — The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below V_{T-(MIN)}.

V_{T-} **Negative-going threshold voltage** — The input voltage of a variable threshold device (*i.e.*, Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above V_{T+(MAX)}.

AC SWITCHING PARAMETERS AND WAVEFORMS

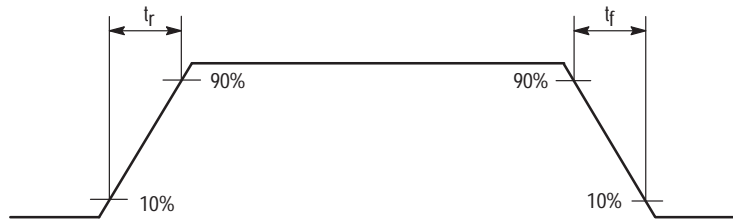
t_{PLH} **LOW-TO-HIGH propagation delay time :**
 The time delay between specified reference points, typically 1.3 V for LS and 1.5 V for FAST, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **HIGH-TO-LOW propagation delay time:**
 The time delay between specified reference points, typically 1.3 V for LS and 1.5 V for FAST, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.



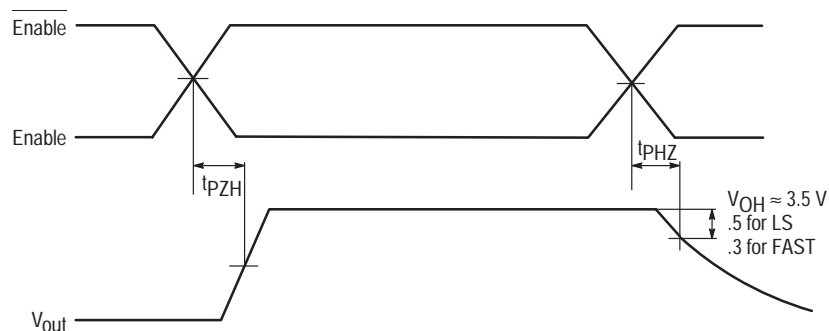
t_r **Waveform Rise Time:**
 LOW to HIGH logic transition time, measured from the 10% to 90% points of the waveform.

t_f **Waveform Fall Time:**
 HIGH to LOW logic transition time, measured the 90% to the 10% points of the waveform.



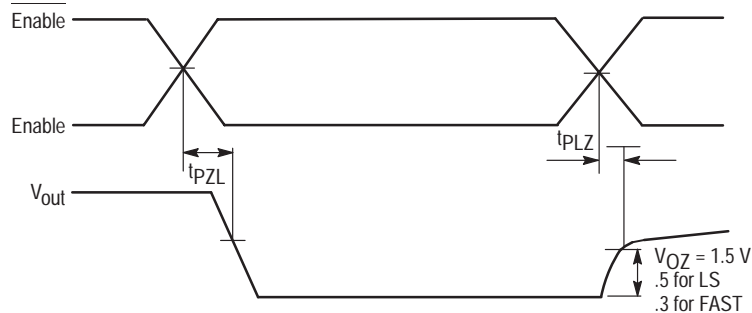
t_{PHZ} **Output disable time: HIGH to Z**
 The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined HIGH level to a high impedance (OFF) state. Reference point on the output voltage waveform is $V_{OH} - 0.5$ V for LS and $V_{OH} - 0.3$ V for FAST.

t_{PZH} **Output enable time: Z to HIGH**
 The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from a high impedance (OFF) state to a HIGH level.

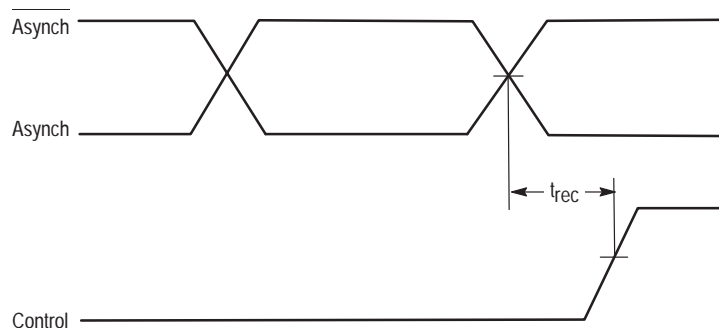


t_{PLZ} **Output disable time: LOW to Z**
 The time delay between the specified reference points on the input and output voltage waveforms, with the 3-state output changing from the defined LOW level to a high impedance (OFF) state. Reference point on the output voltage waveform is $V_{OL} + 0.5$ V for LS and $V_{OL} + 0.3$ V for FAST.

t_{PZL} **Output enable time: Z to LOW**
 The time delay between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance (OFF) state to a HIGH level.

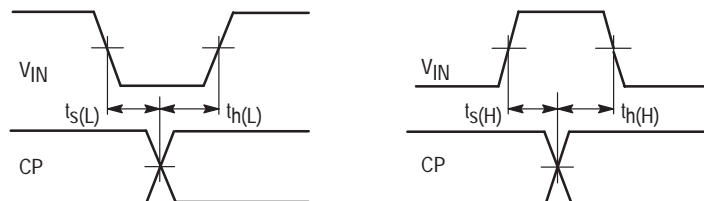


t_{rec} **Recovery time**
 Time required between an asynchronous signal (SET, RESET, CLEAR or PARALLEL load) and the active edge of a synchronous control signal, to insure that the device will properly respond to the synchronous signal.



t_h **Hold Time**
 The interval of time from the active edge of the control signal (usually the clock) to when the data to be recognized is no longer required to ensure proper interpretation of the data. A negative hold time indicates that the data may be removed at some time prior to the active edge of the control signal.

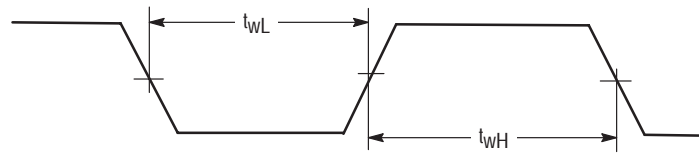
t_s **Setup time**
 The interval of time during which the data to be recognized is required to remain constant prior to the active edge of the control signal to ensure proper data recognition. A negative setup time indicates that data may be initiated sometime after the active transition of the timing pulse and still be recognized.



t_w or t_{pw}

Pulse width

The time between the specified amplitude points (1.3 V for LS and 1.5 V for FAST™) on the leading and trailing edges of a pulse.



f_{MAX}

Toggle frequency/operating frequency

The maximum rate at which clock pulses meeting the clock requirements (i.e., t_{wH} , t_{wL} , and t_r , t_f) may be applied to a sequential circuit. Above this frequency the device may cease to function.

f_{MAXmin}

Guaranteed maximum clock frequency

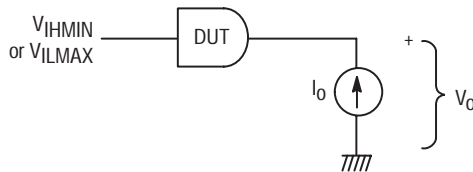
The lowest possible value for f_{MAX} .

TESTING

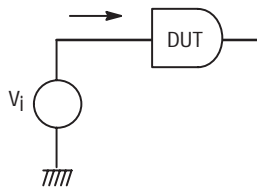
DC TEST CIRCUITS

The following test circuits and forcing functions represent Motorola's typical DC test procedures.

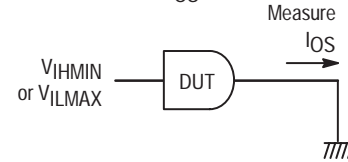
V_{OH} AND V_{OL} TESTS
Force I_{OHMAX} or I_{OLMAX}
Measure V_{OH} or V_{OL}



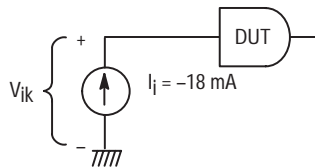
I_{IH} , I_{IH} AND I_{IL} TESTS
Force 7, 5.5, 2.7, or 0.4 V
Measure I_{IH} , I_{IH} , or I_{IL}



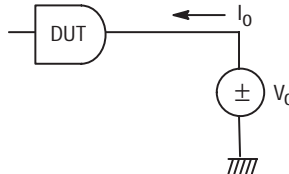
I_{OS} TEST



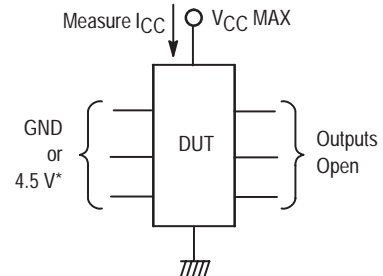
V_{IK} TEST
Force I_j
Measure V_{IK}



I_{OH} , I_{OZH} , and I_{OZL} TESTS
Force 5.5, 2.4, or 0.4 V
Measure I_o



I_{CC} TEST



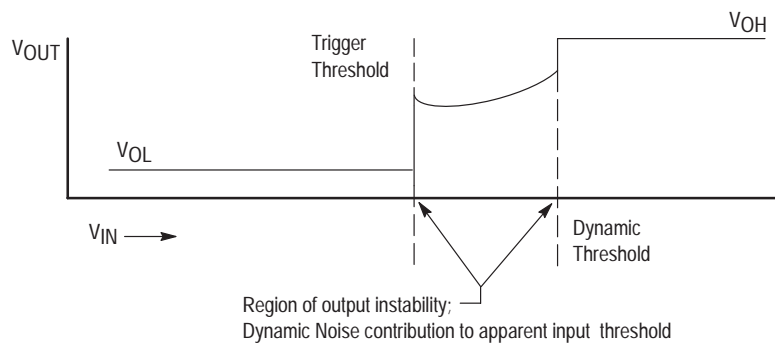
*Unless otherwise indicated, input conditions are selected to produce a worst case condition.

AC TEST CIRCUITS. The following test circuits and conditions represent Motorola's typical test procedures. AC waveforms and terminology can be found on pages 3-8 to 3-10.

Proper testing requires that care be taken in the construction of AC test fixtures. This is especially true of FAST™ TTL. Maintaining a 50 Ω environment on the ac test fixture, as well as the use of multilayer boards with internal V_{CC} and ground planes is highly recommended for FAST™ TTL. Bypassing with both electrolytic and high quality RF type capacitors should be provided on the board. Lead lengths for all components should be kept as short as possible (Motorola uses and recommends chip capacitors and resistors for ac test fixtures). Following these rules will result in cleaner waveforms as well as better correlation between Motorola and the FAST™ TTL consumer.

FUNCTIONAL TESTING OF TTL IN A NOISY ENVIRONMENT/"DYNAMIC" THRESHOLD

Testing noise (noise generated by the test system itself and noise generated by TTL devices under test interacting with the test system) adds to, or subtracts from the threshold voltage applied to the TTL device under test. For this reason Motorola does not recommend functional testing of TTL devices using threshold levels of 0.8 V and 2.0 V. Instead, good TTL testing techniques call for hard levels of less than 0.5 V V_{IL} and greater than 2.4 V V_{IH} to be applied for functional testing. Input threshold voltages should be tested separately, and only (for noise reasons above) after setting the device state with a hard level.



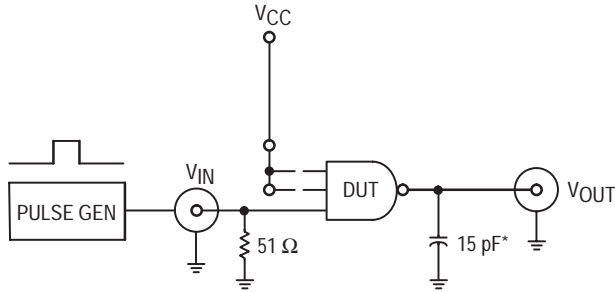
The V_{IN} versus V_{OUT} plot shows the practical effect of testing noise on a logic IC device. The actual device *Trigger threshold* is represented by the initial low to high output transition. The device will oscillate if the input voltage does not exceed the trigger threshold plus the noise generated by the interaction of the test system or given application with the device.

The *Dynamic threshold* (that creates Quiescent outputs), is the input logic level required to overcome the interactive DYNAMIC NOISE generated by a device switching states. The amount of interactive DYNAMIC NOISE can be characterized by the difference between the Trigger threshold and the Dynamic threshold of the device under test. A simple number cannot be assigned to this parameter as it is heavily dependent on any given application or test environment.

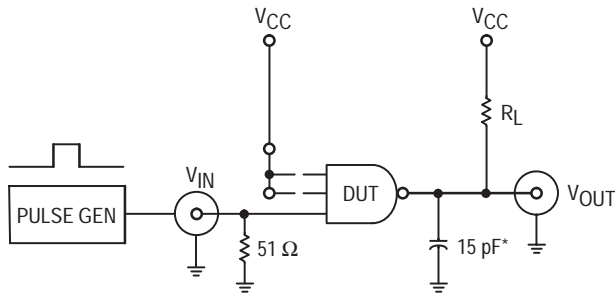
So although the Trigger threshold of any given device will correlate well between any test system, the correlation of "Dynamic" threshold cannot be made directly and will have meaning only in a relative sense.

LS TEST CIRCUITS

Test Circuit for Standard Output Devices

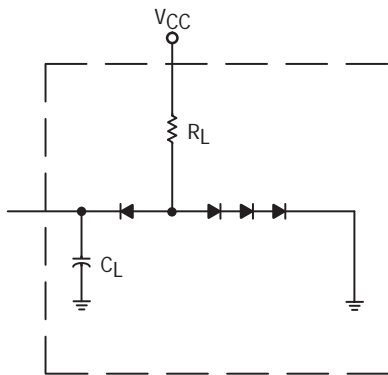


Test Circuit for Open Collector Output Devices



*includes all probe and jig capacitance

Optional LS Load (Guaranteed—Not Tested)

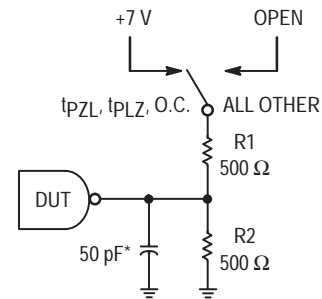


PULSE GENERATOR SETTINGS (UNLESS OTHERWISE SPECIFIED)

	LS	FAST
Frequency =	1 MHz	1 MHz
Duty Cycle =	50%	50%
1 TLH (t_r) =	6 ns (15)*	2.5 ns
1 THL (t_f) =	6 ns (15)*	2.5 ns
Amplitude =	0 to 3 V	0 to 3 V

*The specified propagation delay limits can be guaranteed with a 15 ns input rise time on all parameters except those requiring narrow pulse widths. Any frequency measurement over 15 MHz or pulse width less than 30 ns must be performed with a 6 ns input rise time.

FAST TEST CIRCUITS



*includes all probe and jig capacitance

APPLICATIONS ASSISTANCE FORM

In the event that you have any questions or concerns about the performance of any Motorola device listed in this catalog, please contact your local Motorola sales office or the Motorola Help line for assistance. If further information is required, you can request direct factory assistance.

Please fill out as much of the form as is possible if you are contacting Motorola for assistance or are sending devices back to Motorola for analysis. Your information can greatly improve the accuracy of analysis and can dramatically improve the correlation response and resolution time.

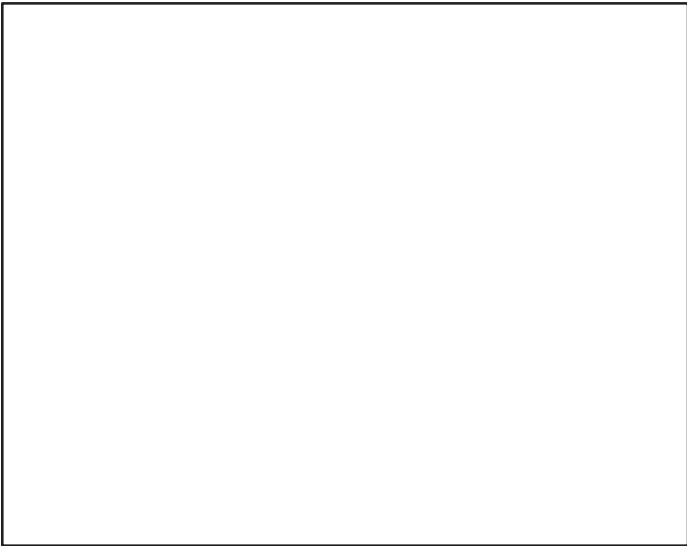
Items 4 thru 8 of the following form contains important questions that can be invaluable in analyzing application or device problems. It can be used as a self-help diagnostic guideline or for a baseline of information gathering to begin a dialog with Motorola representatives.

MOTOROLA Device Correlation/Component Analysis Request Form

— Please fill out entire form and return with devices to MOTOROLA INC., R&QA DEPT., 2200 W. Broadway, Mesa, AZ 85202.

- 1) Name of Person Requesting Correlation: _____
Phone No: _____ Job Title: _____ Company: _____
- 2) Alternate Contact: _____ Phone/Position: _____
- 3) Device Type (user part number): _____
- 4) Industry Generic Device Type: _____
- 5) # of devices tested/sampled: _____
of devices in question*: _____
returned for correlation: _____
* In the event of 100% failure, does Customer have other date codes of Motorola devices that pass inspection?
Yes _____ No _____ Please specify passing date code(s) if applicable _____
If none, does customer have viable alternate vendor(s) for device type?
Yes _____ No _____ Alternate vendor's name _____
- 6) Date code(s) and Serial Number(s) of devices returned for correlation — If possible, please provide one or two "good" units (Motorola's and/or other vendor) for comparison: _____
- 7) Describe USER process that device(s) are questionable in:
____ Incoming component inspection {test system = ?}: _____
____ Design prototyping: _____
____ Board test/burn-in: _____
____ Other (please describe): _____
- 8) Please describe the device correlation operating parameters as completely as possible for device(s) in question:
> Describe all pin conditions (e.g. floating, high, low, under test, stimulated but not under test, whatever ...), including any input or output loading conditions (resistors, caps, clamps, driving devices or devices being driven ...). Potentially critical information includes:
____ Input waveform timing relationships
____ Input edge rates
____ Input Overshoot or Undershoot — Magnitude and Duration
____ Output Overshoot or Undershoot — Magnitude and Duration
> Photographs, plots or sketches of relevant inputs and outputs with voltages and time divisions clearly identified for all waveforms are greatly desirable.
> V_{CC} and Ground waveforms should be carefully described as these characteristics vary greatly between applications and test systems. Dynamic characteristics of Ground and V_{CC} during device switching can dramatically effect input and internal operating levels. Ground & V_{CC} measurements should be made as physically close to the device in question as possible.
> Are there specific circumstances that seem to make the questionable unit(s) worse? Better?
____ Temperature _____
____ V_{CC} _____
____ Input rise/fall time _____
____ Output loading (current/capacitance) _____
____ Others _____
> ATE functional data should include pattern with decoding key and critical parameters such as V_{CC}, input voltages, Func step rate, voltage expected, time to measure.

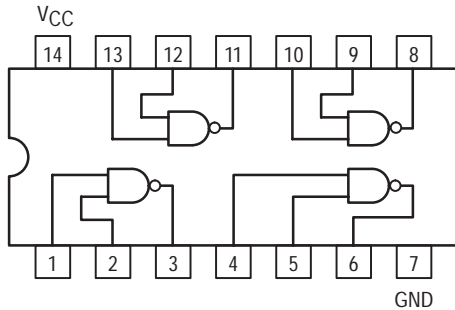
FAST AND LS TTL





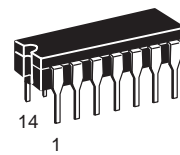
MOTOROLA

QUAD 2-INPUT NAND GATE

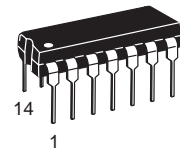


MC54/74F00

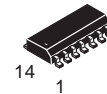
QUAD 2-INPUT NAND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 632-08



N SUFFIX
 PLASTIC
 CASE 646-06



D SUFFIX
 SOIC
 CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
 MC74FXXN Plastic
 MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			2.8	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			10.2	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

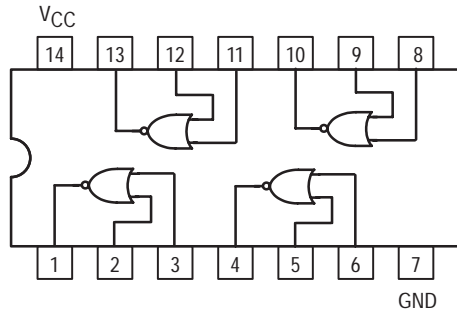
AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t _{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns



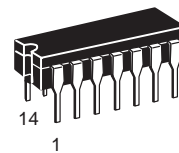
MOTOROLA

QUAD 2-INPUT NOR GATE

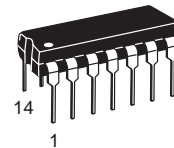


MC54/74F02

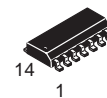
QUAD 2-INPUT NOR GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F02

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			5.6	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			13	mA	V _{CC} = MAX, V _{IN} = Note 3

NOTES:

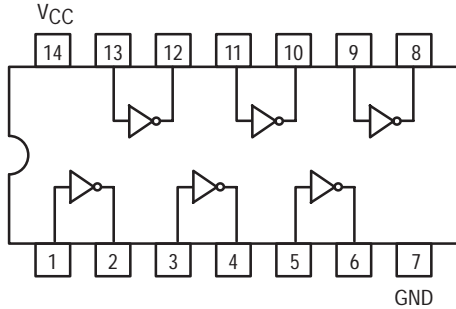
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.
3. Measured with one input high, one input low for each gate.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	5.5	2.5	7.5	2.5	6.5	ns
t _{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

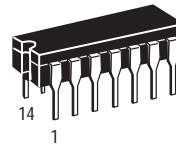


HEX INVERTER

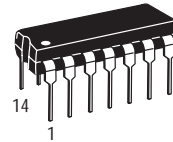


MC54/74F04

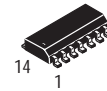
**HEX INVERTER
FAST™ SCHOTTKY TTL**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F04

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			4.2	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			15.3	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

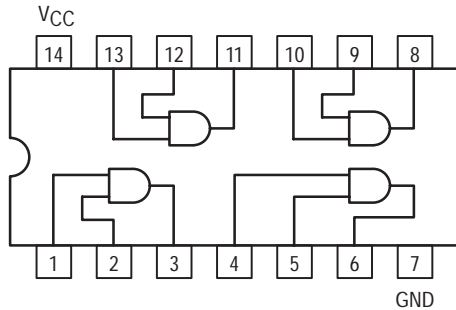
AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	MAX	
t _{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t _{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns



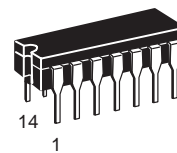
MOTOROLA

QUAD 2-INPUT AND GATE

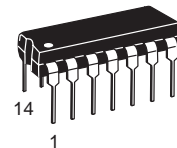


MC54/74F08

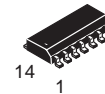
QUAD 2-INPUT AND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F08

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			8.3	mA	V _{CC} = MAX, V _{IN} = Open
	Total, Output LOW			12.9	mA	V _{CC} = MAX, V _{IN} = GND

NOTES:

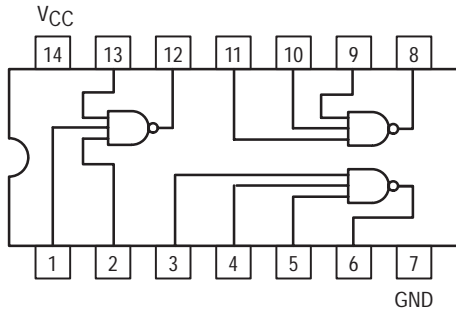
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
t _{PHL}	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.3	ns

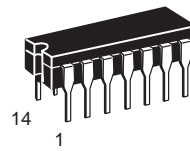


TRIPLE 3-INPUT NAND GATE

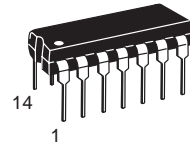


MC54/74F10

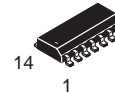
TRIPLE 3-INPUT NAND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F10

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			2.1	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			7.7	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

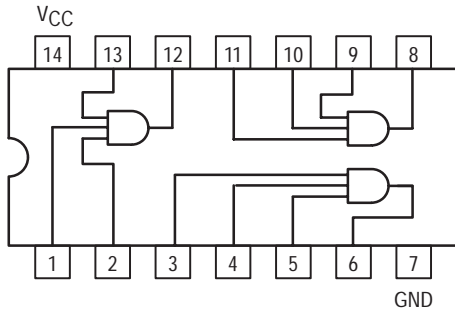
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t _{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns

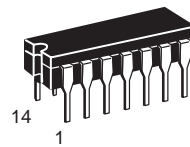


TRIPLE 3-INPUT AND GATE

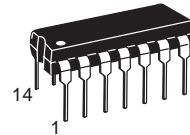


MC54/74F11

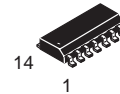
TRIPLE 3-INPUT AND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F11

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			6.2	mA	V _{CC} = MAX, V _{IN} = Open
	Total, Output LOW			9.7	mA	V _{CC} = MAX, V _{IN} = GND

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.6	2.5	7.5	3.0	6.6	ns
t _{PHL}	Propagation Delay	2.5	5.5	2.0	7.5	2.5	6.5	ns



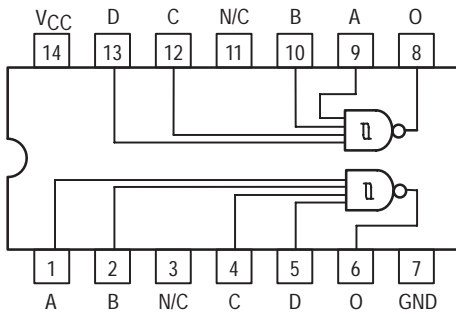
SCHMITT TRIGGERS DUAL 4-INPUT NAND/HEX INVERTERS

The MC54/74F13 and MC54/74F14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

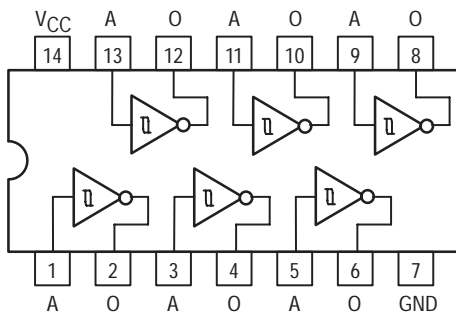
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAMS

MC54/74F13



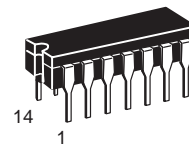
MC54/74F14



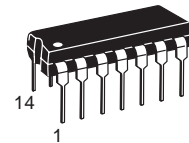
MC54/74F13
MC54/74F14

SCHMITT TRIGGERS
DUAL 4-INPUT
NAND/HEX INVERTERS

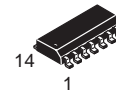
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F13 • MC54/74F14

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{T+}	Positive-Going Threshold Voltage		1.5		2.0	V	V _{CC} = 5.0 V	
V _{T-}	Negative-Going Threshold Voltage		0.7		1.1	V	V _{CC} = 5.0 V	
V _{T+} -V _{T-}	Hysteresis		0.4	0.8		V	V _{CC} = 5.0 V	
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74	2.5			V	I _{OH} = -1.0 mA	V _{CC} = 4.5
		74	2.7			V	I _{OH} = -1.0 mA	V _{CC} = 4.75
V _{OL}	Output LOW Voltage				0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{T+}	Input Current at Positive-Going Threshold			-0.14		mA	V _{CC} = 5.0 V, V _{IN} = V _{T+}	
I _{T-}	Input Current at Negative-Going Threshold			-0.18		mA	V _{CC} = 5.0 V, V _{IN} = V _{T-}	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CCH}	Power Supply Current Total, Output HIGH	F13		4.5	8.5	mA	V _{CC} = MAX	
		F14		13	22			
I _{CCL}	Power Supply Current Total, Output LOW	F13		7.0	10			
		F14		23	32			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (C_L = 50 pF)

Symbol	Parameter		54/74F		54F		74F		Unit
			T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to 70°C		
			V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	F13	3.5	7.0	3.5	9.0	3.5	8.0	ns
t _{PHL}			3.0	8.0	3.0	9.5	3.0	8.5	
t _{PLH}	Propagation Delay	F14	3.5	7.0	3.5	9.0	3.5	8.0	ns
t _{PHL}			3.0	6.5	3.0	8.0	3.0	7.0	

MC54/74F13 • MC54/74F14

FUNCTION TABLE MC54/74F13

Inputs				Output
A	B	C	D	O
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

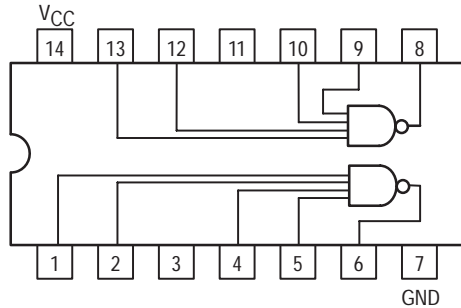
X = Don't Care

FUNCTION TABLE MC54/74F14

Input	Output
A	O
L	H
H	L

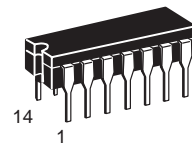


DUAL 4-INPUT NAND GATE

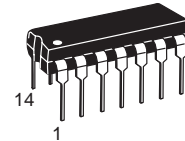


MC54/74F20

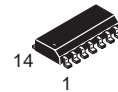
DUAL 4-INPUT NAND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F20

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			1.4	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			5.1	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

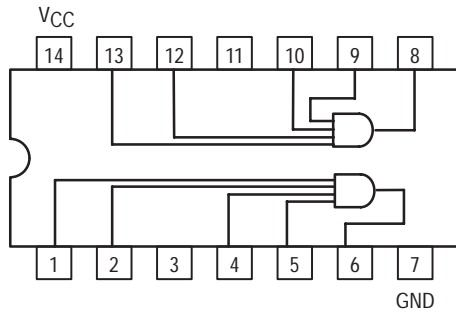
Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to 70°C		
		V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
		C _L = 50 pF		C _L = 50 pF		C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.4	5.0	2.0	7.0	2.4	6.0	ns
t _{PHL}	Propagation Delay	1.5	4.3	1.5	6.5	1.5	5.3	ns



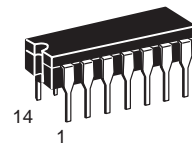
DUAL 4-INPUT AND GATE

MC54/74F21

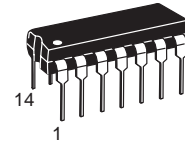
CONNECTION DIAGRAM



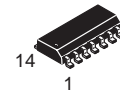
DUAL 4-INPUT AND GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F21

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			4.1	mA	V _{CC} = MAX, V _{IN} = Open
	Total, Output LOW			6.4	mA	V _{CC} = MAX, V _{IN} = GND

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

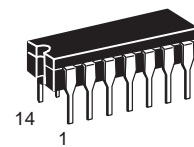
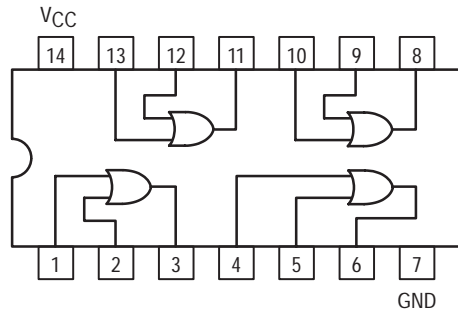
Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.0	5.6	2.0	7.5	2.0	6.6	ns
t _{PHL}	Propagation Delay	2.5	5.3	2.0	7.5	2.5	6.3	ns



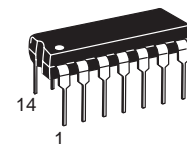
QUAD 2-INPUT OR GATE

MC54/74F32

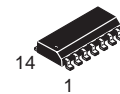
QUAD 2-INPUT OR GATE
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F32

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			9.2	mA	V _{CC} = MAX, V _{IN} = 4.5 V
	Total, Output LOW			15.5	mA	V _{CC} = MAX, V _{IN} = GND

NOTES:

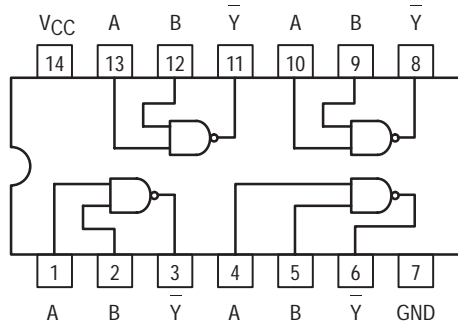
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to 70°C		
		V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
		C _L = 50 pF		C _L = 50 pF		C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.6	3.0	7.5	3.0	6.6	ns
t _{PHL}	Propagation Delay	3.0	5.3	2.5	7.5	3.0	6.3	ns

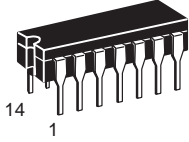


QUAD 2-INPUT NAND BUFFER

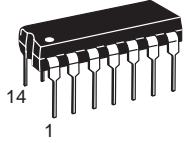


MC74F37

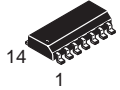
**QUAD 2-INPUT
NAND BUFFER**
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC74FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-15	mA
I _{OL}	Output Current — Low	74			64	mA

MC74F37

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74	2.0		V	I _{OH} = -15 mA V _{CC} = 4.50 V
		74	2.4		V	I _{OH} = -1.0 mA
		74	2.7		V	I _{OH} = -1.0 mA V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.55	V	I _{OL} = 64 mA V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-100		-225	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			6	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			33	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C		T _A = 0°C to 70°C		
		V _{CC} = +5.0 V C _L = 50 pF		V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.5	5.5	1.5	6.5	ns
t _{PHL}	Propagation Delay	1.0	4.5	1.0	5.0	ns

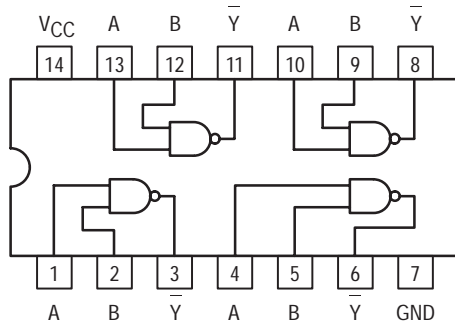
FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

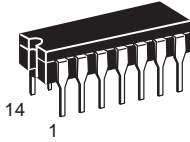


QUAD 2-INPUT NAND BUFFER, OPEN COLLECTOR

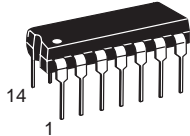


MC74F38

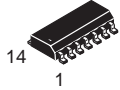
**QUAD 2-INPUT NAND BUFFER,
OPEN COLLECTOR**
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

MC74FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	74	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OL}	Output Current — Low	74			64	mA

MC74F38

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OL}	Output LOW Voltage			0.55	V	I _{OL} = 64 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OH}	Output HIGH Current			250	μA	V _{CC} = MIN, V _{IL} = MAX V _{IH} = MIN, V _{OH} = MAX
I _{CC}	Power Supply Current Total, Output HIGH			7.0	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			30	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C		T _A = 0°C to 70°C		
		Min	Max	Min	Max	
		V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		
		C _L = 50 pF		C _L = 50 pF		
t _{PLH}	Propagation Delay	7.5	12.5	7.5	13	ns
t _{PHL}	Propagation Delay	1.0	5.0	1.0	5.5	ns

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

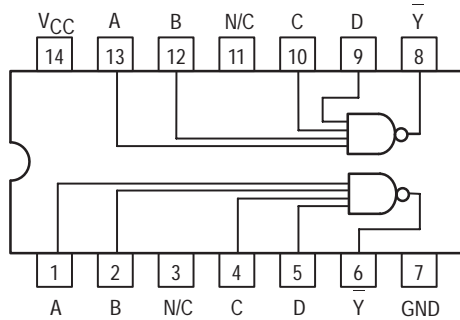
H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

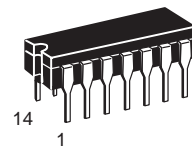


DUAL 4-INPUT NAND BUFFER

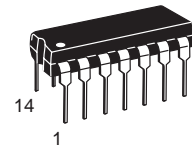


MC74F40

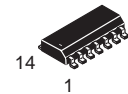
DUAL 4-INPUT NAND BUFFER
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC74FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	74	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-15	mA
I _{OL}	Output Current — Low	74			64	mA

MC74F40

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74	2.0		V	I _{OH} = -15 mA V _{CC} = 4.50 V
		74	2.4		V	I _{OH} = -1.0 mA
		74	2.7		V	I _{OH} = -1.0 mA V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.55	V	I _{OL} = 64 mA V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-100		-225	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			4	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			17	mA	V _{CC} = MAX, V _{IN} = Open

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C		T _A = 0°C to 70°C		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	V _{CC} = +5.0 V C _L = 50 pF		V _{CC} = 5.0 V ± 10% C _L = 50 pF		ns
t _{PHL}	Propagation Delay	1.5	6.0	1.5	7.0	ns
		1.0	5.0	1.0	5.5	ns

FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

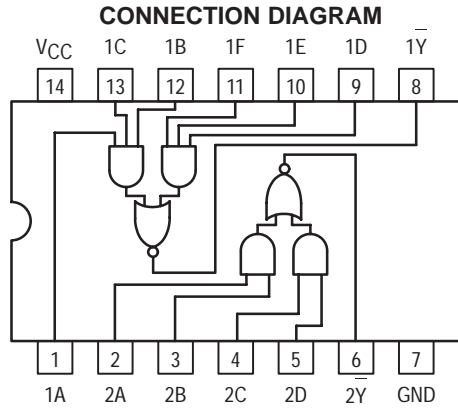
H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care



DUAL 2-WIDE 2-INPUT, 2-WIDE 3-INPUT AND-OR-INVERT GATE

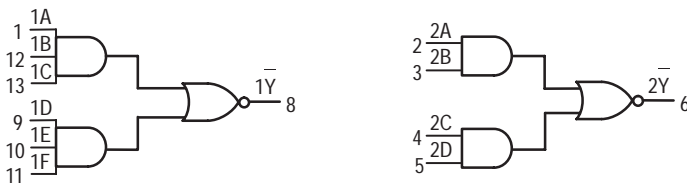


FUNCTION TABLE

For 3-Input Gates							For 2-Input Gates				
Inputs			Inputs			Output	Inputs				Output
A	B	C	D	E	F	1Y	A	B	C	D	2Y
H	H	H	X	X	X	L	H	H	X	X	L
X	X	X	H	H	H	L	X	X	H	H	L
All other combinations						H	All other combinations				H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

LOGIC SYMBOL



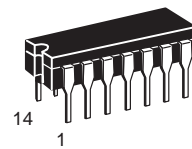
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

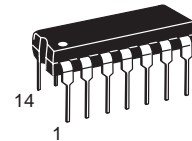
MC54/74F51

DUAL 2-WIDE 2-INPUT, 2-WIDE 3-INPUT AND-OR-INVERT GATE

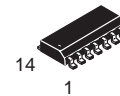
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 632-08



N SUFFIX
 PLASTIC
 CASE 646-06



D SUFFIX
 SOIC
 CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
 MC74FXXN Plastic
 MC74FXXD SOIC

MC54/74F51

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V	
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V	
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Total Supply Current	I _{CC} H	1.8	3.0	mA	V _{IN} = GND	V _{CC} = MAX
		I _{CC} L	5.5	7.5		V _{IN} = 4.5 V	

NOTES:

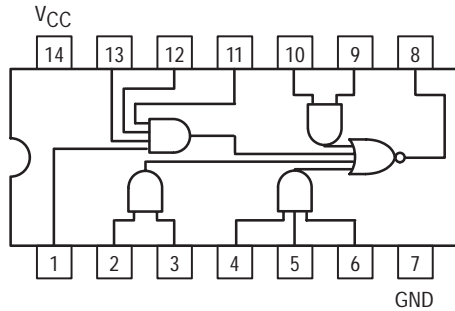
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.0		5.5	1.5	7.5	1.5	6.5	ns
t _{PHL}	A, B, C, D, E, F, to nY	1.0		4.0	1.0	5.5	1.0	4.5	

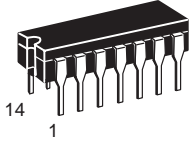


4-2-3-2-INPUT AND-OR-INVERT GATE

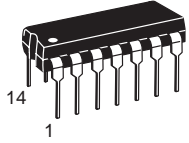


MC54/74F64

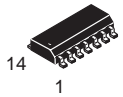
**4-2-3-2-INPUT
AND-OR-INVERT GATE
FAST™ SCHOTTKY TTL**



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F64

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH			2.8	mA	V _{CC} = MAX, V _{IN} = GND
	Total, Output LOW			4.7	mA	V _{CC} = MAX, V _{IN} = Note 3

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.
- I_{CC}L is measured with all inputs of one gate open and remaining inputs grounded.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	6.5	2.5	8.5	2.5	7.5	ns
t _{PHL}	Propagation Delay	1.5	4.5	1.5	6.5	1.5	5.5	ns

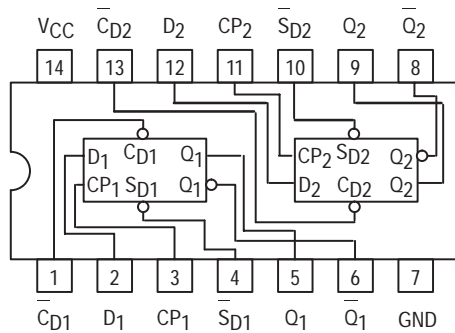


DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The MC54/74F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

- ESD > 4000 Volts

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Input	Outputs
@ t_n	@ $t_n + 1$
D	Q \bar{Q}
L	L H
H	H L

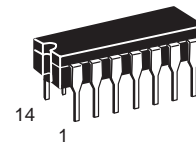
Asynchronous Inputs:

- LOW Input to \bar{S}_D sets Q to HIGH level
- LOW Input to \bar{C}_D sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

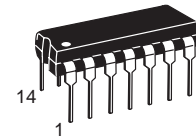
- H = HIGH Voltage Level
- L = LOW Voltage Level
- t_n = Bit time before clock pulse
- $t_n + 1$ = Bit time after clock pulse

MC54/74F74

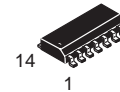
**DUAL D-TYPE POSITIVE
EDGE-TRIGGERED FLIP-FLOP**
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

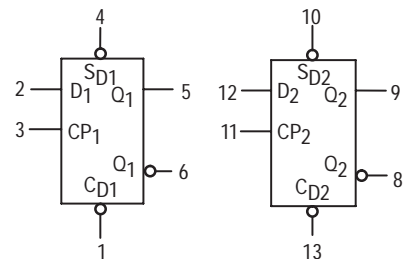


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

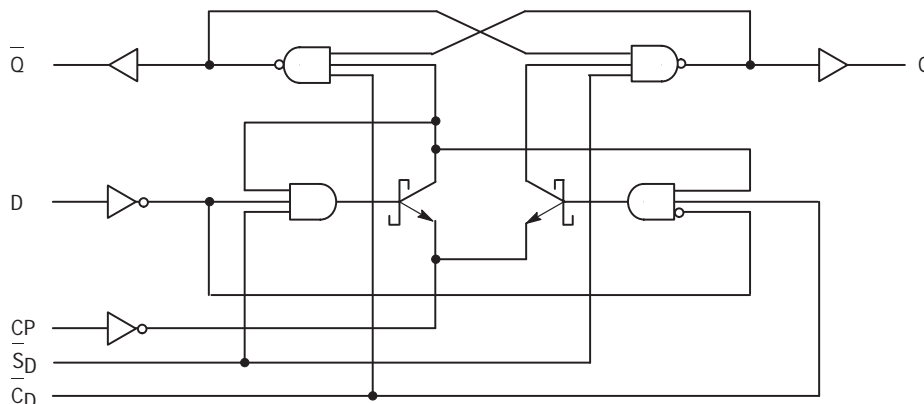
LOGIC SYMBOL



VCC = PIN 14
GND = PIN 7

MC54/74F74

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.50	5.0	5.50	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current (CP and D Inputs) (C _D and S _D Inputs)			-0.6	mA	V _{IN} = 0.5V	V _{CC} = MAX
				-1.8	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		10.5	16	mA	V _{CP} = 0 V	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F74

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100		100		100		MHz
t_{PLH}	Propagation Delay CP _n to Q _n or \overline{Q}_n	3.8	6.8	3.8	8.5	3.8	7.8	ns
t_{PHL}		4.4	8.0	4.4	10.5	4.4	9.2	
t_{PLH}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n	2.5	6.1	2.5	8.0	2.5	7.1	ns
t_{PHL}		3.5	9.0	3.5	11.5	3.5	10.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	2.0			3.0		2.0		ns
$t_{\text{S}}(\text{L})$	D _n to CP _n	3.0			4.0		3.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	1.0			2.0		1.0		
$t_{\text{H}}(\text{L})$	D _n to CP _n	1.0			2.0		1.0		ns
$t_{\text{W}}(\text{H})$	CP _n Pulse Width, HIGH	4.0			4.0		4.0		
$t_{\text{W}}(\text{L})$	or LOW	5.0			6.0		5.0		
$t_{\text{W}}(\text{L})$	\overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width, LOW	4.0			4.0		4.0		ns
t_{rec}	Recovery Time \overline{C}_{Dn} or \overline{S}_{Dn} to CP	2.0			3.0		2.0		ns

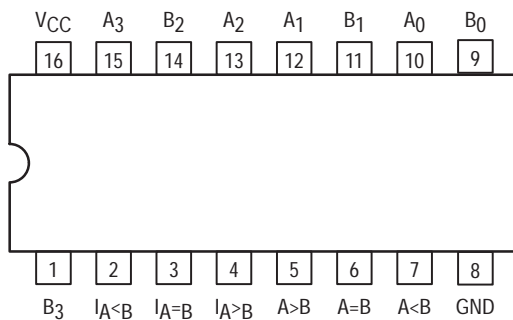


4-BIT MAGNITUDE COMPARATOR

The MC54/74F85 is a 4-Bit Magnitude Comparator which compares two 4-Bit words (A_0 - A_3 , B_0 - B_3), A_3 , B_3 being the most significant inputs. Operation is not restricted to binary codes; the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($0_A > B$), "A less than B" ($0_A < B$), "A equal to B" ($0_A = B$). Three Expander Inputs, $I_A > B$, $I_A < B$, $I_A = B$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_A < B = I_A > B = L$, $I_A = B = H$. For serial (ripple) expansion the $0_A > B$, $0_A < B$ Outputs are connected respectively to the $I_A > B$ and $I_A = B$ inputs of the next most significant comparator, as shown in Figure 1. Refer to applications section of data sheet for high speed method of comparing large words.

- High Impedance NPN Base Inputs for Reduced Loading (20 μ A in HIGH and LOW States)
- Magnitude Comparison of any Binary Words
- Serial or Parallel Expansion Without Extra Gating
- ESD > 4000 Volts

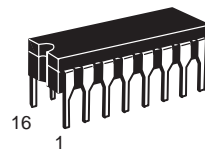
CONNECTION DIAGRAM



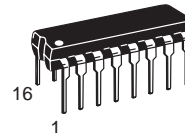
MC54/74F85

4-BIT MAGNITUDE COMPARATOR

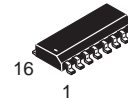
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXJ	Ceramic
MC74FXXN	Plastic
MC74FXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

MC54/74F85

FUNCTION TABLE

Comparing Inputs				Expansion Inputs			Outputs		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _A > B	I _A < B	I _A = B	A > B	A < B	A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

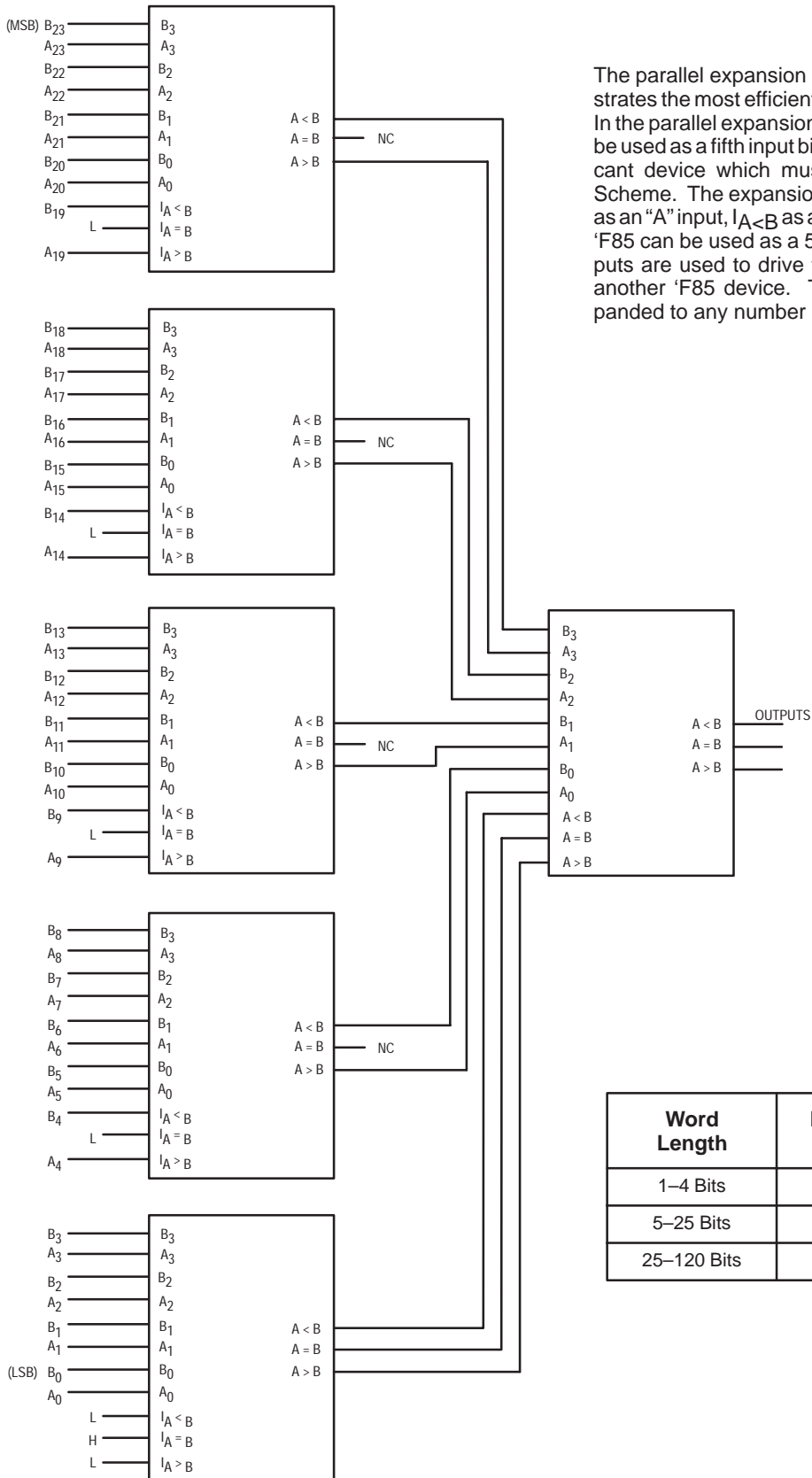
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA V _{CC} = 4.50 V
		74	2.7			
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = 0 V, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Total Supply Current				mA	V _{CC} = MAX
	HIGH V _{IN} = HIGH			50		
	LOW A _n = B _n = I _A -B = GND: I _A >B = I _A <B = 4.5 V			54		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F85



The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the Serial Scheme. The expansion inputs are used by labelling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ low. The 'F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A₀-A₃) and (B₀-B₃) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1

Word Length	Number of Packages	Typical Speeds 74F
1-4 Bits	1	12 ns
5-25 Bits	2-6	22 ns
25-120 Bits	8-31	34 ns

Figure 1. Comparison of Two 24-Bit Words

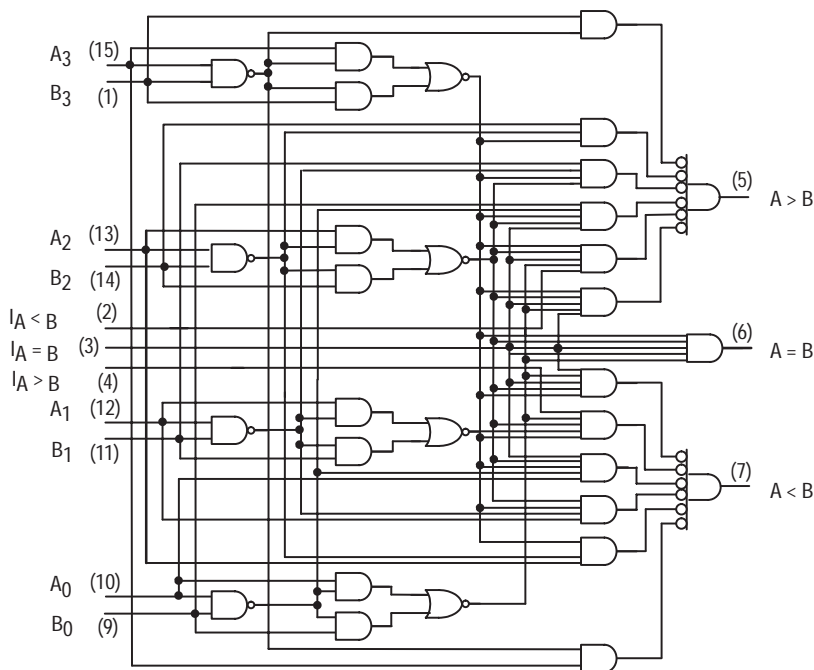
MC54/74F85

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	A or B Input to	6.0	11	5.5	14	5.5	13	ns
t_{PHL}	A < B, A > B Output	6.0	14	5.5	16.5	5.5	15.5	
t_{PLH}	A or B Input to	5.5	11.5	5.0	15	5.0	14	ns
t_{PHL}	A = B Output	7.0	14	6.5	15.5	6.5	14.5	
t_{PLH}	$I_{A<B}$ and $I_{A=B}$ Input	3.0	7.5	2.5	10	2.5	9.0	ns
t_{PHL}	to A > B Output	3.0	9.0	2.5	11	2.5	10	
t_{PLH}	$I_{A=B}$ Input to	2.5	7.0	2.0	10	2.0	9.0	ns
t_{PHL}	A = B Output	3.5	10	2.5	13	2.5	12	
t_{PLH}	$I_{A>B}$ and $I_{A=B}$ Input	3.0	8.0	3.0	10.5	3.0	9.5	ns
t_{PHL}	to A < B Output	3.0	9.0	2.0	10.5	2.0	9.5	

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B, and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15 ns

is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B} = \text{LOW}$, $I_{A=B} = \text{HIGH}$, and $I_{A<B} = \text{LOW}$.

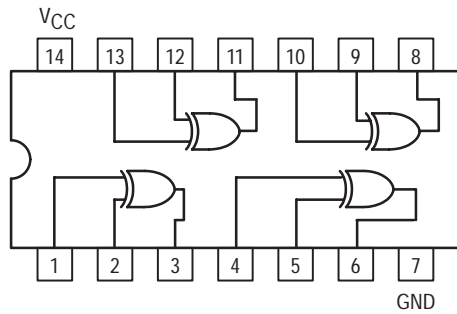


NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

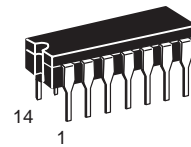


QUAD 2-INPUT EXCLUSIVE-OR GATE

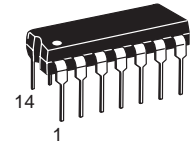


MC54/74F86

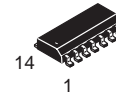
**QUAD 2-INPUT
EXCLUSIVE-OR GATE
FAST™ SCHOTTKY TTL**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

MC54FXXJ Ceramic
MC74FXXN Plastic
MC74FXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F86

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				100	μA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		15	23	mA	1-Input HIGH 1-Input LOW
			18	28		Inputs LOW

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

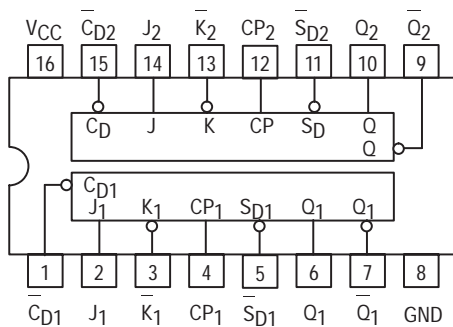
Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C			T _A = -55°C to +125°C		T _A = 0°C to 70°C		
		V _{CC} = +5.0 V			V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
		C _L = 50 pF			C _L = 50 pF		C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	4.0	5.5	2.5	7.0	3.0	6.5	ns
t _{PHL}	(Other Input LOW)	3.0	4.2	5.5	3.0	7.0	3.0	6.5	
t _{PLH}	Propagation Delay	3.5	5.3	7.0	3.5	8.5	3.5	8.0	ns
t _{PHL}	(Other Input HIGH)	3.0	4.7	6.5	3.0	8.0	3.0	7.5	



DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

The MC54/74F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to F74 data sheet) by connecting the J and K inputs together.

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Input		Output	
@ t_n		@ $t_n + 1$	
J	K	Q	Q
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

Asynchronous Inputs:

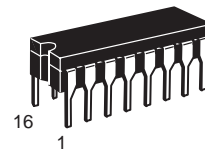
- LOW Input to \bar{S}_D sets Q to HIGH level
- LOW Input to \bar{C}_D sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
 t_n = Bit time before clock pulse
 $t_n + 1$ = Bit time after clock pulse

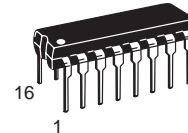
MC54/74F109

DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

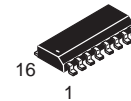
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

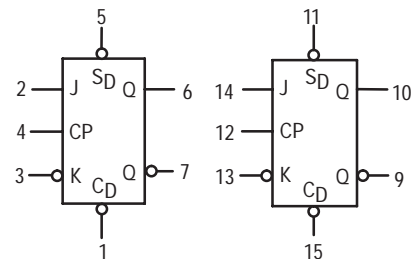


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

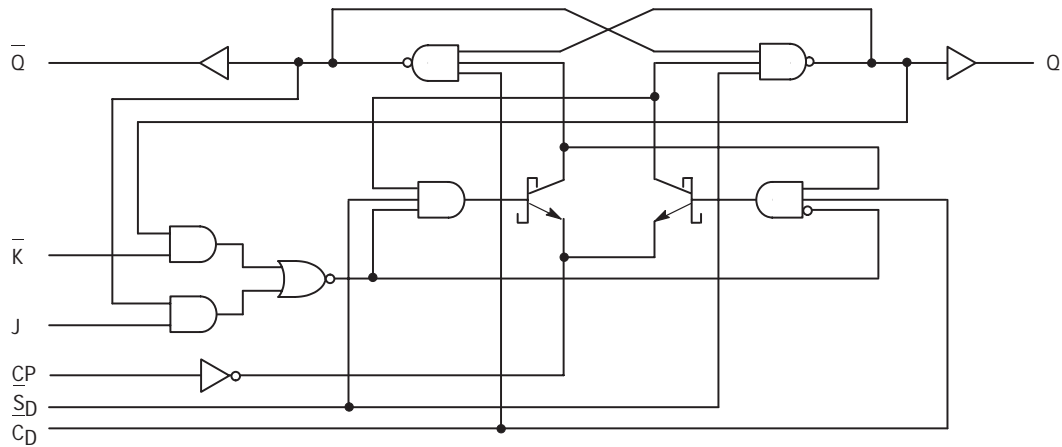
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MC54/74F109

LOGIC DIAGRAM (one half shown)



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current (J, K and CP Inputs) (\overline{C}_D and \overline{S}_D Inputs)			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
				-1.8	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		11.7	17	mA	V _{CP} = 0 V	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F109

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	125		70		90		MHz
t_{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	9.0	3.8	8.0	ns
t_{PHL}	\overline{CP}_n to Q_n or \overline{Q}_n	4.4	6.2	8.0	4.4	10.5	4.4	9.2	
t_{PLH}	Propagation Delay	2.5	5.2	7.0	2.5	9.0	2.5	8.0	ns
t_{PHL}	\overline{CD}_n or \overline{SD}_n to Q_n or \overline{Q}_n	3.5	7.0	9.0	3.5	11.5	3.5	10.5	

AC OPERATING REQUIREMENTS

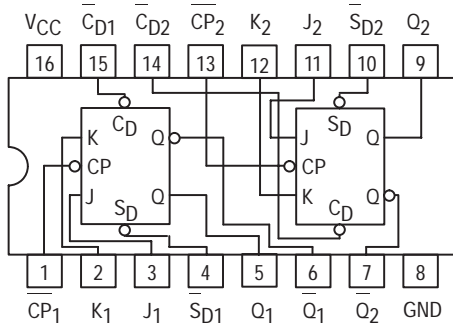
Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Typ	Max	Min	Max	Min	Max	
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
$t_{\text{S}}(\text{L})$	\overline{J}_n or \overline{K}_n to \overline{CP}_n	3.0			3.0		3.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	1.0			1.0		1.0		ns
$t_{\text{H}}(\text{L})$	\overline{J}_n or \overline{K}_n to \overline{CP}_n	1.0			1.0		1.0		
$t_{\text{W}}(\text{H})$	\overline{CP}_n Pulse Width, HIGH	4.0			4.0		4.0		ns
$t_{\text{W}}(\text{L})$	or LOW	5.0			5.0		5.0		
$t_{\text{W}}(\text{L})$	\overline{CD}_n or \overline{SD}_n Pulse Width, LOW	4.0			4.0		4.0		ns
t_{rec}	Recovery Time \overline{CD}_n or \overline{SD}_n to CP	2.0			2.0		2.0		ns



DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The MC74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S_D}$ or $\overline{C_D}$ prevents clocking and forces Q or Q HIGH, respectively. Simultaneous LOW signals on $\overline{S_D}$ and $\overline{C_D}$ force both Q and Q HIGH.

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Inputs		Output
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	\overline{Q}_n

Asynchronous Inputs:

- LOW Input to $\overline{S_D}$ sets Q to HIGH level
- LOW Input to $\overline{C_D}$ sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and \overline{Q} HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

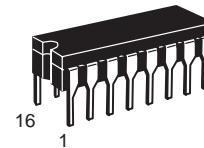
t_n = Bit time before clock pulse

$t_n + 1$ = Bit time after clock pulse

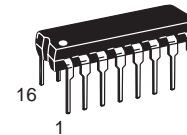
MC74F112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

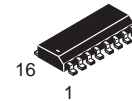
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

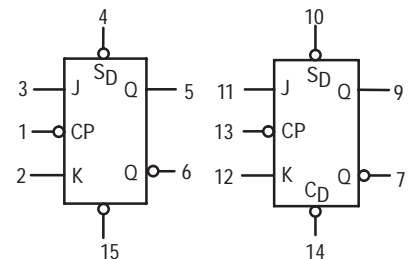


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

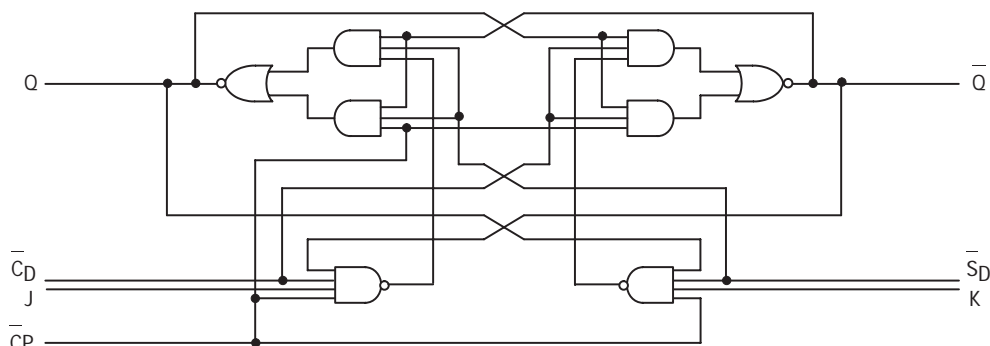
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MC74F112

LOGIC DIAGRAM (one half shown)



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				100	μA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current (J and K Inputs)			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
	(C _P Inputs)			-2.4	mA		
	(C _D and S _D Inputs)			-3.0	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Power Supply Current		12	19	mA	V _{CC} = MAX, V _{CP} = 0 V	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F112

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	110				MHz
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	2.0	6.5	2.0	7.5	ns
t _{PHL}		2.0	6.5	2.0	7.5	
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	2.0	6.5	2.0	7.5	ns
t _{PHL}		2.0	6.5	2.0	7.5	

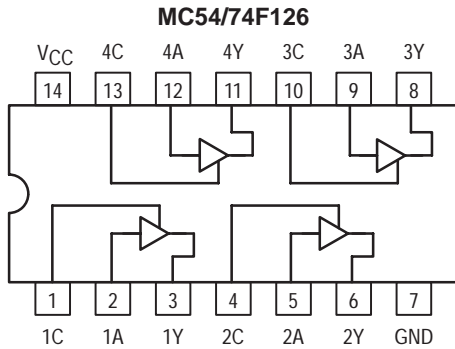
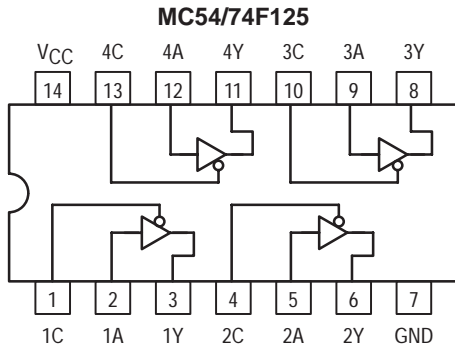
AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t _S (L)	J _n or K _n to CP _n	3.0			3.0		
t _H (H)	Hold Time, HIGH or LOW	0			0		ns
t _H (L)	J _n or K _n to CP _n	0			0		
t _W (H)	CP _n Pulse Width, HIGH	4.5			4.5		ns
t _W (L)	or LOW	4.5			4.5		
t _W (L)	C _{Dn} or S _{Dn} Pulse Width, LOW	4.5			4.5		ns
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to CP	4.0			5.0		ns



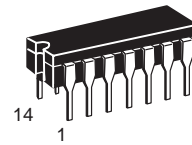
3-STATE QUAD BUFFERS

- High Impedance NPN Base Inputs for Reduced Loading

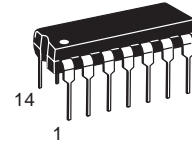


MC54/74F125
MC54/74F126

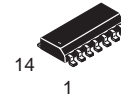
QUAD BUFFERS, 3-STATE
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-12	mA
		74			-15	
I _{OL}	Output Current — Low	54			48	mA
		74			64	

MC54/74F125 • MC54/74F126

Function Table MC54/74F125

Inputs		Output
C	A	Y
L	L	L
L	H	H
H	X	Z

Function Table MC54/74F126

Inputs		Output
C	A	Y
H	L	L
H	H	H
L	X	Z

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
Z = High Impedance (off)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54,74	2.4	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
		54	2.0		V	I _{OH} = -12 mA	V _{CC} = 4.50 V
		74	2.0		V	I _{OH} = -15 mA	
V _{OL}	Output LOW Voltage	54		0.55	V	I _{OL} = 48 mA	V _{CC} = MAX
		74		0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output Off Current LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	V _{CC} = 0 V
I _{IL}	Input LOW Current			-20	μA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current Note 2	-100		-225	mA	V _{OUT} = GND	V _{CC} = MAX
I _{CC}	F125	I _{CCH}		24	mA	V _{CC} = MAX	
		I _{CCL}		40			
		I _{CCZ}		35			
	F126	I _{CCH}		30			
		I _{CCL}		48			
		I _{CCZ}		39			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F125 • MC54/74F126

AC ELECTRICAL CHARACTERISTICS

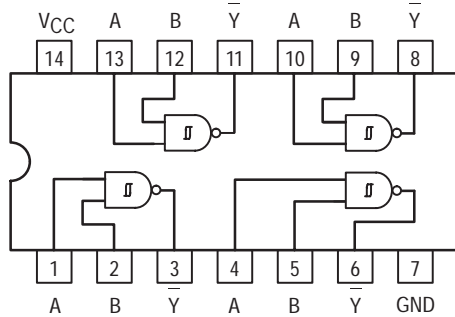
Symbol	Parameter		54/74F			54F		74F		Unit
			T _A = +25 °C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to + 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, nA to nY	F125	1.5	4.0	6.0	1.5	7.5	1.5	6.5	ns
t _{PHL}			3.0	5.5	7.5	3.0	9.0	3.0	8.0	
t _{PZH}	Output Enable Time to HIGH and LOW level		3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t _{PZL}			3.0	6.0	8.0	3.0	10	3.0	9.0	
t _{PHZ}	Output Disable Time from HIGH and LOW level		1.5	3.5	5.0	1.5	7.0	1.5	6.0	ns
t _{PLZ}			1.5	3.5	5.5	1.5	7.0	1.5	6.0	
t _{PLH}	Propagation Delay, nA to nY	F126	1.5	4.0	6.5	1.5	8.0	1.5	7.0	ns
t _{PHL}			3.0	5.5	8.0	3.0	9.5	3.0	8.5	
t _{PZH}	Output Enable Time to HIGH and LOW level		3.0	6.0	7.5	3.0	9.5	3.0	8.5	ns
t _{PZL}			3.0	6.0	8.0	3.0	9.5	3.0	8.5	
t _{PHZ}	Output Disable Time from HIGH and LOW level		2.0	4.5	6.5	2.0	8.5	2.0	7.5	ns
t _{PLZ}			3.0	5.5	7.5	3.0	9.0	3.0	8.0	



QUAD 2-INPUT NAND SCHMITT TRIGGER

The MC54/74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

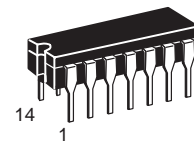
Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed up slow input transitions and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.



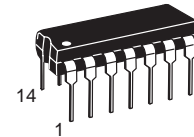
MC54/74F132

QUAD 2-INPUT NAND SCHMITT TRIGGER

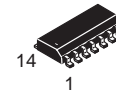
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54,74			-1.0	mA
I _{OL}	Output Current — Low	54,74			20	mA

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Voltage level
L = LOW voltage level

MC54/74F132

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{T+}	Positive-Going Threshold Voltage	1.5		2.0	V	$V_{CC} = 5.0\text{ V}$
V_{T-}	Negative-Going Threshold Voltage	0.7		1.1	V	$V_{CC} = 5.0\text{ V}$
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V	$V_{CC} = 5.0\text{ V}$
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{ mA}$
V_{OH}	Output HIGH Voltage	54,74	2.5		V	$I_{OH} = -1.0\text{ mA}$, $V_{CC} = 4.50\text{ V}$
		74	2.7		V	$I_{OH} = -1.0\text{ mA}$, $V_{CC} = 4.75\text{ V}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20\text{ mA}$, $V_{CC} = \text{MIN}$
I_{T+}	Input Current at Positive-Going Threshold		0		μA	$V_{CC} = 5.0\text{ V}$, $V_{IN} = V_{T+}$
I_{T-}	Input Current at Negative-Going Threshold		-350		μA	$V_{CC} = 5.0\text{ V}$, $V_{IN} = V_{T-}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0\text{ V}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5\text{ V}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0\text{ V}$
I_{CC}	Total, Supply Current	I_{CCH}	8.5	12	mA	$V_{IN} = \text{GND}$, $V_{CC} = \text{MAX}$
		I_{CCL}	13	19.5		$V_{IN} = 4.5\text{ V}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	3.5	5.5	7.0	3.5	9.0	3.5	8.0	ns
t_{PHL}	A, B to Y	3.0	5.0	6.5	3.0	8.0	3.0	7.0	

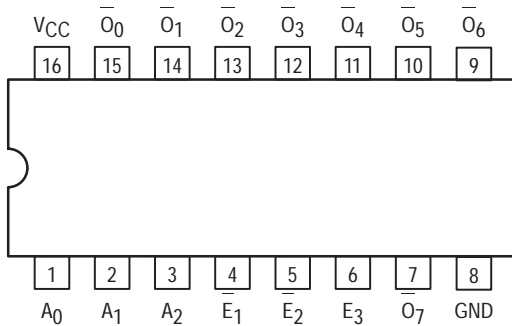


1-OF-8 DECODER/ DEMULTIPLEXER

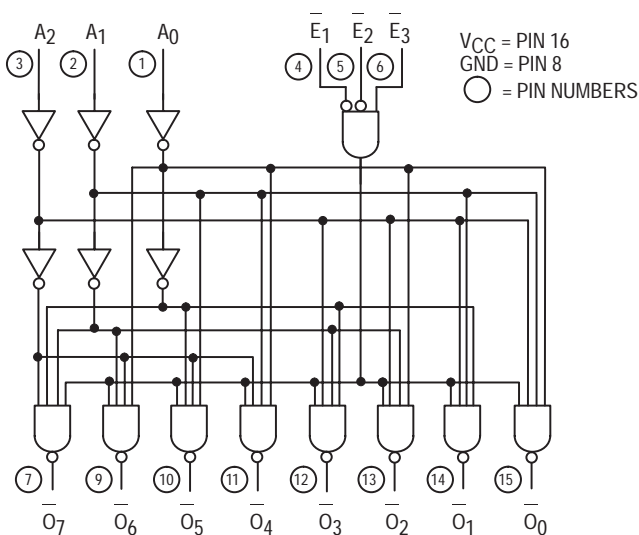
The MC54/74F138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three F138 devices or to a 1-of-32 decoder using four F138s and one inverter.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

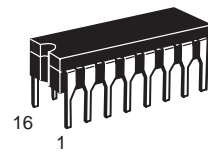


LOGIC DIAGRAM

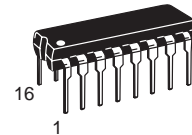


MC54/74F138

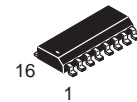
**1-OF-8 DECODER/
DEMULTIPLEXER**
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

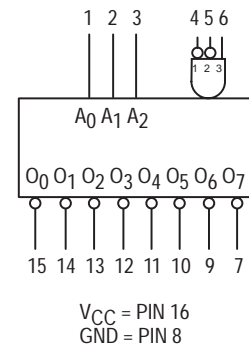


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



MC54/74F138

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			20	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	Levels of Delay	54/74F		54F		74F		Unit
			T _A = +25 °C V _{CC} = +5.0 V C _L = 50 pF		T _A = +25 °C to +125 °C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 °C to 70 °C V _{CC} = 5.0 V ±10% C _L = 50 pF		
			Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, Address to Output	3	3.0	7.5	3.0	12	3.0	8.5	ns
t _{PHL}			3.0	8.0	3.0	9.5	3.0	9.0	
t _{PLH}	Enable to Output	2	3.5	7.0	3.5	11	3.5	8.0	ns
t _{PHL}	\bar{E}_1 or \bar{E}_2		3.0	7.0	3.0	8.0	3.0	7.5	
t _{PLH}	Enable to Output	3	4.0	8.0	4.0	12.5	4.0	9.0	ns
t _{PHL}	E ₃		3.5	7.5	3.5	8.5	3.5	8.5	

FUNCTIONAL DESCRIPTION

The decoder accepts three binary weighted inputs (A₀, A₁, A₂) and when enabled provides eight mutually exclusive active LOW outputs (O₀–O₇). The F138 features three Enable inputs, two active LOW (\bar{E}_1 , \bar{E}_2) and one active HIGH (E₃). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E₃ is HIGH. This multiple enable function allows easy parallel

expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four F138s and one inverter.

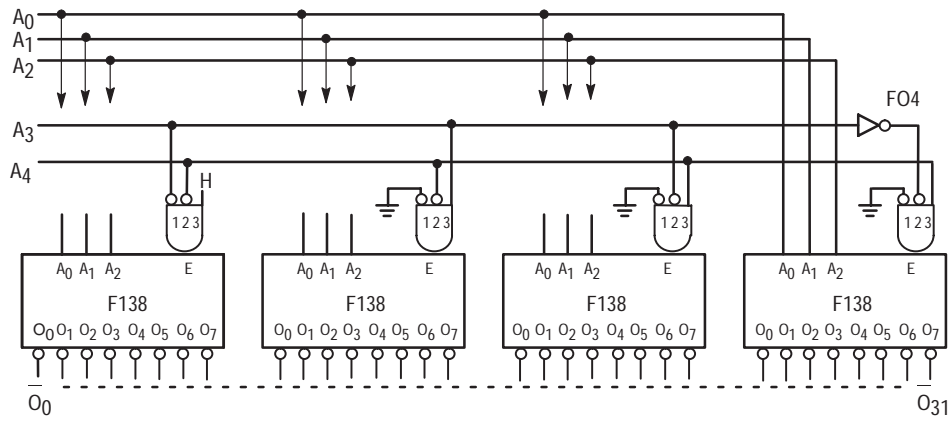
The F138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW states.

MC54/74F138

FUNCTION TABLE

Inputs						Outputs							
E ₁	E ₂	E ₃	A ₀	A ₁	A ₂	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

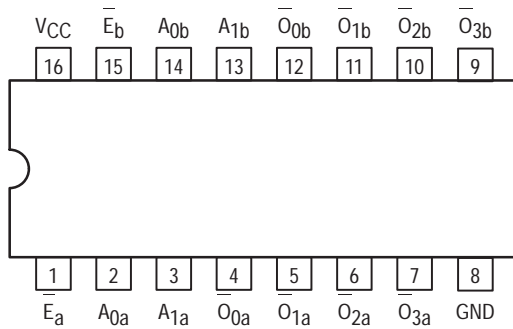


DUAL 1-OF-4 DECODER

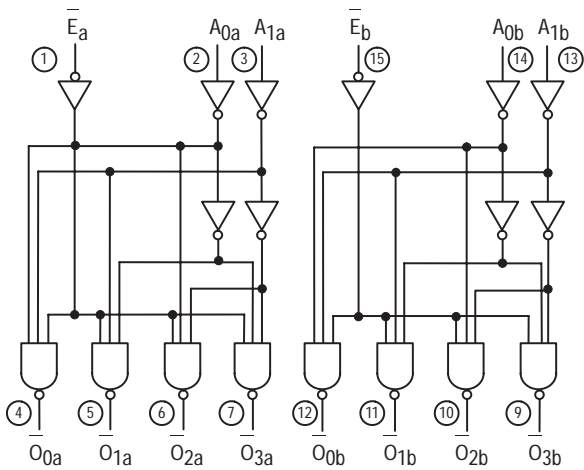
The MC54/74F139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the F139 can be used as a function generator providing all four miniterms of two variables.

- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM



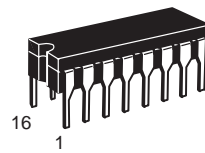
LOGIC DIAGRAM



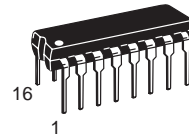
V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

MC54/74F139

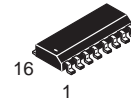
DUAL 1-OF-4 DECODER FAST™ SHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

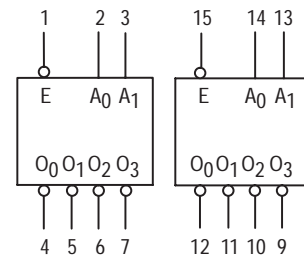


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



V_{CC} = Pin 16
 GND = Pin 8

MC54/74F139

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			20	mA	V _{CC} = MAX

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, Address to Output	3.5	7.0	2.5	12.0	3.0	8.5	ns
t _{PHL}	Enable to Output	3.5	8.0	3.5	9.5	3.5	9.0	
t _{PLH}	Propagation Delay, Address to Output	3.5	7.0	3.0	9.0	3.5	8.0	ns
t _{PHL}	Enable to Output	2.5	6.5	2.5	8.0	2.5	7.5	

FUNCTIONAL DESCRIPTION

The F139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accepts two binary weighted inputs (A₀, A₁) and provide four mutually exclusive active LOW outputs (O₀-O₃). Each decoder has an active LOW Enable (\bar{E}). When \bar{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the F139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure 1, and thereby reducing the number of packages required in a logic network.

MC54/74F139

FUNCTION TABLE

Inputs			Outputs			
\bar{E}	A_0	A_1	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

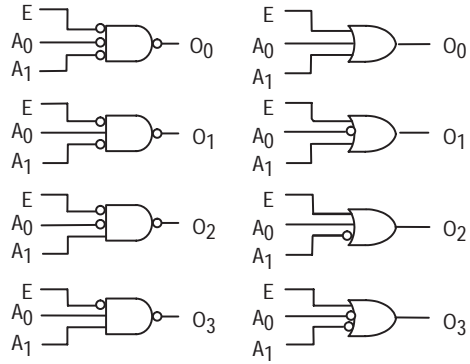


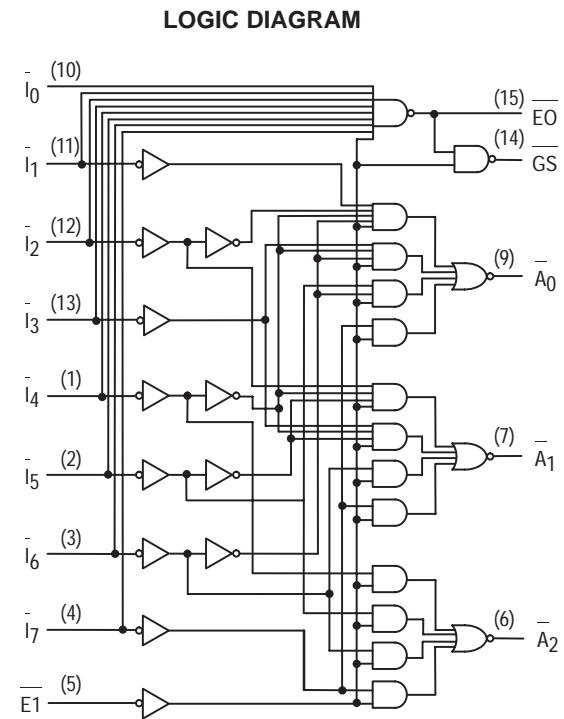
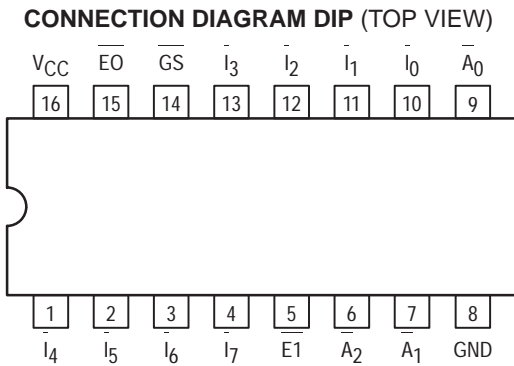
Figure 1.



8-LINE TO 3-LINE PRIORITY ENCODER

The MC54/74F148 provides three bits of binary coded output representing the position of the highest order active input, along with an output indicating the presence of any active input. It is easily expanded via input and output enables to provide priority encoding over many bits.

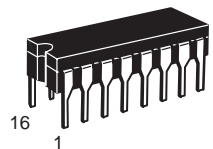
- Encodes Eight Data Lines in Priority
- Provides 3-Bit Binary Priority Code
- Input Enable Capability
- Signals When Data Present on Any Input
- Cascadable for Priority Encoding of n Bits



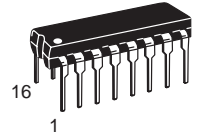
NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F148

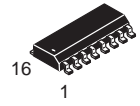
8-LINE TO 3-LINE PRIORITY ENCODER FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-08



N SUFFIX
PLASTIC
CASE 648-08

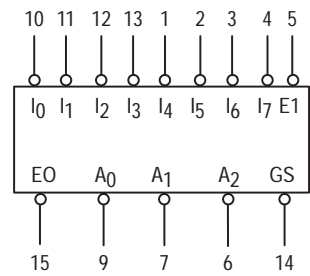


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MC54/74F148

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

FUNCTIONAL DESCRIPTION

The F148 8-input priority encoder accepts data from eight active LOW inputs (I₀–I₇) and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority. A HIGH on the Enable Input (E1) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing

erroneous information at the outputs. A Group Signal output (GS) and Enable Output (EO) are provided along with the three priority data outputs (A₂, A₁, A₀). GS is active LOW when any input is LOW; this indicates when any input is active. EO is active LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows cascading for priority encoding on any number of input signals. Both EO and GS are in the inactive HIGH state when the Enable Input is HIGH.

FUNCTION TABLE

Inputs									Outputs				
E1	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	GS	A ₀	A ₁	A ₂	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

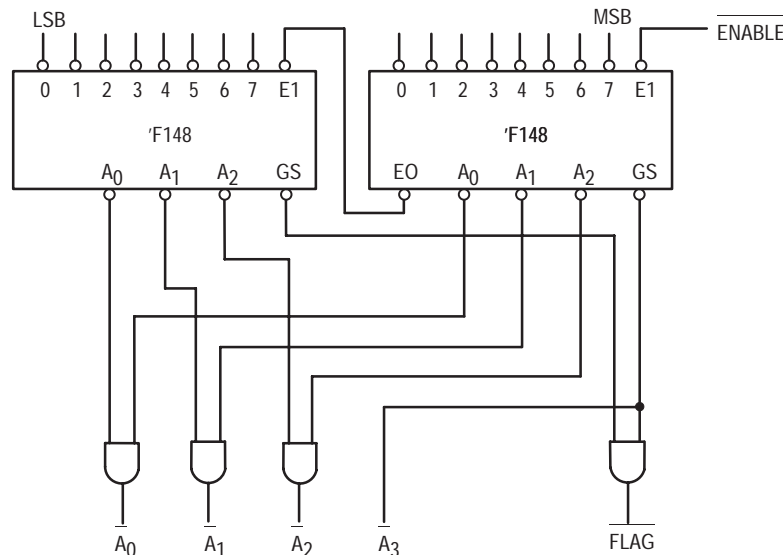


Figure 1. Application: 16-Input Priority Encoder

MC54/74F148

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				100	μA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	I ₀ , E1			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
	I ₁₋₁₇			-1.2	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Power Supply Current		23	35	mA	V _{CC} = MAX, V _{IN} = 4.5 V	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay \overline{I}_n to \overline{A}_n	3.5	7.0	9.0	3.5	11	3.5	10	ns
t _{PHL}	\overline{I}_n to \overline{A}_n	4.0	8.0	10.5	4.0	13	4.0	12	
t _{PLH}	Propagation Delay \overline{I}_n to \overline{EO}	2.5	5.0	6.5	2.5	8.5	2.5	7.5	ns
t _{PHL}	\overline{I}_n to \overline{EO}	2.0	5.5	7.5	2.0	9.5	2.0	8.5	
t _{PLH}	Propagation Delay \overline{I}_n to \overline{GS}	3.0	7.0	9.0	3.0	11	3.0	10	ns
t _{PHL}	\overline{I}_n to \overline{GS}	2.0	6.0	8.0	2.0	10	2.0	9.0	
t _{PLH}	Propagation Delay E1 to \overline{A}_n	3.5	6.5	8.5	3.5	10.5	3.5	9.5	ns
t _{PHL}	E1 to \overline{A}_n	3.0	6.0	8.0	3.0	10	3.0	9.0	
t _{PLH}	Propagation Delay E1 to \overline{GS}	2.5	5.0	7.0	2.5	9.0	2.5	8.0	ns
t _{PHL}	E1 to \overline{GS}	3.0	6.0	7.5	3.0	10	3.0	8.5	
t _{PLH}	Propagation Delay E1 to \overline{EO}	3.0	5.5	7.0	3.0	9.0	3.0	8.0	ns
t _{PHL}	E1 to \overline{EO}	4.5	8.0	10.5	4.5	13	4.5	12	



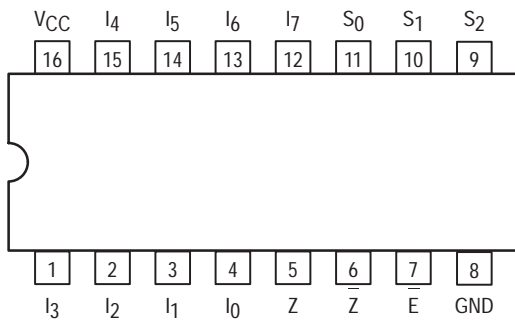
8-INPUT MULTIPLEXER

The MC54/74F151 is a high-speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The F151 can be used as a universal function generator to generate any logic function of four variables. Both asserted and negated outputs are provided.

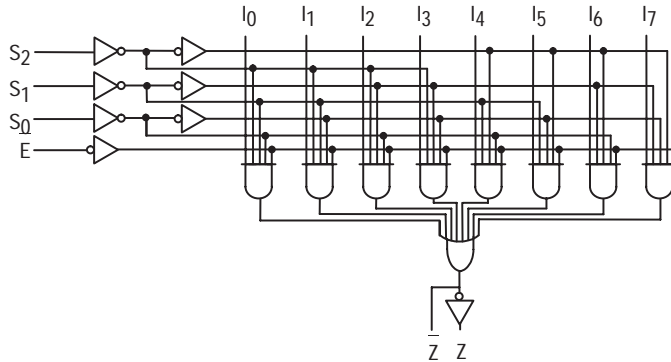
The F151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2 . The Enable input (E) is active LOW. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_3 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_4 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_5 \cdot S_0 \cdot S_1 \cdot S_2 + I_6 \cdot S_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



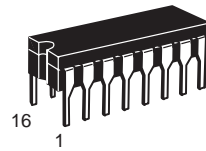
FUNCTION TABLE

Inputs				Outputs	
E	S ₂	S ₁	S ₀	Z	Z̄
H	X	X	X	I ₀	I ₀
L	L	L	L	I ₁	I ₁
L	L	L	H	I ₂	I ₂
L	L	H	L	I ₃	I ₃
L	L	H	H	I ₄	I ₄
L	H	L	L	I ₅	I ₅
L	H	L	H	I ₆	I ₆
L	H	H	L	I ₇	I ₇
L	H	H	H	I ₇	I ₇

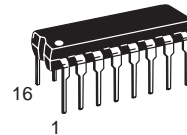
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

MC54/74F151

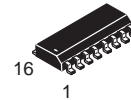
8-INPUT
MULTIPLEXER
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

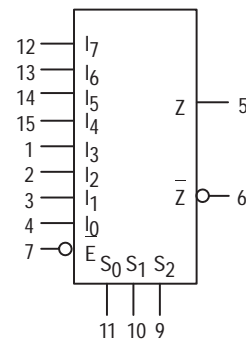


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MC54/74F151

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				100	μA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		13.5	21	mA	V _{CC} = MAX, V _{IN} = 4.5 V

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

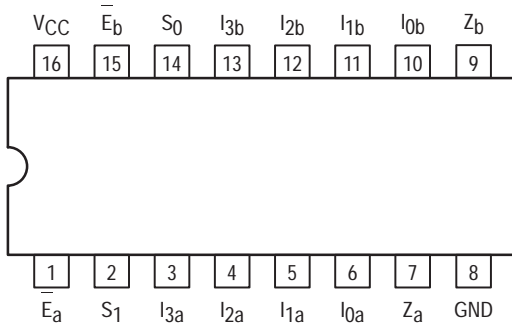
Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.0	8.0	3.5	10	3.5	9.0	ns
t _{PHL}	S _n to \bar{Z}	3.2	6.1	3.0	8.0	3.2	7.0	
t _{PLH}	Propagation Delay	4.5	13	3.0	17.5	4.0	14	ns
t _{PHL}	S _n to Z	4.5	9.0	4.0	11.5	4.0	10.5	
t _{PLH}	Propagation Delay	3.0	6.1	2.5	7.5	2.5	7.0	ns
t _{PHL}	\bar{E} to \bar{Z}	3.0	8.5	2.5	10.5	2.5	10	
t _{PLH}	Propagation Delay	5.0	9.5	3.0	14.5	4.0	11	ns
t _{PHL}	\bar{E} to Z	3.5	7.0	3.0	9.5	3.5	8.0	
t _{PLH}	Propagation Delay	2.5	5.7	2.5	7.5	2.5	6.5	ns
t _{PHL}	I _n to \bar{Z}	1.5	4.0	1.5	6.0	1.5	5.0	
t _{PLH}	Propagation Delay	3.0	9.5	2.5	11.5	2.5	11	ns
t _{PHL}	I _n to Z	3.0	6.5	3.0	8.0	3.0	7.5	



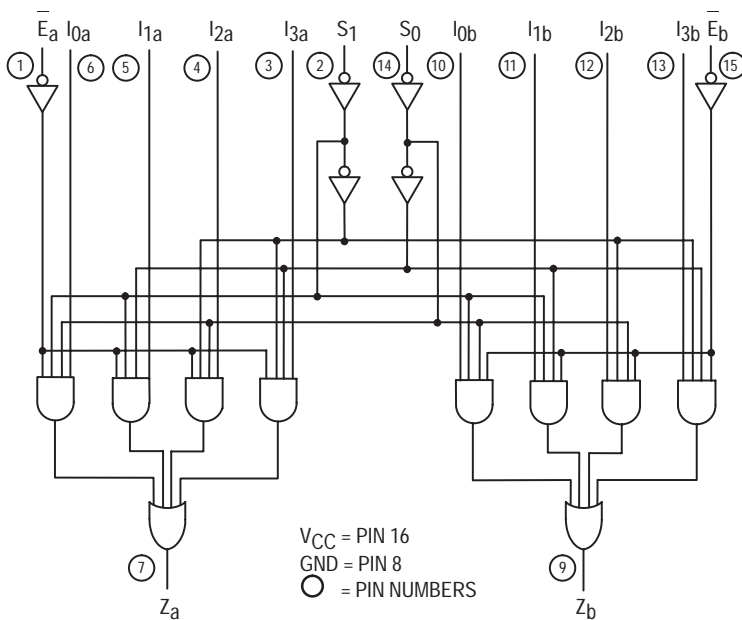
DUAL 4-INPUT MULTIPLEXER

The MC54/74F153 is a high-speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the F153 can generate any two functions of three variables.

CONNECTION DIAGRAM DIP (TOP VIEW)

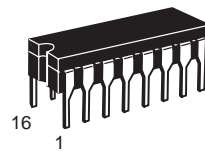


LOGIC DIAGRAM

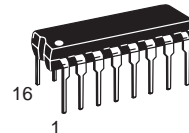


MC54/74F153

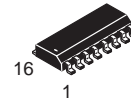
**DUAL 4-INPUT
 MULTIPLEXER**
FAST™ SHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08



D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F153

FUNCTIONAL DESCRIPTION

The MC54/74F153 is a Dual 4-Input Multiplexer. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active LOW Enables (E_a , E_b) which can be used to strobe the outputs independently. When the Enables (E_a , E_b) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW.

The F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is as a function generator. The F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

FUNCTION TABLE

Select Inputs		Inputs (a or b)					Output
S_0	S_1	\bar{E}	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18 \text{ mA}$, $V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5		V	$I_{OL} = -1.0 \text{ mA}$, $V_{CC} = 4.50 \text{ V}$
		74	2.7		V	$I_{OL} = -1.0 \text{ mA}$, $V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20 \text{ mA}$, $V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7 \text{ V}$, $V_{CC} = \text{MAX}$
				0.1	mA	$V_{IN} = 7.0 \text{ V}$, $V_{CC} = \text{MAX}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5 \text{ V}$, $V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0 \text{ V}$, $V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			20	mA	$V_{IN} = \text{GND}$, $V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F153

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.5	10.5	4.5	14	4.5	12	ns
t _{PHL}	S _n to Z _n	3.5	9.0	3.5	11	3.5	10.5	
t _{PLH}	Propagation Delay	4.5	9.0	4.5	11.5	4.5	10.5	ns
t _{PHL}	\bar{E}_n to Z _n	3.0	7.0	2.5	9.0	2.5	8.0	
t _{PLH}	Propagation Delay	3.0	7.0	2.5	9.0	3.0	8.0	ns
t _{PHL}	I _n to Z _n	3.0	6.5	2.5	8.0	2.5	7.5	

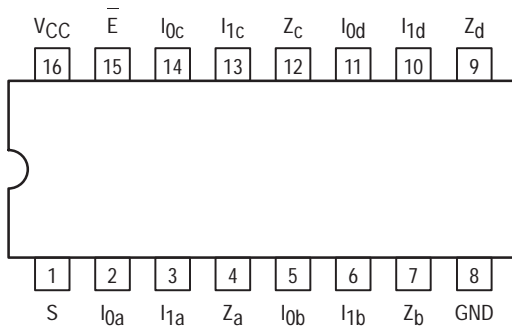


QUAD 2-INPUT MULTIPLEXER

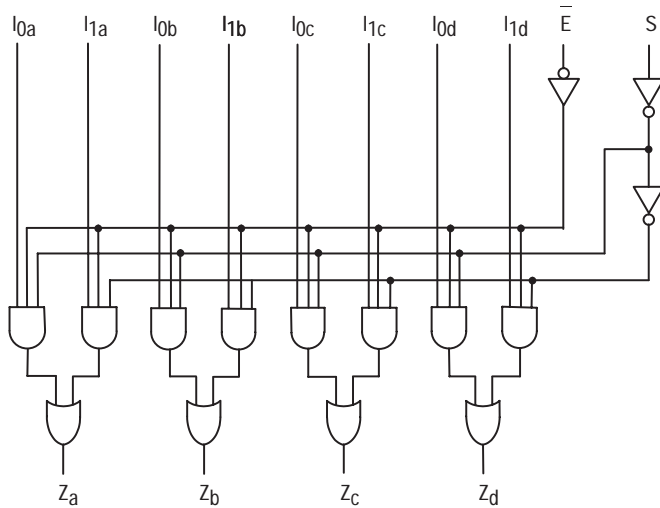
The MC74F157A is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The F157A can also be used to generate any four of the 16 different functions to two variables.

- AC Enhanced Version of the F157

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



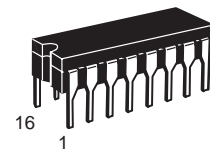
FUNCTION TABLE

Inputs				Output
E	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

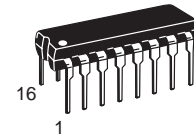
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

MC74F157A

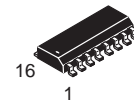
QUAD 2-INPUT MULTIPLEXER FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

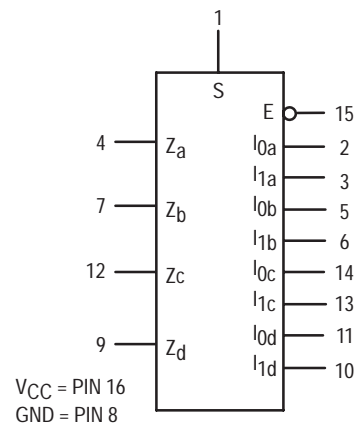


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC74F157A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
		74	2.5				V _{CC} = 4.50 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		15	23	mA	All Inputs = 4.5 V	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	10	3.5	11	ns
t _{PHL}	S to Z _n	3.0	7.0	3.0	8.0	
t _{PLH}	Propagation Delay	3.5	9.5	3.5	11	ns
t _{PHL}	\bar{E} to Z _n	2.5	6.5	2.5	7.0	
t _{PLH}	Propagation Delay	2.0	6.0	2.0	6.5	ns
t _{PHL}	I _n to Z _n	2.5	5.5	2.0	7.0	

FUNCTIONAL DESCRIPTION

The F157A is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The F157A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

A common use of the F157A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F157A can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

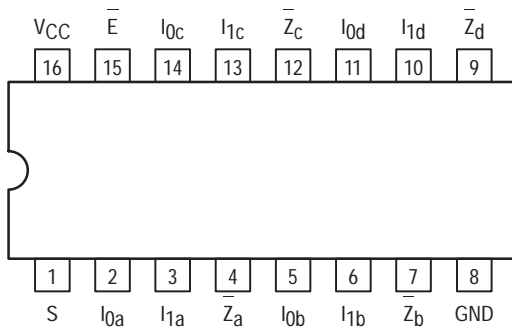


QUAD 2-INPUT MULTIPLEXER

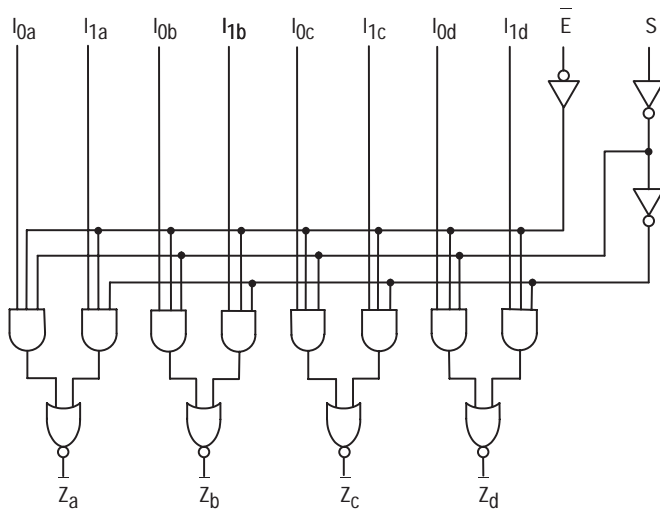
The MC74F158A is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The F158A can also generate any four of the 16 different functions of two variables.

- AC Enhanced Version of the F158

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM



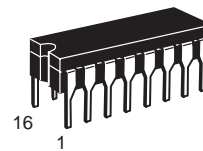
FUNCTION TABLE

Inputs				Output
\bar{E}	S	I_0	I_1	Z
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

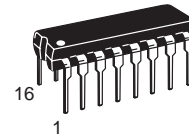
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

MC74F158A

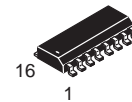
QUAD 2-INPUT MULTIPLEXER FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

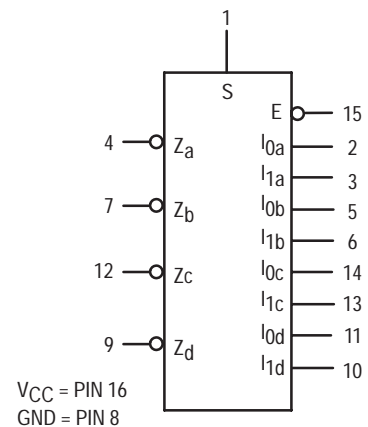


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC74F158A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
		74	2.5				V _{CC} = 4.50 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current (Note 3)		10	15	mA	V _{CC} = MAX, V _{IN} = HIGH	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.
- I_{CC} measured with outputs open and 4.5 V applied to all inputs.

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	8.5	3.0	9.5	ns
t _{PHL}	S to \bar{Z}	2.5	6.5	2.5	7.0	
t _{PLH}	Propagation Delay	2.5	6.0	2.5	7.0	ns
t _{PHL}	\bar{E} to \bar{Z}_n	2.0	6.0	2.0	6.5	
t _{PLH}	Propagation Delay	2.0	5.9	2.0	7.0	ns
t _{PHL}	I _n to \bar{Z}	1.0	4.0	1.0	4.5	

FUNCTIONAL DESCRIPTION

The F158A quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced HIGH regardless of all other inputs. The F158A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the F158A is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The F158A can generate four functions of two variables with one variable in common. This is useful for implementing gating functions.

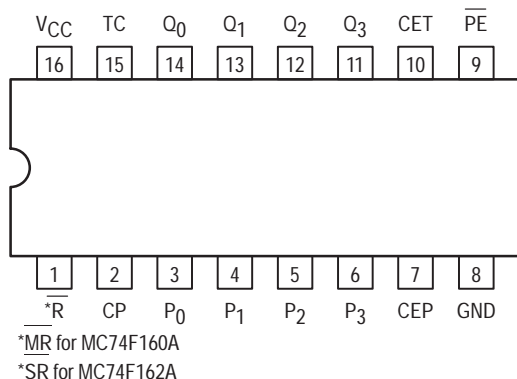


SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

The MC74F160A and MC74F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74F162A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz

CONNECTION DIAGRAM

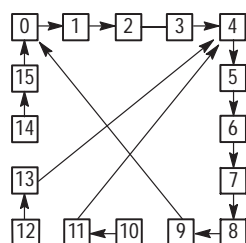


FUNCTION TABLE

SR	PE	CET	CEP	ACTION ON THE RISING CLOCK EDGE (\uparrow)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

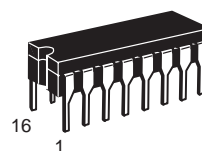
STATE DIAGRAM



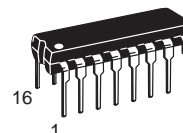
MC74F160A
MC74F162A

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

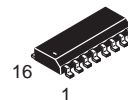
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

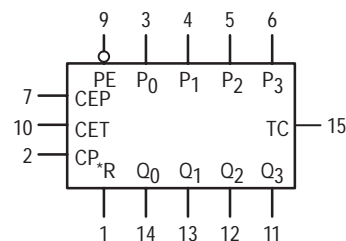


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXAJ Ceramic
MC74FXXXAN Plastic
MC74FXXXAD SOIC

LOGIC SYMBOL

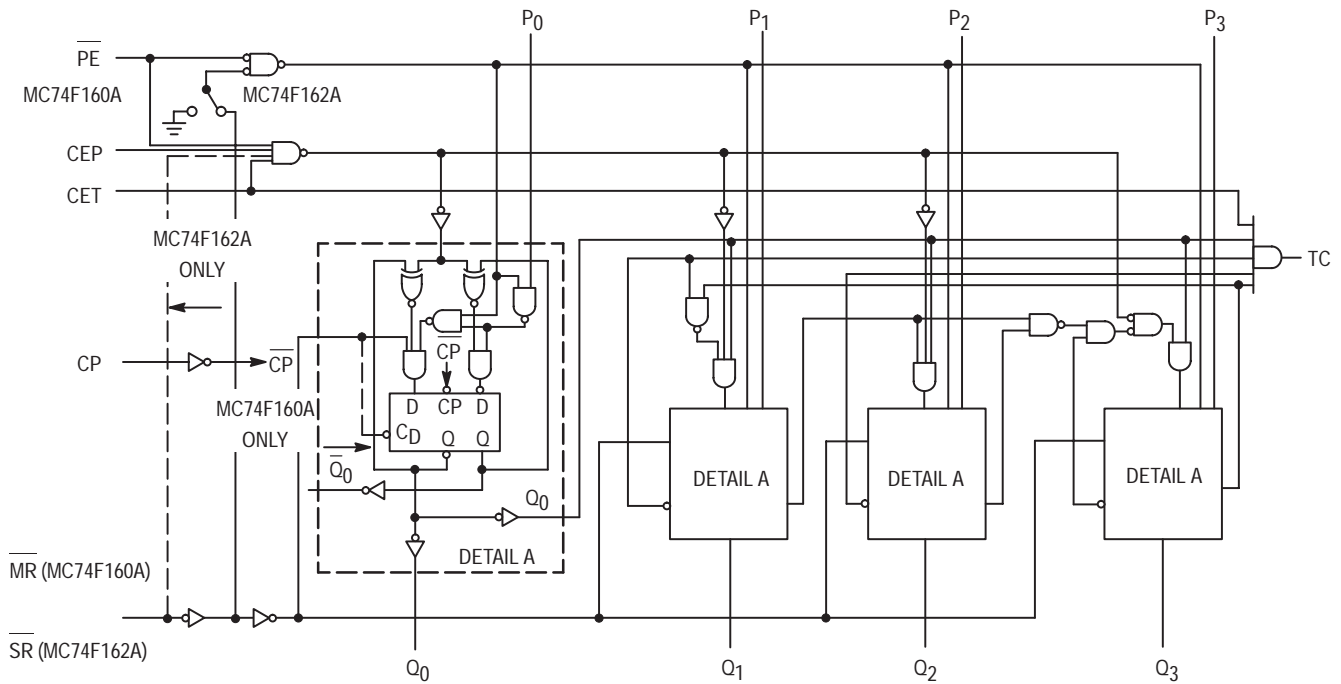


V_{CC} = PIN 16
GND = PIN 8

*MR for MC74F160A
*SR for MC74F162A

MC74F160A • MC74F162A

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74F160A and MC74F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus, all changes of the Q outputs (except due to Master Reset of the MC74F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC74F160A), synchronous reset (MC74F162A), parallel load, count-up and hold. Five control inputs — Master Reset (MR, MC74F160A), Synchronous Reset (SR, MC74F162A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Function Table. A LOW signal on

MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR (MC74F160A) or SR (MC74F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74F160A and MC74F162A use D-type edge-triggered flip-flops and changing the SR, PE, CEP, and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

MC74F160A • MC74F162A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74	2.5	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET, SR			-0.6 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		37	55	mA	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 9. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters, or registers. In the MC74F160A and

MC74F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations:

$$\text{Count Enable} = \overline{\text{CEP}} \cdot \text{CET} \cdot \overline{\text{PE}}$$

$$\text{TC} = \text{Q}_0 \cdot \text{Q}_1 \cdot \text{Q}_2 \cdot \text{Q}_3 \cdot \text{CET}$$

MC74F160A • MC74F162A

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}	Maximum Count Frequency	100		90		MHz
t _{PLH}	Propagation Delay, Count	3.5	7.5	3.5	8.5	ns
t _{PHL}	CP to Q _n (PE Input HIGH)	3.5	10	3.5	11	
t _{PLH}	Propagation Delay	3.5	8.5	3.5	9.5	ns
t _{PHL}	CP to Q _n (PE Input LOW)	4.0	8.5	4.0	9.5	
t _{PLH}	Propagation Delay	5.0	14	5.0	15	ns
t _{PHL}	CP to TC	4.5	14	4.5	15	
t _{PLH}	Propagation Delay	2.5	7.5	2.5	8.5	ns
t _{PHL}	CET to TC	2.5	7.5	2.5	8.5	
t _{PHL}	Propagation Delay MR to Q _n (MC74F160A)	5.5	12	5.5	13	ns
t _{PHL}	Propagation Delay MR to TC (MC74F160A)	4.5	10.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	5.0		5.0		ns
t _S (L)	P _n to CP	5.0		5.0		
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		ns
t _H (L)	P _n to CP	2.0		2.0		
t _S (H)	Setup Time, HIGH or LOW	11		11.5		ns
t _S (L)	PE or SR to CP	8.5		9.5		
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		ns
t _H (L)	PE or SR to CP	0		0		
t _S (H)	Setup Time, HIGH or LOW	11		11.5		ns
t _S (L)	CEP or CET to CP	5.0		5.0		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	CEP or CET to CP	0		0		
t _w (H)	Clock Pulse Width (Load)	5.0		5.0		ns
t _w (L)	HIGH or LOW	5.0		5.0		
t _w (H)	Clock Pulse Width (Count)	4.0		4.0		ns
t _w (L)	HIGH or LOW	6.0		7.0		
t _w (L)	MR Pulse Width, LOW (MC74F160A)	5.0		5.0		ns
t _{rec}	Recovery Time, MR to CP (MC74F160A)	6.0		6.0		

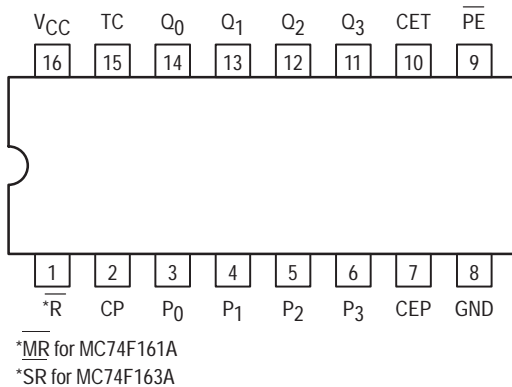


SYNCHRONOUS PRESETTABLE BINARY COUNTER

The MC74F161A and MC74F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74F161A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Frequency of 120 MHz

CONNECTION DIAGRAM

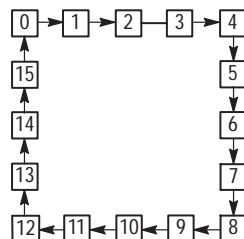


FUNCTION TABLE

SR	PE	CET	CEP	ACTION ON THE RISING CLOCK EDGE (\uparrow)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

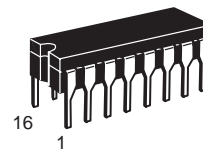
H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

STATE DIAGRAM

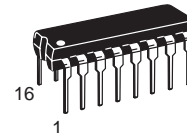


MC74F161A
MC74F163A

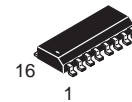
SYNCHRONOUS PRESETTABLE BINARY COUNTER
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

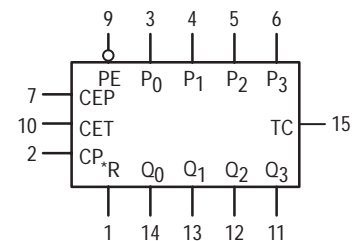


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXAJ Ceramic
MC74FXXXAN Plastic
MC74FXXXAD SOIC

LOGIC SYMBOL

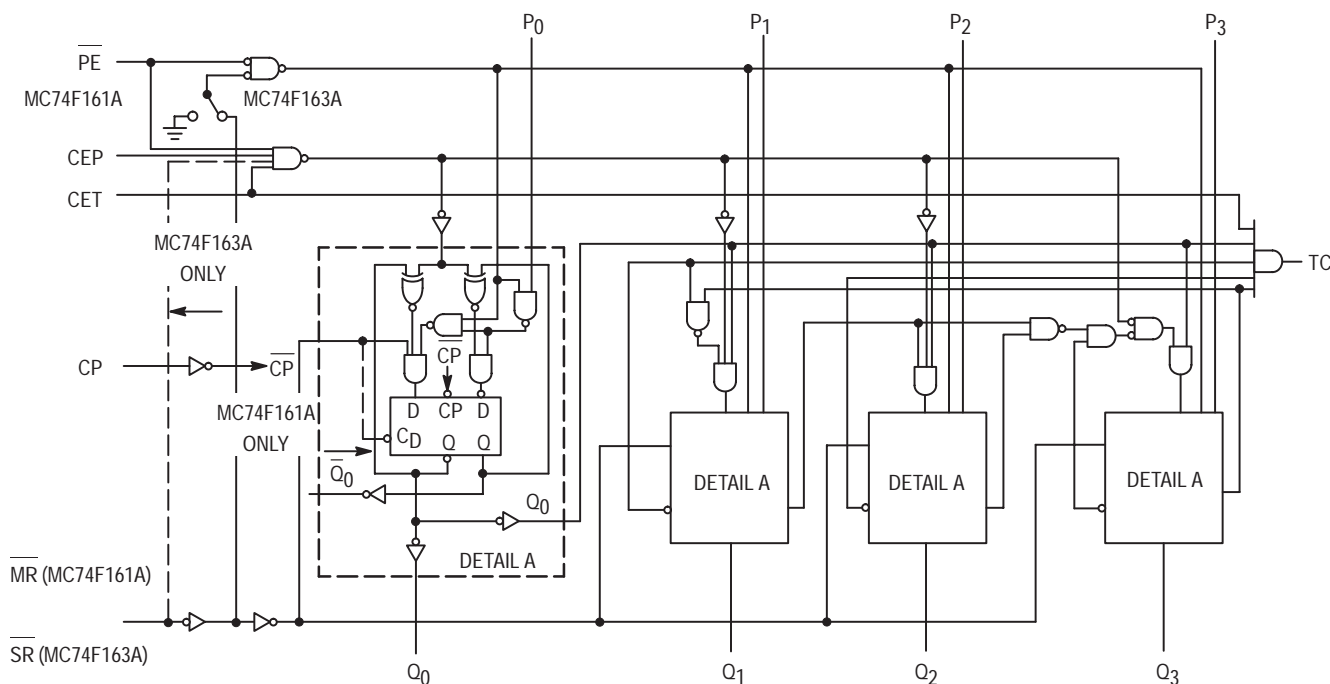


V_{CC} = PIN 16
 GND = PIN 8

*MR for MC74F161A
*SR for MC74F163A

MC74F161A • MC74F163A

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74F161A and MC74F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the MC74F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (MC74F161A), synchronous reset (MC74F163A), parallel load, count-up and hold. Five control inputs— Master Reset (MR, MC74F161A), Synchronous Reset (SR, MC74F163A), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)— determine the mode of operation, as shown in the Function Table. A LOW signal on MR overrides

all other inputs and asynchronously forces all outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR (MC74F161A) or SR (MC74F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74F161A and MC74F163A use D-type edge-triggered flip-flops and changing the SR, PE, CEP, and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

MC74F161A • MC74F163A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			– 1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage			–1.2	V	V _{CC} = MIN, I _{IN} = – 18 mA
V _{OH}	Output HIGH Voltage	74	2.5	3.4	V	I _{OH} = –1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = –1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Data, CEP, Clock PE, CET, SR			–0.6 –1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	–60		– 150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		37	55	mA	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is there-

fore not recommended for use as a clock or asynchronous reset for flip-flops, counters, or registers.

Logic Equations:

$$\text{Count Enable} = \text{CEP} \cdot \text{CET} \cdot \overline{\text{PE}}$$

$$\text{TC} = \text{Q}_0 \cdot \text{Q}_1 \cdot \text{Q}_2 \cdot \text{Q}_3 \cdot \text{CET}$$

MC74F161A • MC74F163A

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}	Maximum Count Frequency	100		90		MHz
t _{PLH}	Propagation Delay, Count	3.5	6.0	3.5	7.0	ns
t _{PHL}	CP to Q _n (PE Input HIGH)	3.5	10	3.5	11	
t _{PLH}	Propagation Delay	3.5	7.0	3.5	9.5	ns
t _{PHL}	CP to Q _n (PE Input LOW)	4.0	8.5	4.0	9.5	
t _{PLH}	Propagation Delay	5.0	14	5.0	15	ns
t _{PHL}	CP to TC	4.5	14	4.5	15	
t _{PLH}	Propagation Delay	2.5	7.5	2.5	8.5	ns
t _{PHL}	CET to TC	2.5	7.5	2.5	8.5	
t _{PHL}	Propagation Delay MR to Q _n (MC74F161A)	5.5	12	5.5	13	ns
t _{PHL}	Propagation Delay MR to TC (MC74F161A)	4.5	10.5	4.5	11.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	5.0		5.0		ns
t _S (L)	P _n to CP	5.0		5.0		
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		ns
t _H (L)	P _n to CP	2.0		2.0		
t _S (H)	Setup Time, HIGH or LOW	11		11.5		ns
t _S (L)	PE or SR to CP	8.5		9.5		
t _H (H)	Hold Time, HIGH or LOW	2.0		2.0		ns
t _H (L)	PE or SR to CP	0		0		
t _S (H)	Setup Time, HIGH or LOW	11		11.5		ns
t _S (L)	CEP or CET to CP	5.0		5.0		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	CEP or CET to CP	0		0		
t _W (H)	Clock Pulse Width (Load)	5.0		5.0		ns
t _W (L)	HIGH or LOW	5.0		5.0		
t _W (H)	Clock Pulse Width (Count)	4.0		4.0		ns
t _W (L)	HIGH or LOW	6.0		7.0		
t _W (L)	MR Pulse Width, LOW (MC74F161A)	5.0		5.0		ns
t _{rec}	Recovery Time, MR to CP (MC74F161A)	6.0		6.0		

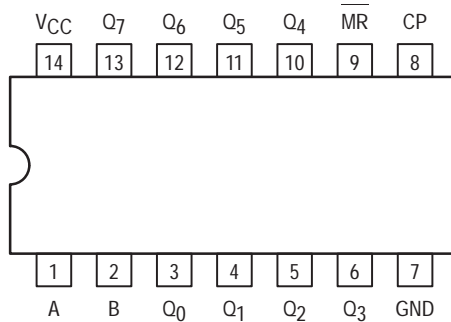


8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

The MC54/74F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

- Typical Shift Frequency of 90 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers

CONNECTION DIAGRAM



MODE SELECT TABLE

Operating Mode	Inputs			Outputs	
	MR	A	B	Q ₀	Q ₁ -Q ₇
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q ₀ -q ₆
	H	l	h	L	q ₀ -q ₆
	H	h	l	L	q ₀ -q ₆
	H	h	h	H	q ₀ -q ₆

H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

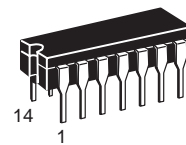
X = Don't Care

q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

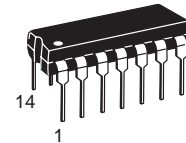
MC54/74F164

8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

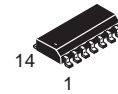
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

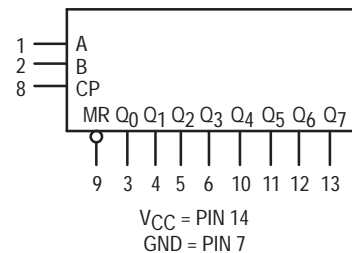


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

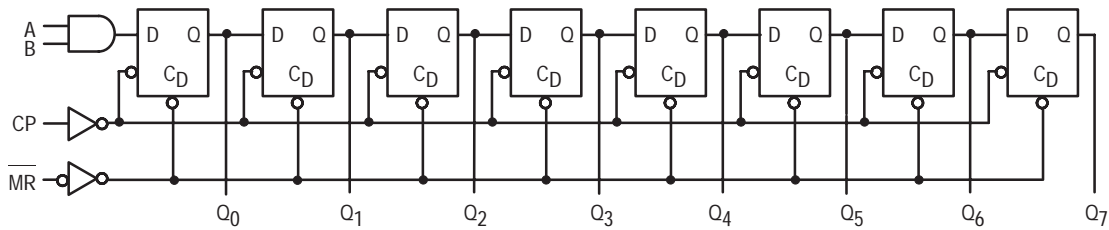
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F164

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = MIN
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		35	55	mA	A, B = GND, V _{CC} = MAX CP = HIGH, MR = GND

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F164

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	80	90		70		80		MHz
t _{PLH}	Propagation Delay	3.0	6.0	8.0	3.0	11	3.0	9.0	ns
t _{PHL}	CP to Q _n	5.0	7.5	10	5.0	13	5.0	11	
t _{PHL}	Propagation Delay MR to Q _n	5.5	10.5	13	5.5	16	5.5	14	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _{S(H)}	Setup Time, HIGH or LOW	7.0			7.0		7.0		ns
t _{S(L)}	D _n to CP	7.0			7.0		7.0		
t _{H(H)}	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t _{H(L)}	D _n to CP	1.0			1.0		1.0		ns
t _{W(H)}	CP Pulse Width, HIGH or LOW	4.0			4.0		4.0		
t _{W(L)}		7.0			7.0		7.0		
t _{W(L)}	MR Pulse Width, LOW	7.0			7.0		7.0		ns
t _{rec}	Recovery Time, MR to CP	7.0			7.0		7.0		ns

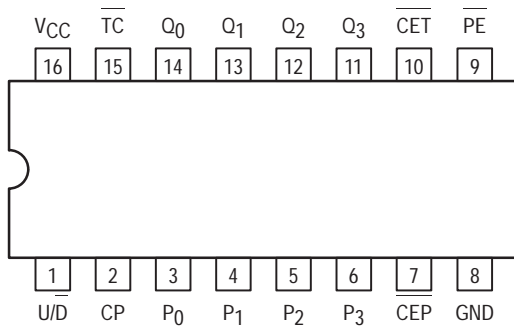


4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

The MC54/74F168 and MC54/74F169 are fully synchronous 4-stage up/down counters. The F168 is a BCD decade counter; the F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading, and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- Asynchronous Counting and Loading
- Built-In Lookahead Carry Capability
- Presetable for Programmable Operation

CONNECTION DIAGRAM (TOP VIEW)

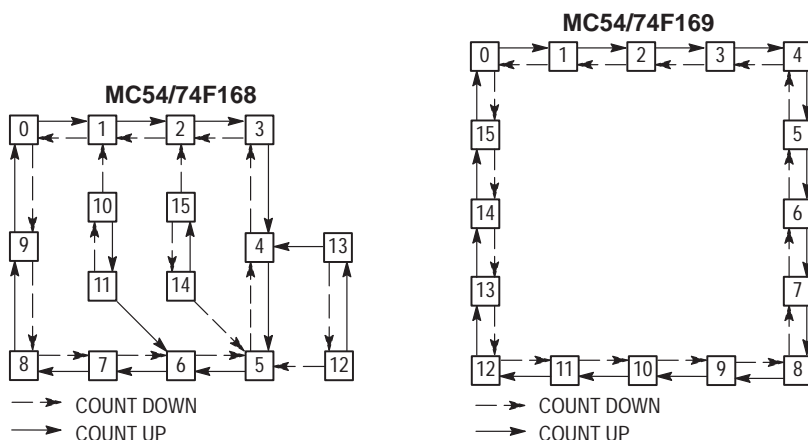


MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

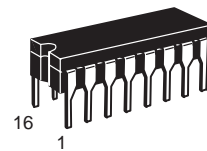
STATE DIAGRAMS



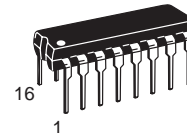
MC54/74F168 MC54/74F169

4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

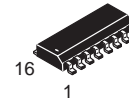
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

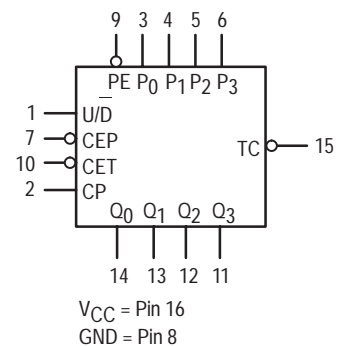


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

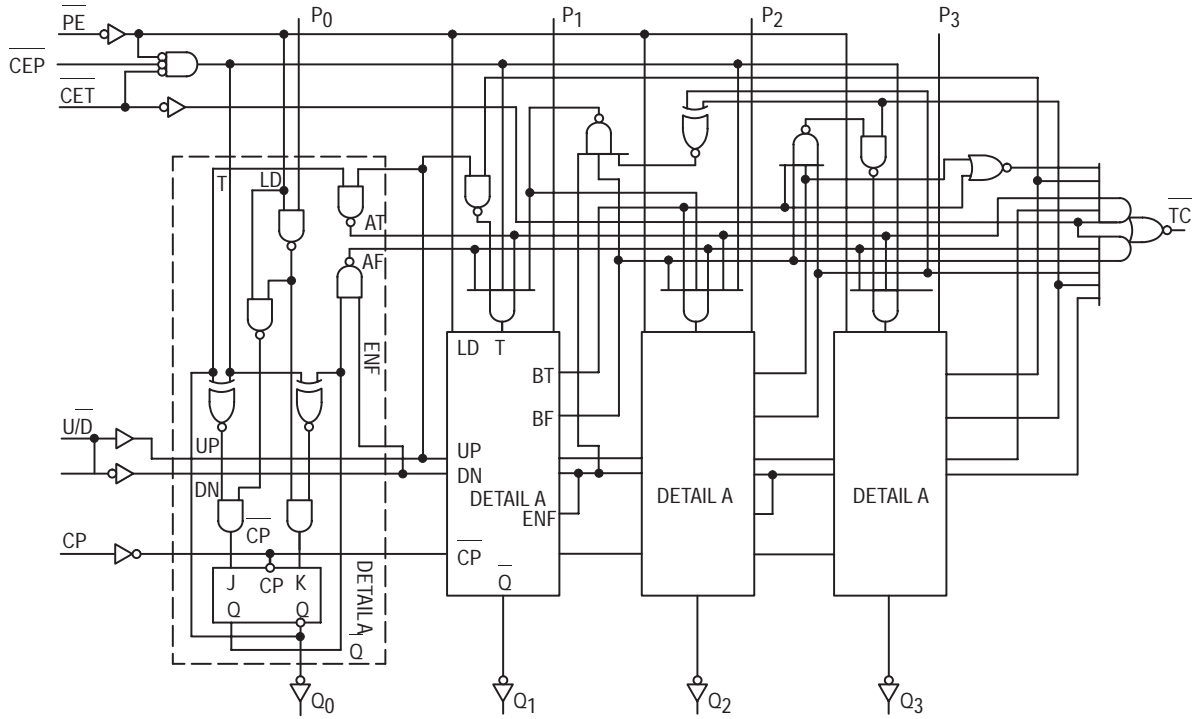
LOGIC SYMBOL



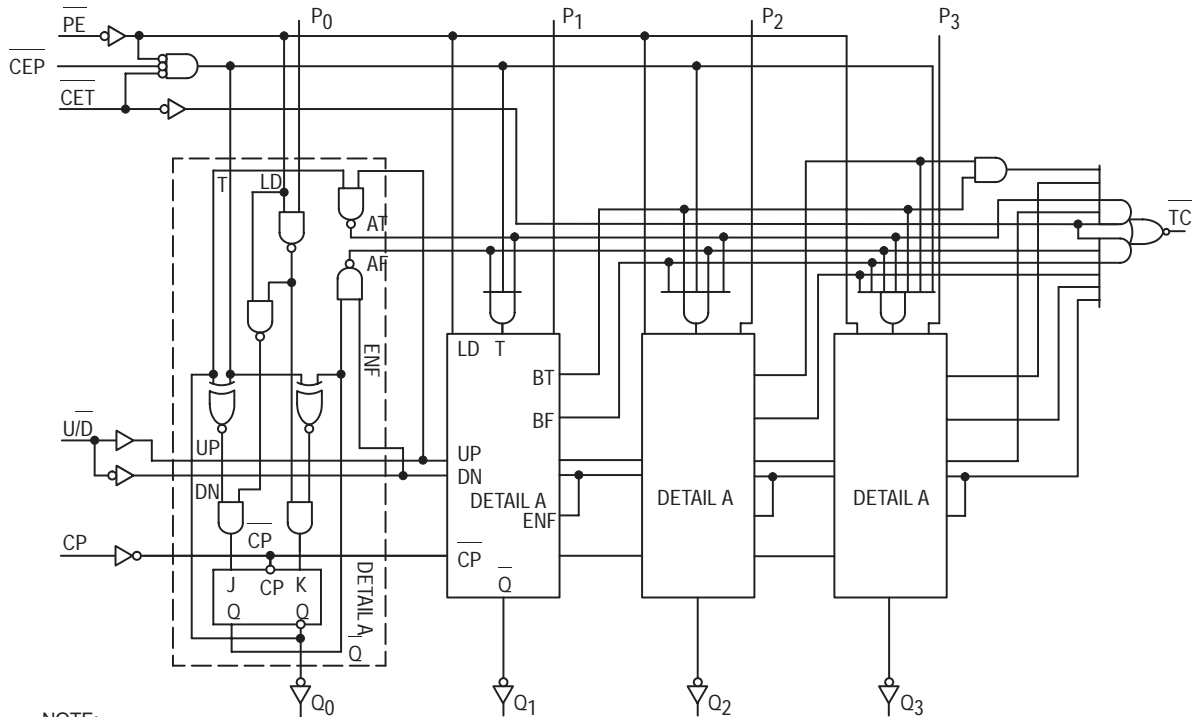
MC54/74F168 • MC54/74F169

LOGIC DIAGRAMS

MC54/74F168



MC54/74F169



NOTE:
These diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F168 • MC54/74F169

FUNCTIONAL DESCRIPTION

The F168 and F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the P₀-P₃ inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both \overline{CET} and CET must be LOW and PE must be HIGH; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the F169) in the Count Up mode. The TC

output state is not a function of the Count Enable Parallel (CEP) input level. The TC output of the F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the F168 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on TC. For this reason the use of TC as a clock signal is not recommended (see logic equations below).

- 1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot PE$
- 2) Up: (F168): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
(F169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot CET$
- 3) Down: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Down) \cdot CET$

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current CET Other Inputs			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
				-0.6		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			52	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F168 • MC54/74F169

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100		60		85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (PE HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC (F168)	5.5 4.0	15.5 11	5.5 4.0	18 13.5	5.5 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC (F169)	5.0 4.0	15.5 11	5.0 4.0	18 13.5	5.0 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/D to TC (F168)	3.5 4.0	11 16	3.5 4.0	13.5 18.5	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation Delay U/D to TC (F169)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Max	Min	Max	Min	Max	
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		5.5 5.5		4.5 4.5		ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup Time, HIGH or LOW CEP or CET to CP	5.0 5.0		7.0 7.0		6.0 6.0		ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold Time HIGH or LOW CEP or CET to CP	0 0		0 0		0 0		ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup Time, HIGH or LOW PE to CP	8.0 8.0		10 10		9.0 9.0		ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold Time, HIGH or LOW PE to CP	0 0		0 0		0 0		ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup Time, HIGH or LOW (F168) U/D to CP	11 16.5		13.5 19		12.5 18		ns
$t_{\text{S(H)}}$ $t_{\text{S(L)}}$	Setup Time, HIGH or LOW (F169) U/D to CP	11 7.0		13.5 9.0		12.5 8.0		ns
$t_{\text{H(H)}}$ $t_{\text{H(L)}}$	Hold time, HIGH or LOW U/D to CP	0 0		0 0		0 0		ns
$t_{\text{W(H)}}$ $t_{\text{W(L)}}$	CP Pulse Width HIGH or LOW	5.0 5.0		8.0 8.0		5.5 5.5		ns



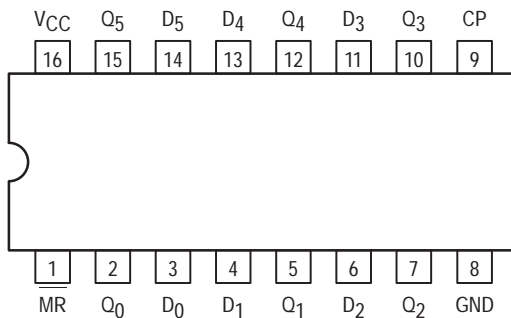
HEX D FLIP-FLOP WITH MASTER RESET

The MC54/74F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The device has a Master Reset to simultaneously clear all flip-flops.

The F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. The state of each D input, one setup time before low-to-high clock transition, is transferred to the corresponding flip-flop's Q output. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The F174 is useful for applications where only the true output is required and the Clock and Master Reset are common to all storage elements.

- Six Edge-triggered D-type Inputs
- Buffered Positive Edge-triggered Common Clock
- Buffered, Asynchronous Common Reset

CONNECTION DIAGRAM DIP (TOP VIEW)



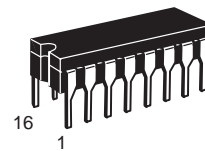
FUNCTION TABLE

Inputs	Outputs
@ t_n , MR = H	@ $t_n + 1$
D_n	Q_n
H	H
L	L

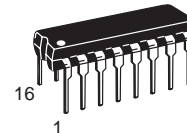
t_n = Bit time before clock pulse
 $t_n + 1$ = Bit time after clock pulse
 H = HIGH Voltage Level
 L = LOW Voltage Level

MC54/74F174

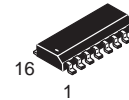
HEX D FLIP-FLOP WITH MASTER RESET
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

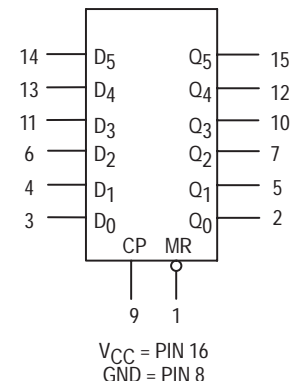


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

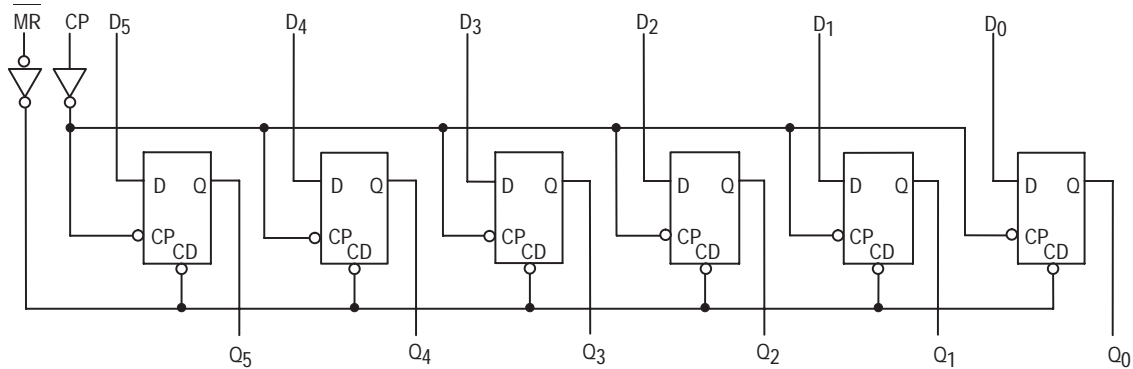
MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F174

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OL} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OL} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		30	45	mA	V _{CC} = MAX, D _n = MR = 4.5 V, CP =

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F174

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		80		80		MHz
t _{PLH}	Propagation Delay CP to Q _n	3.5	5.5	8.0	3.5	10.0	3.5	9.0	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	10	14	5.0	16.0	5.0	15.0	ns

AC OPERATING REQUIREMENTS

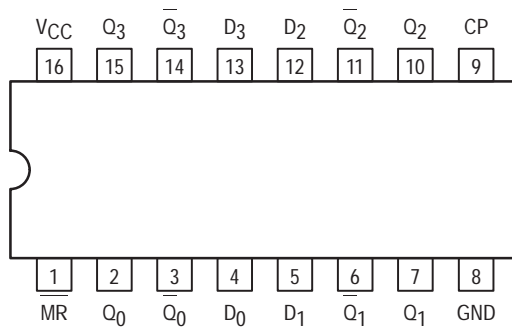
Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.0			4.0		4.0		ns
t _S (L)	D _n to CP	4.0			4.0		4.0		
t _H (H)	Hold Time, HIGH or LOW	0			1.0		0		
t _H (L)	D _n to CP	0			1.0		0		ns
t _W (H)	CP Pulse Width, HIGH	4.0			4.0		4.0		
t _W (L)	or LOW	6.0			6.0		6.0		
t _W (L)	MR Pulse Width LOW	5.0			5.0		5.0		ns
t _{rec}	Recovery Time MR to CP	5.0			5.0		5.0		ns

QUAD D FLIP-FLOP

The MC54/74F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where both true and complementary outputs are required and clock and clear inputs are common to all flip-flops. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs when LOW.

- Four Edge-triggered D-type Inputs
- Buffered Positive Edge-triggered Common Clock
- Buffered Asynchronous Common Reset
- True and Complementary Outputs
- ESD > 4000 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



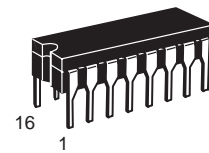
FUNCTION TABLE

Inputs	Outputs	
@ t_n , MR = H	@ $t_n + 1$	
D _n	Q _n	\bar{Q}_n
L	L	H
H	H	L

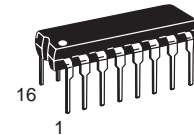
t_n = Bit time before clock positive-going transition
 $t_n + 1$ = Bit time after clock positive-going transition
 H = HIGH Voltage Level
 L = LOW Voltage Level

MC54/74F175

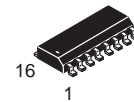
QUAD D FLIP-FLOP
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

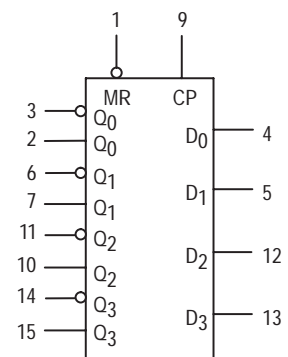


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXD SOIC

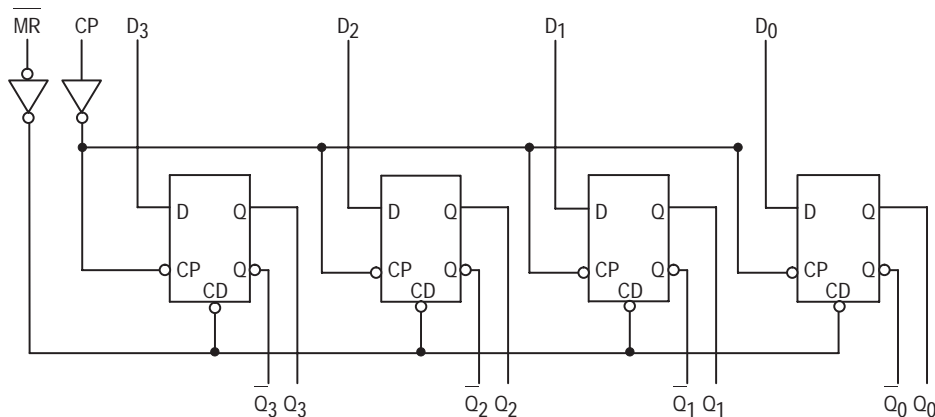
LOGIC SYMBOL



VCC = PIN 16
 GND = PIN 8

MC54/74F175

LOGIC DIAGRAM



NOTE:

This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs, one setup time before, on the LOW-to-HIGH clock (CP) transition, causing individual Q and

\bar{Q} outputs to follow. A LOW input on the Master Reset (MR) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs. The F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.50$ V
		74	2.7	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20$ mA	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μ A	$V_{IN} = 2.7$ V	$V_{CC} = \text{MAX}$
				100	μ A	$V_{IN} = 7.0$ V	$V_{CC} = \text{MAX}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		22.5	34	mA	$D_n = \text{MR} = 4.5$ V $CP = \sqrt{\quad}$	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F175

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		100		100		MHz
t _{PLH}	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t _{PHL}	CP to Q _n or \overline{Q}_n	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t _{PHL}	Propagation Delay MR to Q _n	4.5	9.0	11.5	4.5	15	4.5	13	ns
t _{PLH}	Propagation Delay MR to \overline{Q}_n	4.0	6.5	8.5	4.0	10	4.0	9.0	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
t _S (L)	D _n to CP	3.0			3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0			1.0		1.0		ns
t _H (L)	D _n to CP	1.0			1.0		1.0		
t _W (H)	CP Pulse Width, HIGH	4.0			4.0		4.0		ns
t _W (L)	or LOW	5.0			5.0		5.0		
t _W (L)	MR Pulse Width, LOW	5.0			5.0		5.0		ns
t _{rec}	Recovery Time, MR to CP	5.0			5.0		5.0		ns

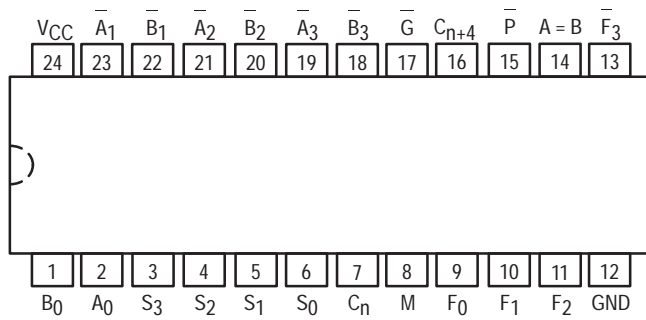


4-BIT ARITHMETIC LOGIC UNIT

The MC54/74F181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

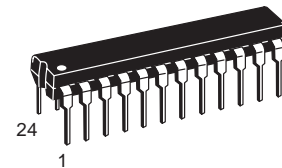
- Provides 16 Arithmetic Operations, ie, Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables, ie, Exclusive-OR, Compare, AND, NAND, OR, NOR, Plus Ten Other Logic Operations
- Full Lookahead for High-Speed Arithmetic Operation on Long Words

CONNECTION DIAGRAM



MC54/74F181

4-BIT ARITHMETIC LOGIC UNIT
FAST™ SCHOTTKY TTL



N SUFFIX
PLASTIC
CASE 724-03

ORDERING INFORMATION

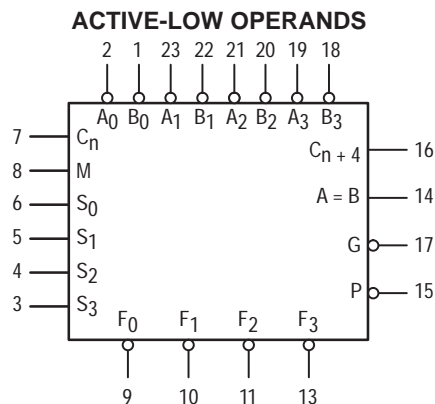
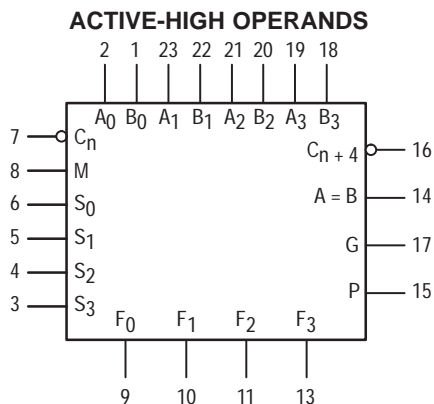
MC54/74FXXXN Plastic

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
V _{OH}	Output Voltage — High A = B output	54, 74			5.5	V
I _{OL}	Output Current — Low	54, 74			20	mA

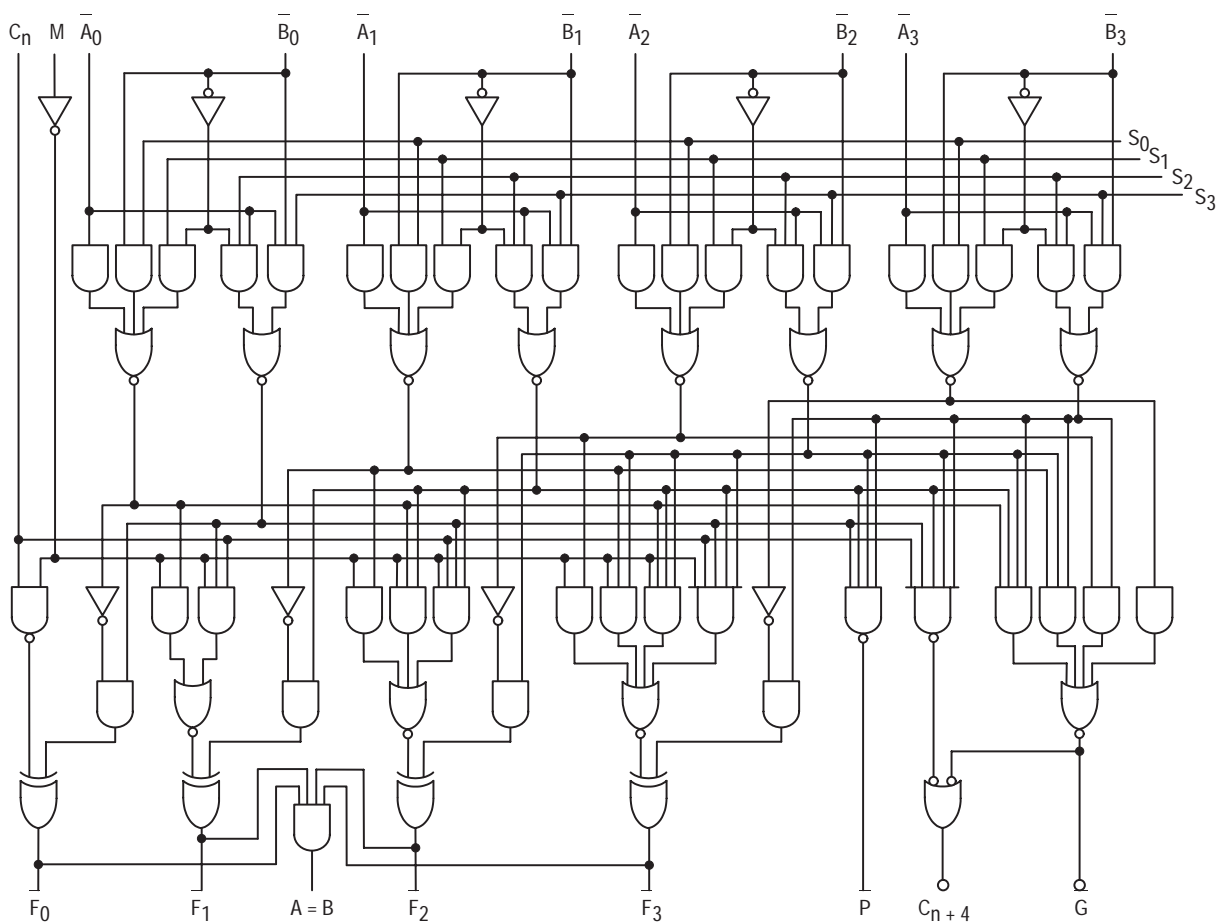
MC54/74F181

LOGIC SYMBOLS



VCC = PIN 24
GND = PIN 12

LOGIC DIAGRAM



MC54/74F181

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18 \text{ mA}$	$V_{CC} = \text{MIN}$
I_{OH}	Output Current — HIGH			250	μA	$V_{OH} = 5.5 \text{ V}$	$V_{CC} = \text{MIN}, A = B$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.5 \text{ V}$
		74	2.7	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20 \text{ mA}$	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7 \text{ V}$	$V_{CC} = \text{MAX}$
				100	μA	$V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current	M Input		-0.6	mA	$V_{IN} = 0.5 \text{ V}$	$V_{CC} = \text{MAX}$
		A and B Inputs		-1.8	mA		
		S_{0-3} Inputs		-2.4	mA		
		C_n Input		-3.0	mA		
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		43	65	mA	$V_{CC} = \text{MAX}$	

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-HIGH or active-LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate). In the Add mode, P indicates that F is 15 or more, while G indicates that F is 16 or more. In the Subtract mode, P indicates that F is zero or less, while G indicates that F is less than zero. P and G are not affected by carry in. When speed requirements are not stringent, it can be used in a simple Ripple Carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for

each group of four F181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-LOW inputs producing active-LOW outputs or with active-HIGH inputs producing active-HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

MC54/74F181

AC CHARACTERISTICS

Symbol	Path	Mode	54/74F		54F		74F		Unit
			T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
			Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	C _n to C _{n+4}		3.0 3.0	8.5 8.0	3.0 3.0	10.5 10	3.0 3.0	9.5 9.0	ns
t _{PLH} t _{PHL}	A or B to C _{n+4}	Sum	5.0 5.0	13 12	5.0 5.0	15 14	5.0 5.0	14 13	ns
t _{PLH} t _{PHL}	A or B to C _{n+4}	Dif	5.0 5.0	14 13	5.0 5.0	16 15	5.0 5.0	15 14	ns
t _{PLH} t _{PHL}	C _n to F	Any	3.0 3.0	8.5 8.5	3.0 3.0	10.5 10.5	3.0 3.0	9.5 9.5	ns
t _{PLH} t _{PHL}	A or B to G	Sum	3.0 3.0	7.5 7.5	3.0 3.0	9.5 9.5	3.0 3.0	8.5 8.5	ns
t _{PLH} t _{PHL}	A or B to G	Dif	3.0 3.0	8.5 9.5	3.0 3.0	10.5 11.5	3.0 3.0	9.5 10.5	ns
t _{PLH} t _{PHL}	A or B to P	Sum	3.0 3.0	7.0 7.5	3.0 3.0	9.0 9.5	3.0 3.0	8.0 8.5	ns
t _{PLH} t _{PHL}	A or B to P	Dif	4.0 3.5	7.5 8.5	4.0 3.5	9.5 10.5	4.0 3.5	8.5 9.5	ns
t _{PLH} t _{PHL}	A _i or B _j to F _i	Sum	3.0 3.0	9.0 10	3.0 3.0	11 11	3.0 3.0	10 10	ns
t _{PLH} t _{PHL}	A _i or B _j to F _i	Dif	3.0 3.0	11 11	3.0 3.0	13 13	3.0 3.0	12 12	ns
t _{PLH} t _{PHL}	Any A or B to Any F	Sum	4.0 4.0	10.5 10	4.0 4.0	12.5 12	4.0 4.0	11.5 11	ns
t _{PLH} t _{PHL}	Any A or B to Any F	Dif	4.5 4.5	12 12	4.5 4.5	14 14	4.5 4.5	13 13	ns
t _{PLH} t _{PHL}	A or B to F	Logic	4.0 4.0	9.0 10	4.0 4.0	11 12	4.0 4.0	10 11	ns
t _{PLH} t _{PHL}	A or B to A = B	Dif	11 7.0	27 12.5	11 7.0	31 14.5	11 7.0	29 13.5	ns

MC54/74F181

FUNCTION TABLE

Mode Select Inputs				Active-LOW Operands & F _n Outputs		Active-HIGH Operands & F _n Outputs	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic** (M = L) (C _n = L)	Logic (M = H)	Arithmetic** (M = L) (C _n = H)
L	L	L	L	\overline{A}	A minus 1	\overline{A}	A
L	L	L	H	$\overline{A}\overline{B}$	$\overline{A}\overline{B}$ minus 1	$\overline{A} + \overline{B}$	A + \overline{B}
L	L	H	L	A + B	AB minus 1	AB	A + B
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus (A + \overline{B})	$\overline{A}\overline{B}$	A plus $\overline{A}\overline{B}$
L	H	L	H	\overline{B}	AB plus (A + B)	\overline{B}	(A + B) plus $\overline{A}\overline{B}$
L	H	H	L	$A \oplus \overline{B}$	A minus B minus 1	$A \oplus \overline{B}$	A minus B minus 1
L	H	H	H	A + B	A + B	AB	AB minus 1
H	L	L	L	$\overline{A}\overline{B}$	A plus (A + B)	$\overline{A} + \overline{B}$	A plus AB
H	L	L	H	$A \oplus \overline{B}$	A plus B	$A \oplus \overline{B}$	A plus \overline{B}
H	L	H	L	\overline{B}	AB plus (A + B)	\overline{B}	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	AB	$\overline{A}\overline{B}$ plus A	A + B	(A + \overline{B}) plus A
H	H	H	L	AB	AB minus A	A + B	(A + B) plus A
H	H	H	H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position.

**Arithmetic operations expressed in 2s complement notation.

H = HIGH Voltage Level

L = LOW Voltage Level

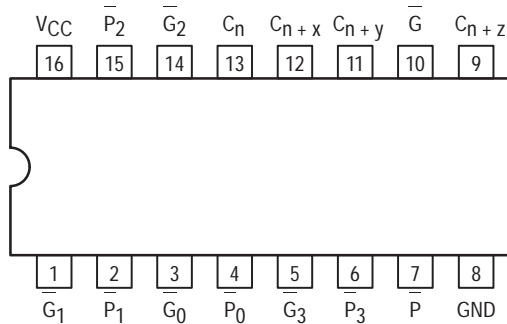


CARRY LOOKAHEAD GENERATOR

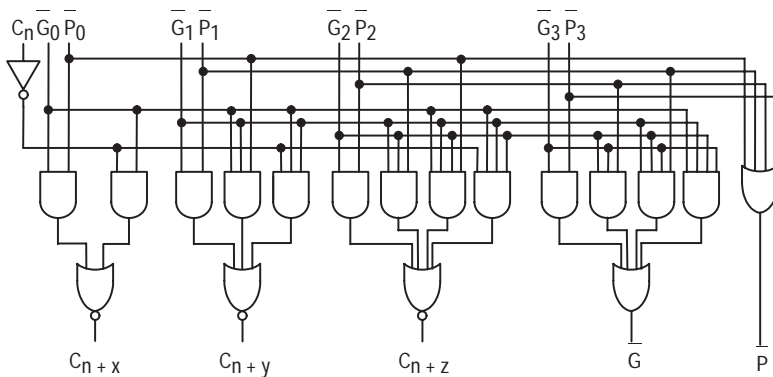
The MC54/74F182 is a high-speed carry lookahead generator. It is generally used with the F181, F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

- Provides Lookahead Carries Across a Group of Four ALUs
- Multi-level Lookahead High-speed Arithmetic Operation Over Long Word Lengths

CONNECTION DIAGRAM DIP (TOP VIEW)



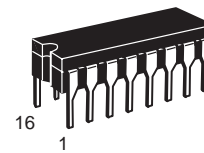
LOGIC DIAGRAM



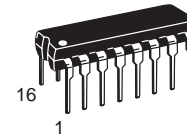
MC54/74F182

CARRY LOOKAHEAD GENERATOR

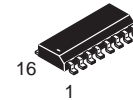
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

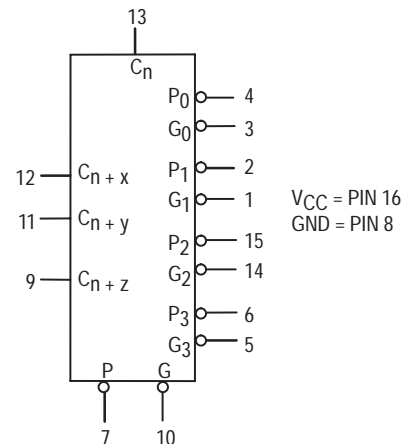


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



MC54/74F182

FUNCTION TABLE

Inputs									Outputs				
C _n	G ₀	P ₀	G ₁	P ₁	G ₂	P ₂	G ₃	P ₃	C _{n+x}	C _{n+y}	C _{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F182

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4		V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4		V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100	μA	V _{IN} = 7.0 V	V _{CC} = MAX
I _{IL}	Input LOW Current	C _n Input			-1.2	mA	V _{IN} = 0.5 V	V _{CC} = MAX
		P ₃ Input			-2.4			
		P ₂ Input			-3.6			
		G ₃ , P ₀ , P ₁ Inputs			-4.8			
		G ₀ , G ₂ Inputs			-8.4			
		G ₁ Input			-9.6			
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current (All Outputs HIGH)			18.4	28	mA	P ₃ , G ₃ = 4.5 V All Other Inputs = GND	V _{CC} = MAX
I _{CCL}	Power Supply Current (All Outputs LOW)			23.5	36	mA	G ₀ , G ₁ , G ₂ = 4.5 V All Other Inputs = GND	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- No more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	10.5	3.0	9.5	ns
t _{PHL}	C _n to C _{n+x} , C _{n+y} , C _{n+z}	3.0	6.8	9.0	3.0	11	3.0	10	
t _{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	10.7	2.5	9.0	ns
t _{PHL}	P ₀ , P ₁ , or P ₂ to C _{n+x} , C _{n+y} , C _{n+z}	1.5	3.7	5.0	1.5	6.5	1.5	6.0	
t _{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	10.5	2.5	9.5	ns
t _{PHL}	G ₀ , G ₁ , or G ₂ to C _{n+x} , C _{n+y} , C _{n+z}	1.5	3.9	5.2	1.5	6.5	1.5	6.0	

MC54/74F182

AC CHARACTERISTICS (Continued)

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
tPLH	Propagation Delay $\overline{P}_1, \overline{P}_2, \text{ or } \overline{P}_3 \text{ to } \overline{G}$	2.0	7.9	10	2.0	12.5	2.0	11	ns
tPHL		2.0	6.0	8.0	2.0	9.5	2.0	9.0	
tPLH	Propagation Delay $\overline{G}_N \text{ to } \overline{G}$	2.0	8.3	10.5	2.0	12.5	2.0	11.5	ns
tPHL		1.5	5.7	7.5	1.5	9.5	1.5	8.5	
tPLH	Propagation Delay $\overline{P}_N \text{ to } \overline{P}$	2.5	5.7	7.5	2.5	11	2.5	8.5	ns
tPHL		2.5	4.1	5.5	2.5	7.5	2.5	6.5	

FUNCTIONAL DESCRIPTION

The F182 carry lookahead generator accepts up to four pairs of active-LOW Carry Propagate (\overline{P}_0 - \overline{P}_3) and carry Generate (\overline{G}_0 - \overline{G}_3) signals and an active-HIGH Carry input (C_n) and provides anticipated active-HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The F182 also has active-LOW Carry Propagate (\overline{P}) and Carry Generate (\overline{G}) outputs which may be used for further levels of lookahead. The logic equations provided at the output are:

$$C_{n+x} = G_0 + P_0 C_n$$

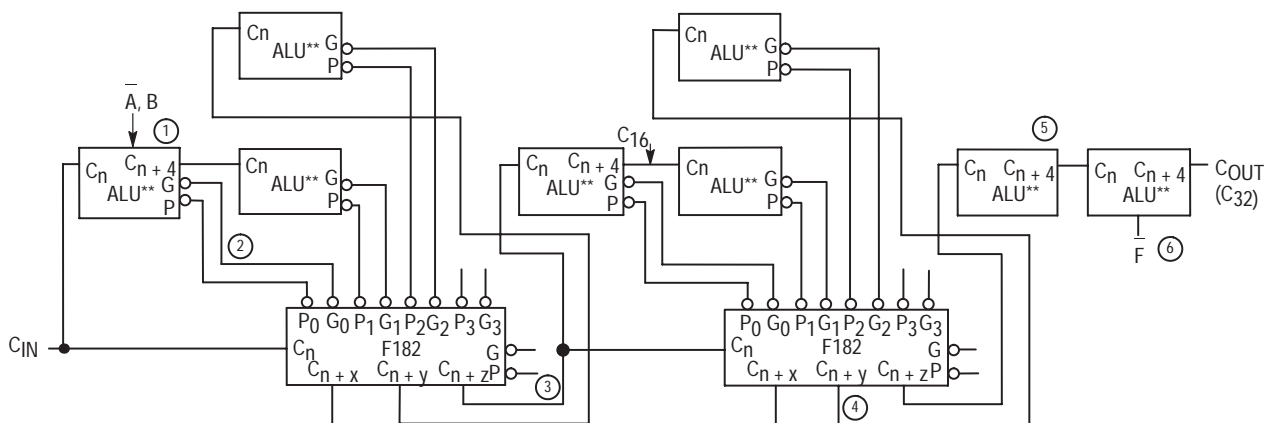
$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$G = \overline{G}_3 + P_3 \overline{G}_2 + P_3 P_2 \overline{G}_1 + P_3 P_2 P_1 \overline{G}_0$$

$$P = P_3 P_2 P_1 P_0$$

Also, the F182 can be used with binary ALUs in an active-LOW or active-HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last F181 or F381.



** ALUs may be either F181, F381, or 2901A.

Figure 1. 32-Bit ALU with Ripple Carry Between 16-Bit Lookahead ALUs



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

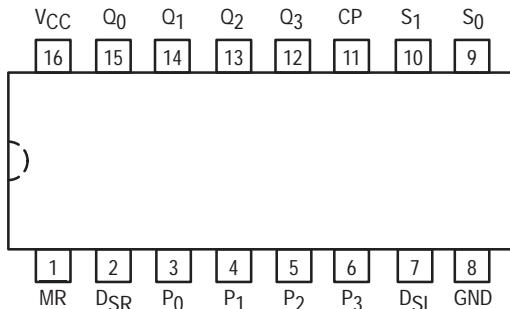
The MC74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The F194 is similar in operation to the S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- Typical Shift Frequency of 150 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers

FUNCTIONAL DESCRIPTION

The F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0 , S_1) inputs determine the type of operation, as shown in the Function Table. Signals on the Select, Parallel data (P_0 – P_3) and Serial data (D_{SR} , D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset (MR) overrides all other inputs and forces the outputs LOW.

CONNECTION DIAGRAM



FUNCTION TABLE

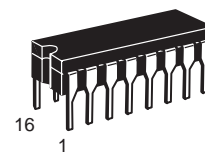
Operating Mode	Inputs						Outputs			
	MR	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 p_n , q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

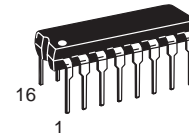
MC74F194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

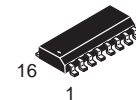
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

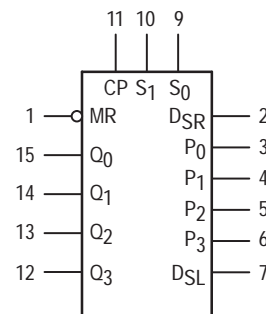


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

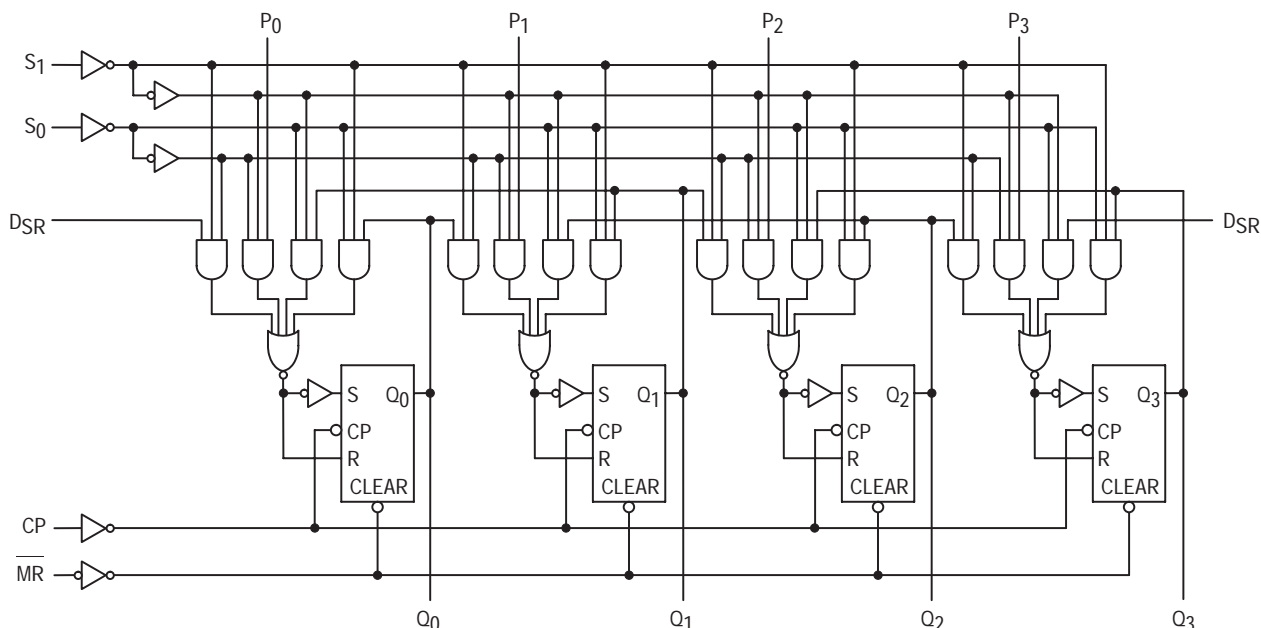
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MC74F194

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		33	46	mA	S _n , MR, DSR, D _{SL} = 4.5 V P _n = Gnd, CP = ⌊	V _{CC} = MAX

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F194

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}	Maximum Shift Frequency	105		90		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	3.0 3.5	7.0 7.5	3.5 3.5	8.0 8.0	ns
t _{PHL}	Propagation Delay MR to Q _n	4.5	12	4.5	14	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V		T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		
		Min	Max	Min	Max	
t _s (H) t _s (L)	Set up Time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	4.0 4.0		4.0 4.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	0 0		1.0 1.0		
t _s (H) t _s (L)	Set up Time, HIGH or LOW S _n to CP	8.0 8.0		9.0 8.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW S _n to CP	0 0		0 0		
t _w (H)	CP Pulse Width HIGH	5.0		5.5		ns
t _w (L)	MR Pulse Width LOW	5.0		5.0		ns
t _{rec}	Recovery Time MR to CP	7.0		8.0		ns



4-BIT PARALLEL ACCESS SHIFT REGISTER

The functional characteristics of the MC74F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting, and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

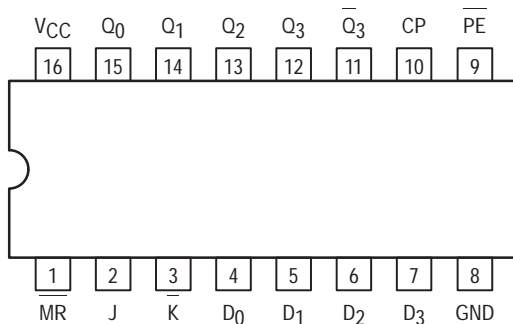
The MC74F195 operates in two primary modes, shift right (Q_0 - Q_1) and parallel load, which are controlled by the state of the Parallel Enable (PE) input. Serial data enters the first flip-flop (Q_0) via the J and K inputs when the PE input is HIGH, and is shifted 1 bit in the direction Q_0 - Q_1 - Q_2 - Q_3 following each LOW-to-HIGH clock transition. The J and K inputs provide the flexibility of the JK type input is made for special applications, and by tying the two pins together the simple D-type input is made for general applications. The device appears as four common clocked D flip-flops when the PE input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs. Shift left operation (Q_3 - Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the PE input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The MC74F195 utilizes edge-triggering; therefore, there is no restriction on the activity of the J, K, D_n , and PE inputs for logic operation, other than the setup and hold time requirements.

A LOW on the asynchronous Master Reset (MR) input sets all Q outputs LOW, independent of any other input condition.

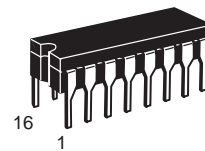
- Shift Right and Parallel Load Capability
- J-K (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset

CONNECTION DIAGRAM DIP

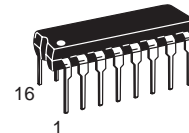


MC74F195

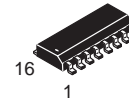
4-BIT PARALLEL ACCESS SHIFT REGISTER FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

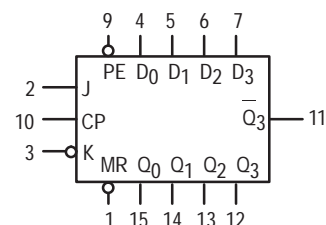


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



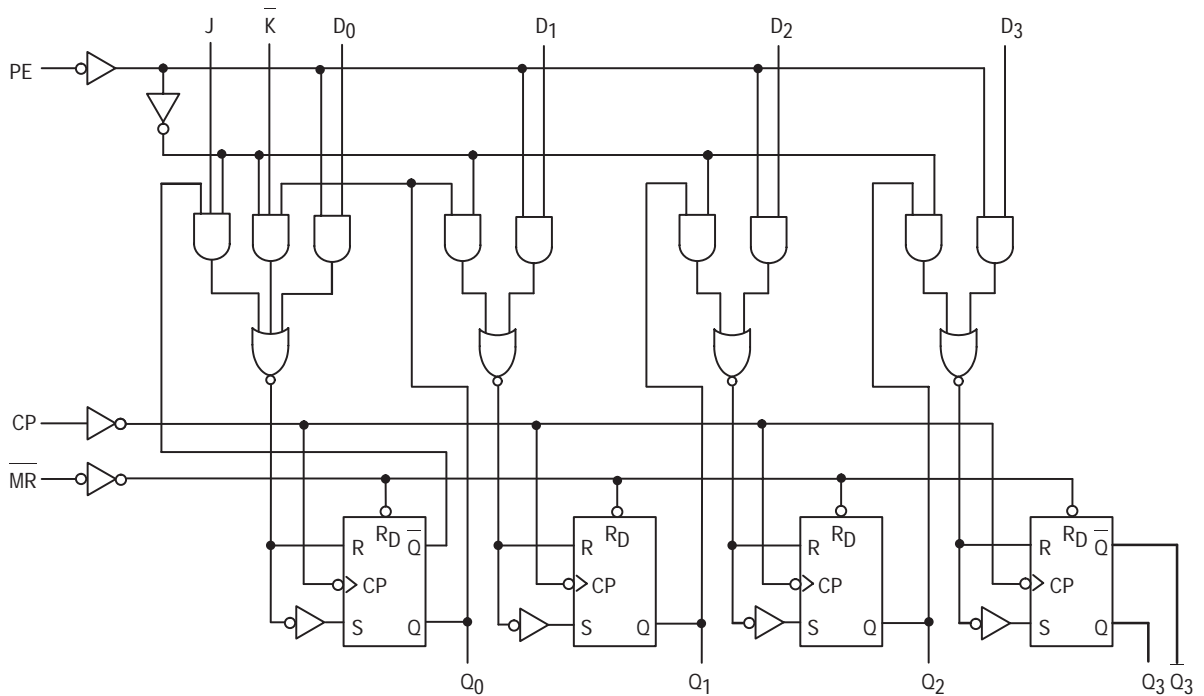
V_{CC} = PIN 16
GND = PIN 8

MC74F195

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

LOGIC DIAGRAM



FUNCTION TABLE

Operating Modes	Inputs						Outputs				
	MR	CP	PE	J	K	D _n	Q ₀	Q ₁	Q ₂	Q ₃	Q ₃
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q ₀	q ₁	q ₂	q ₂
Shift, Reset First Stage	H	↑	h	l	l	X	L	q ₀	q ₁	q ₂	q ₂
Shift, Toggle First Stage	H	↑	h	h	l	X	q ₀	q ₀	q ₁	q ₂	q ₂
Shift, Retain First Stage	H	↑	h	l	h	X	q ₀	q ₀	q ₁	q ₂	q ₂
Parallel Load	H	↑	l	X	X	d _n	d ₀	d ₁	d ₂	d ₃	d ₃

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition

MC74F195

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.5		V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7		V		V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA	V _{CC} = 4.5 V
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX	
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current			38	mA	V _{CC} = MAX	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{max}		105		90		MHz
t _{PLH}	Propagation Delay	2.5	7.0	2.5	8.0	ns
t _{PHL}	CP to Q/Q̄	2.5	8.0	2.5	9.0	
t _{PHL}	Propagation Delay, MR to Q	3.0	10	3.0	11	ns
t _{PLH}	Propagation Delay, MR to Q	3.0	10.5	3.0	11	ns

MC74F195

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F		74F		Unit
		T _A = + 25°C V _{CC} = + 5.0 V C _L = 50 pF		T _A = 0°C to + 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW J, K, D to CP	4.0		4.0		ns
t _S (L)		4.0		4.0		
t _H (H)	Hold Time, HIGH or LOW J, K, D to CP	0		1.0		ns
t _H (L)		0		1.0		
t _S (H)	Setup Time, HIGH or LOW PE to CP	8.0		9.0		ns
t _S (L)		8.0		9.0		
t _H (H)	Hold Time, HIGH or LOW PE to CP	0		0		ns
t _H (L)		0		0		
t _w (H)	CP Pulse Width, HIGH	5.0		5.5		ns
t _w (L)	MR Pulse Width, LOW	5.0		5.0		ns
t _{rec}	Recovery Time, MR to CP	7.0		8.0		ns

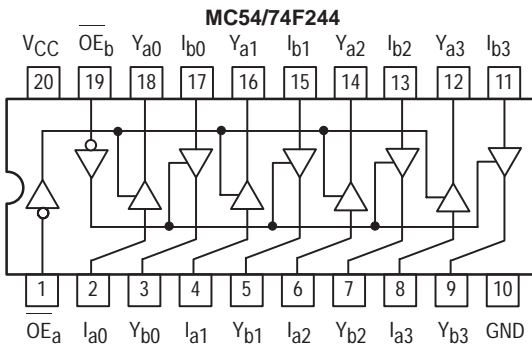
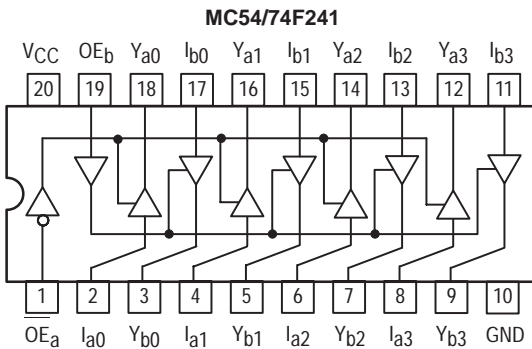
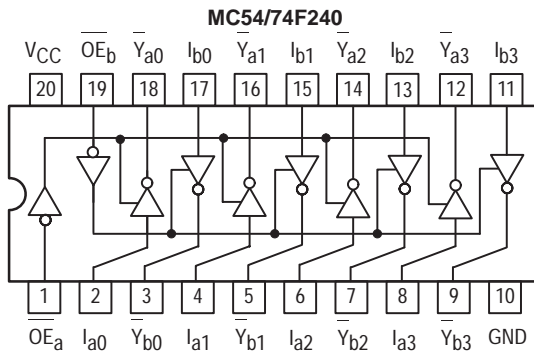


OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The F240, F241 and F244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers which provide improved PC board density.

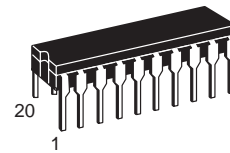
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 4000 Volts

CONNECTION DIAGRAMS

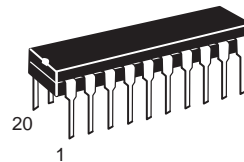


**MC54/74F240
 MC54/74F241
 MC54/74F244**

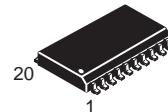
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS
FAST™ SCHOTTKY TTL



**J SUFFIX
 CERAMIC
 CASE 732-03**



**N SUFFIX
 PLASTIC
 CASE 738-03**



**DW SUFFIX
 SOIC
 CASE 751D-03**

ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXDW SOIC

MC54/74F240 • MC54/74F241 • MC54/74F244

**FUNCTION TABLE
MC54/74F240**

Inputs				Outputs	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

**FUNCTION TABLE
MC54/74F241**

Inputs				Outputs	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

**FUNCTION TABLE
MC54/74F244**

Inputs				Outputs	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = High Impedance

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-12	mA
		74			-15	
I _{OL}	Output Current — Low	54			48	mA
		74			64	

MC54/74F240 • MC54/74F241 • MC54/74F244

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
		54	2.0			V	I _{OH} = -12 mA	V _{CC} = 4.50 V
		74	2.0			V	I _{OH} = -15 mA	V _{CC} = 4.50 V
V _{OL}	Output LOW Voltage	54			0.55	V	I _{OL} = 48 mA	V _{CC} = MIN
		74			0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH				50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output Off Current LOW				-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	Data Inputs F241, F244			-1.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
		Other			-1.0			
I _{OS}	Output Short Circuit Current (Note 2)	74	-100		-225	mA	V _{OUT} = GND	V _{CC} = MAX
		54	-100		-275			
I _{CCH}	Power Supply Current HIGH	F240			35	mA	V _{CC} = MAX	
		F241, F244			60			
I _{CCL}	Power Supply Current LOW	F240			75			
		F241, F244			90			
I _{CCZ}	Power Supply Current OFF	F240			75			
		F241, F244			90			

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F240 • MC54/74F241 • MC54/74F244

AC CHARACTERISTICS – MC54/74F240

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, Data to Output	2.5	5.1	7.0	2.5	9.0	2.5	8.0	ns
t _{PHL}		1.5	3.5	4.7	1.5	6.0	1.5	5.7	
t _{PZH}	Output Enable Time	2.0	3.5	5.2	2.0	6.5	2.0	5.7	ns
t _{PZL}		4.0	6.9	9.0	4.0	13.5	4.0	10	
t _{PHZ}	Output Disable Time	2.0	4.0	5.3	2.0	6.5	2.0	6.3	ns
t _{PLZ}		1.5	6.0	8.0	2.0	12.5	1.5	9.5	

AC CHARACTERISTICS – MC54/74F241

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, Data to Output	2.5	4.0	5.2	2.0	6.5	2.5	6.2	ns
t _{PHL}		2.5	4.0	5.2	2.0	7.0	2.5	6.5	
t _{PZH}	Output Enable Time	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns
t _{PZL}		2.0	5.4	7.0	2.0	8.5	2.0	8.0	
t _{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	2.0	7.0	ns
t _{PLZ}		2.0	4.5	6.5	2.0	12.5	2.0	7.5	

AC CHARACTERISTICS – MC54/74F244

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay, Data to Output	2.5	4.0	5.2	2.5	6.5	2.5	6.2	ns
t _{PHL}		2.5	4.0	5.2	2.5	7.0	2.5	6.5	
t _{PZH}	Output Enable Time	2.0	4.3	5.7	2.0	7.0	2.0	6.7	ns
t _{PZL}		2.0	5.4	7.0	2.0	8.5	2.0	8.0	
t _{PHZ}	Output Disable Time	2.0	4.5	6.0	2.0	7.0	2.0	7.0	ns
t _{PLZ}		2.0	4.5	6.0	2.0	10.0	2.0	7.0	

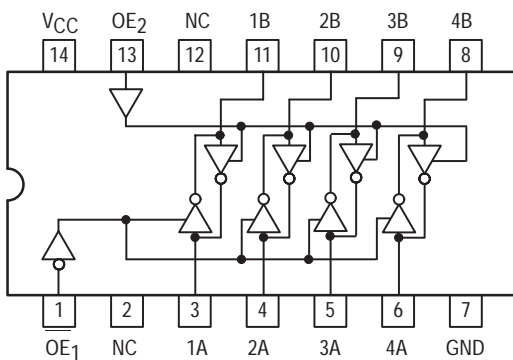


QUAD BUS TRANCEIVERS WITH 3-STATE OUTPUTS

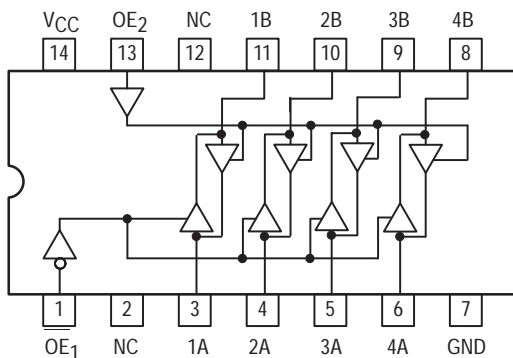
The MC54/74F242 and MC54/74F243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communication between data buses.

- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 4000 Volts

MC54/74F242 (TOP VIEW)



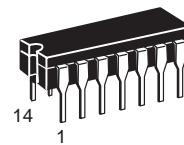
MC54/74F243 (TOP VIEW)



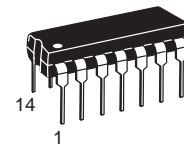
**MC54/74F242
MC54/74F243**

**QUAD BUS TRANCEIVERS
WITH 3-STATE OUTPUTS**

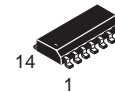
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-12	mA
		74			-15	
I _{OL}	Output Current — Low	54			48	mA
		74			64	

MC54/74F242 • MC54/74F243

FUNCTION TABLE – MC54/74F242

Inputs		Output	Inputs		Output
OE ₁	D		OE ₂	D	
L	L	H	L	X	Z
L	H	L	L	X	Z
H	X	Z	H	L	H
H	X	Z	H	H	L

FUNCTION TABLE – MC54/74F243

Inputs		Output	Inputs		Output
OE ₁	D		OE ₂	D	
L	L	L	L	X	Z
L	H	H	L	X	Z
H	X	Z	H	L	L
H	X	Z	H	H	H

H = HIGH Voltage Level; L = LOW Voltage Level ; X = Don't Care; Z = HIGH Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54	2.0		V	I _{OH} = -12 mA	V _{CC} = 4.50 V
		74	2.0		V	I _{OH} = -15 mA	V _{CC} = 4.50 V
		54, 74	2.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	54		0.55	V	I _{OL} = 48 mA	V _{CC} = MIN
		74		0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH			70	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
				1.0	mA	V _{OUT} = 5.5 V	
I _{OZL}	Output Off Current LOW			-1.6	mA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current	Enable		20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
		Data		70	μA	V _{IN} = 2.7 V	
		Data		1.0	mA	V _{IN} = 5.5 V	
		Enable		0.1	mA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	Enable		-1.0	mA	V _{IN} = 0.5 V	V _{CC} = MAX
		Data		-1.6	mA	V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)	74	-100	-225	mA	V _{OUT} = 0 V	V _{CC} = MAX
		54	-100	-275	mA		
I _{CCH}	Power Supply Current HIGH	F242		60	mA	Outputs	V _{CC} = MAX
		F243		80	mA	HIGH	
I _{CCL}	Power Supply Current LOW	F242		75	mA	Outputs	V _{CC} = MAX
		F243		90	mA	LOW	
I _{CCZ}	Power Supply Current OFF	F242		75	mA	Outputs	V _{CC} = MAX
		F243		90	mA	OFF	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F242 • MC54/74F243

AC CHARACTERISTICS – MC54/74F242

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay,	2.5	7.0	2.5	9.0	2.5	8.0	ns
t _{PHL}	Data to Output	1.5	4.7	1.5	6.0	1.5	5.7	
t _{PZH}	Output Enable Time	2.0	4.7	2.0	6.5	2.0	5.7	ns
t _{PZL}		4.0	9.0	4.0	12	4.0	10	
t _{PHZ}	Output Disable Time	2.0	5.3	2.0	6.5	2.0	6.3	ns
t _{PLZ}		1.5	6.5	1.5	12.5	1.5	8.0	

AC CHARACTERISTICS – MC54/74F243

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay,	2.5	5.2	2.0	6.5	2.0	6.2	ns
t _{PHL}	Data to Output	2.5	5.2	2.0	8.5	2.0	6.5	
t _{PZH}	Output Enable Time	2.0	5.7	2.0	8.0	2.0	6.7	ns
t _{PZL}		2.0	7.5	2.0	10.5	2.0	8.5	
t _{PHZ}	Output Disable Time	2.0	6.0	1.5	7.5	1.5	7.0	ns
t _{PLZ}		1.5	6.5	2.0	12.5	1.5	7.5	

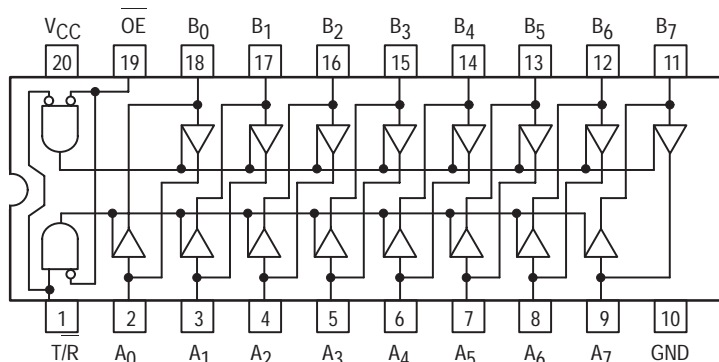


OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

The MC54/74F245 contains eight noninverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-Z condition.

- Noninverting Buffers
- Bidirectional Data Path
- B Outputs Sink 64 mA
- ESD > 4000 Volts

CONNECTION DIAGRAM (TOP VIEW)



FUNCTION TABLE

Inputs		Output
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

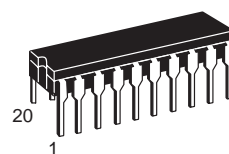
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	A _n Outputs	54, 74		-3.0	mA
			74		24	
I _{OL}	Output Current — Low	A _n Outputs	54		20	mA
			74			
I _{OH}	Output Current — High	B _n Outputs	54		-12	mA
			74		-15	
I _{OL}	Output Current — Low	B _n Outputs	54		48	mA
			74		64	

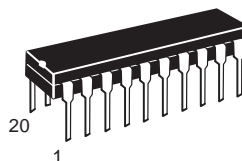
MC54/74F245

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

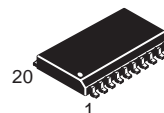
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

MC54/74F245

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V _{OH}	Output HIGH Voltage, A _n Outputs	54, 74	2.4	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V	
		74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V	
V _{OH}	Output HIGH Voltage, B _n Outputs	54, 74	2.4	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V	
		74	2.7	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V	
		54	2.0		V	I _{OH} = -12 mA	V _{CC} = 4.50 V	
		74	2.0		V	I _{OH} = -15 mA		
V _{OL}	Output LOW Voltage, A _n Outputs	54		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
		74		0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage, B _n Outputs	54			0.55	V	I _{OL} = 48 mA	V _{CC} = MIN
		74			0.55	V	I _{OL} = 64 mA	
I _{OZH} + I _{IH}	Output Off Current HIGH				70	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL} + I _{IL}	Output Off Current LOW				-650	mA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current	OE, T/R Inputs			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
		OE, T/R Inputs			100	μA	V _{IN} = 7.0 V	
		A _n , B _n Inputs			1.0	mA	V _{IN} = 5.5 V	
I _{IL}	Input LOW Current	T/R Input			-0.8	mA	V _{IN} = 0.5 V	V _{CC} = MAX
		OE Input			-1.2	mA		
I _{OS}	Output Short Circuit Current (Note 2)	A _n Outputs	-60		-150	mA	V _{OUT} = GND	V _{CC} = MAX
		B _n Outputs	-100		-225	mA	V _{OUT} = GND	V _{CC} = MAX
I _{CCH}	Power Supply Current HIGH				90	mA	V _{CC} = MAX, Outputs HIGH	
I _{CCL}	Power Supply Current LOW				120	mA	V _{CC} = MAX, Outputs LOW	
I _{CCZ}	Power Supply Current OFF				110	mA	V _{CC} = MAX, Outputs OFF	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to +70°C		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	6.0	2.5	8.0	2.5	7.0	ns
t _{PHL}	A _n to B _n or B _n to A _n	2.5	6.0	2.5	8.0	2.5	7.0	
t _{PZH}	Output Enable Time	3.0	7.0	3.0	9.0	3.0	8.0	ns
t _{PZL}		3.5	8.0	3.5	10	3.5	9.0	
t _{PHZ}	Output Disable Time	2.5	6.5	2.5	8.5	2.5	7.5	ns
t _{PLZ}		2.0	6.5	2.0	8.5	2.0	7.5	



8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74F251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Multifunctional Capacity
- On-Chip Select Logic Decoding
- Inverting and Noninverting 3-State Outputs

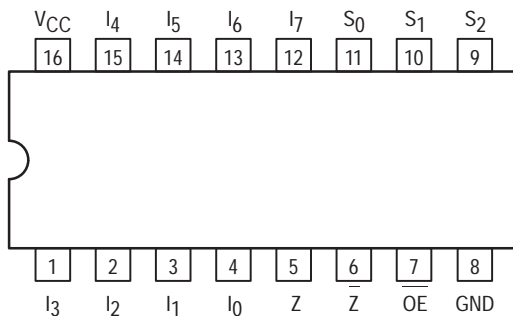
FUNCTIONAL DESCRIPTION

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both assertion and negation outputs are provided. The Output Enable input (OE) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_3 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_4 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_5 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

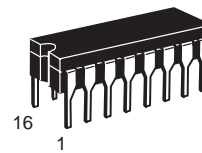
CONNECTION DIAGRAM



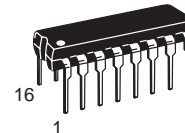
MC54/74F251

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

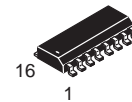
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-08



N SUFFIX
PLASTIC
CASE 648-08

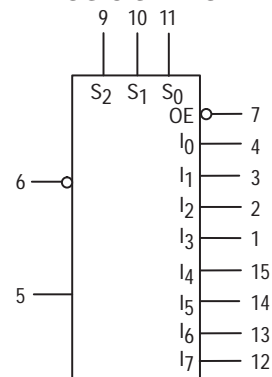


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

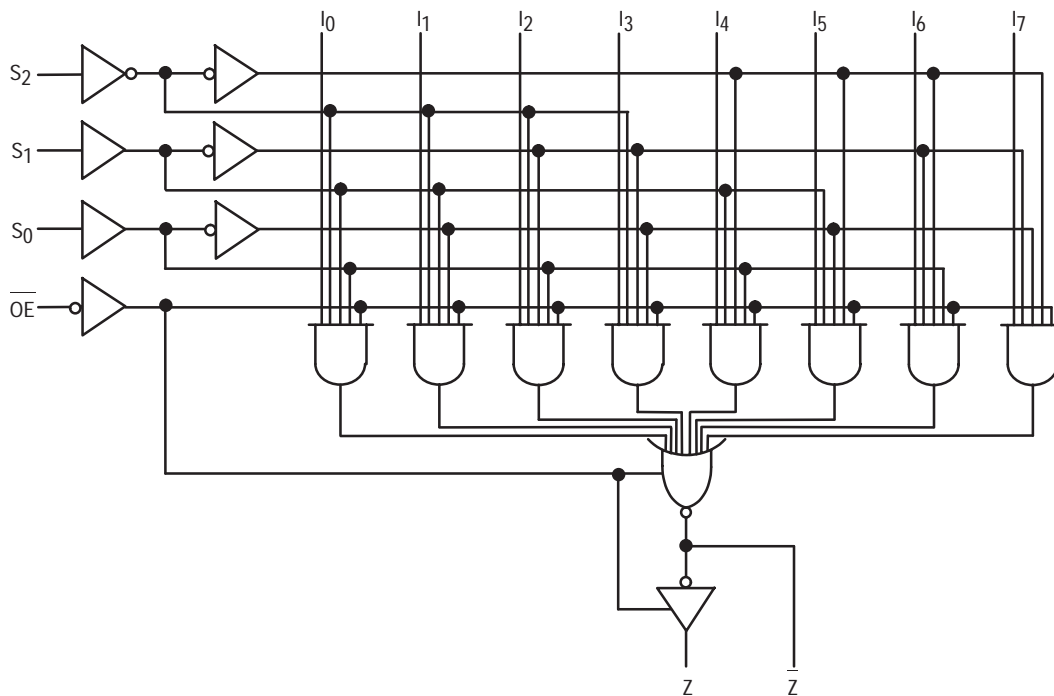
MC54/74F251

FUNCTION TABLE

Inputs				Outputs	
OE	S ₂	S ₁	S ₀	Z	Z
H	X	X	X	Z	Z
L	L	L	L	I ₀	I ₀
L	L	L	H	I ₁	I ₁
L	L	H	L	I ₂	I ₂
L	L	H	H	I ₃	I ₃
L	H	L	L	I ₄	I ₄
L	H	L	H	I ₅	I ₅
L	H	H	L	I ₆	I ₆
L	H	H	H	I ₇	I ₇

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

MC54/74F251

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output Off Current — HIGH				50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output Off Current — LOW				-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current			15	22	mA	I _{IN} , S _n = 4.5 V OE = GND	V _{CC} = MAX
				16	24	mA	OE, I _n = 4.5 V	V _{CC} = MAX

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

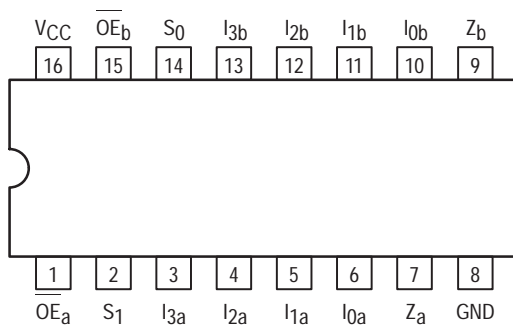
Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 °C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.0	8.0	3.5	9.5	4.0	9.0	ns
t _{PHL}	S _n to Z _n	3.2	7.5	3.2	9.5	3.2	8.5	
t _{PLH}	Propagation Delay	4.5	13	3.5	16.5	4.5	14	ns
t _{PHL}	S _n to Z _n	4.5	9.0	3.0	10.5	4.0	10.5	
t _{PLH}	Propagation Delay	3.0	5.7	2.5	8.0	3.0	7.0	ns
t _{PHL}	I _n to Z _n	1.5	4.0	1.5	6.0	1.5	5.0	
t _{PLH}	Propagation Delay	4.0	9.5	3.5	11.5	4.0	10.5	ns
t _{PHL}	I _n to Z	3.0	6.5	3.0	7.5	3.0	7.5	
t _{PZH}	Output Enable Time	3.0	7.0	3.0	9.5	3.0	8.0	ns
t _{PZL}	OE to Z _n	3.0	8.5	3.0	10.5	3.0	9.5	
t _{PHZ}	Output Disable Time	3.0	6.5	3.0	8.5	3.0	7.5	ns
t _{PLZ}	OE to Z _n	2.0	4.5	2.0	8.0	2.0	5.5	
t _{PZH}	Output Enable Time	4.0	9.0	4.0	10	4.0	10	ns
t _{PZL}	OE to Z	3.5	8.0	3.5	10	3.5	9.0	
t _{PHZ}	Output Disable Time	3.0	6.0	3.0	7.0	3.0	7.0	ns
t _{PLZ}	OE to Z	2.0	4.5	2.0	8.0	2.0	5.5	



DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74F253 is a Dual 4-Input Multiplexer with 3-State Outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus-oriented systems.

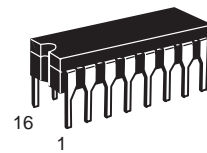
CONNECTION DIAGRAM DIP (TOP VIEW)



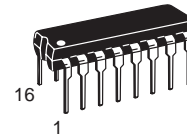
MC54/74F253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

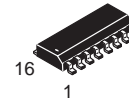
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

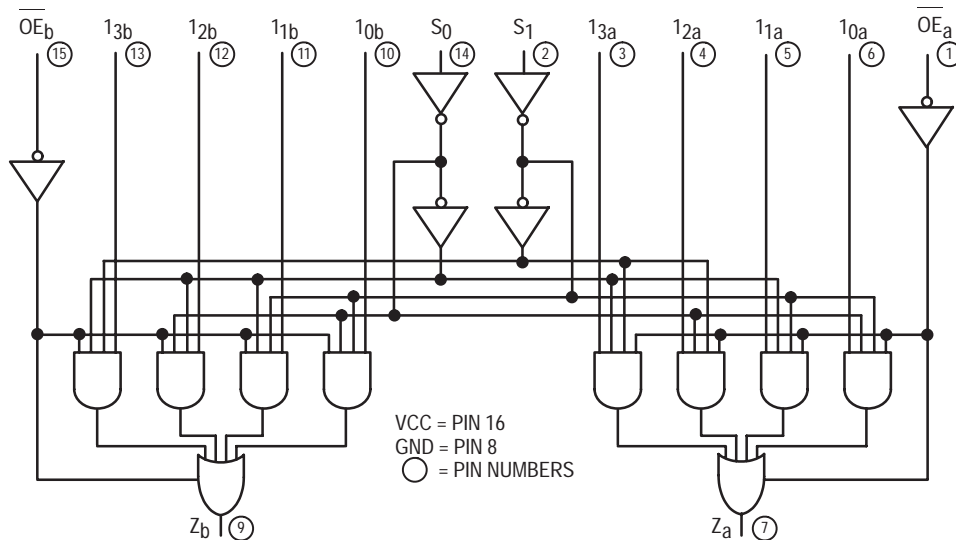
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

MC54/74F253

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-input Multiplexers with 3-State Outputs. They select two bits from four sources selected by common Select Inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable (OE_a , OE_b) inputs which, when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE_a} \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot \underline{S_1} \cdot \underline{S_0} + I_{3a} \cdot \underline{S_1} \cdot S_0)$$

$$Z_b = OE_b \cdot (I_{0b} \cdot S_1 \cdot \underline{S_0} + I_{1b} \cdot S_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot \overline{S_0})$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

FUNCTION TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	OE	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

MC54/74F253

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output Off Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output Off Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current				mA	OE _n = GND	
	Total, Output HIGH			16		I _O = 4.5 V; S _n , I ₁ - I ₃ = GND	
	Total, Output LOW			23		I _n , S _n , OE _n = GND V _{CC} = MAX	
	Total at HIGH-Z			23		OE _n = 4.5 V, V _{CC} = MAX I _n , S _n = GND	

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C		T _A = -55°C to +125°C		T _A = 0°C to +70°C		
		V _{CC} = +5.0 V		V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
C _L = 50 pF		C _L = 50 pF		C _L = 50 pF				
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.5	11.5	3.5	15	4.5	13.5	ns
t _{PHL}	S _n to Z _n	3.0	9.0	2.5	11	3.0	10	
t _{PLH}	Propagation Delay	3.0	7.0	2.5	9.0	3.0	8.0	ns
t _{PHL}	I _n to Z _n	2.5	6.0	2.5	8.0	2.5	7.0	
t _{PZH}	Output Enable Time	3.0	8.0	2.5	10	3.0	9.0	ns
t _{PZL}		3.0	8.0	2.5	10	3.0	9.0	
t _{PHZ}	Output Disable Time	2.0	5.0	2.0	6.5	2.0	6.0	ns
t _{PLZ}		2.0	6.0	2.0	8.0	2.0	7.0	



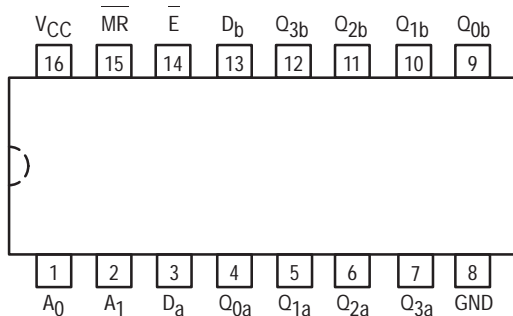
DUAL 4-BIT ADDRESSABLE LATCH

The MC54/74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode (MR = E = LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

- Combines Dual Demultiplexer and 8-Bit Latch
- Serial-to-Parallel Capability
- Output from Each Storage Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Common Clear Input
- Useful as Dual 1-of-4 Active HIGH Decoder

CONNECTION DIAGRAM



FUNCTION TABLE

Operating Mode	Inputs					Outputs			
	MR	E	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
Master Reset	L	H	X	X	X	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	Q=d	L	L	L
	L	L	d	H	L	L	Q=d	L	L
	L	L	d	L	H	L	L	Q=d	L
Store (Do Nothing)	L	L	d	H	H	L	L	L	Q=d
	H	H	X	X	X	q ₀	q ₁	q ₂	q ₃
Addressable Latch	H	L	d	L	L	Q=d	q ₁	q ₂	q ₃
	H	L	d	H	L	q ₀	Q=d	q ₂	q ₃
	H	L	d	L	H	q ₀	q ₁	Q=d	q ₃
	H	L	d	H	H	q ₀	q ₁	q ₂	Q=d

H = HIGH Voltage Level Steady State

L = LOW Voltage Level Steady State

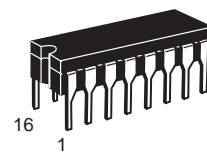
X = Immaterial

d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition.

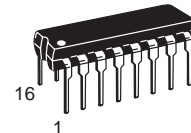
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

MC54/74F256

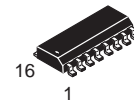
DUAL 4-BIT ADDRESSABLE LATCH
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

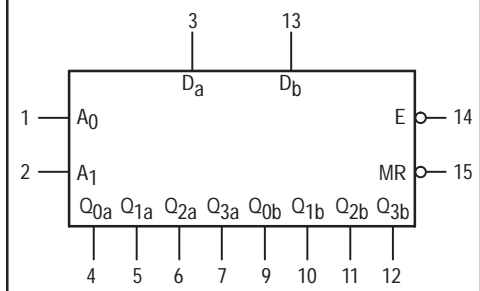


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

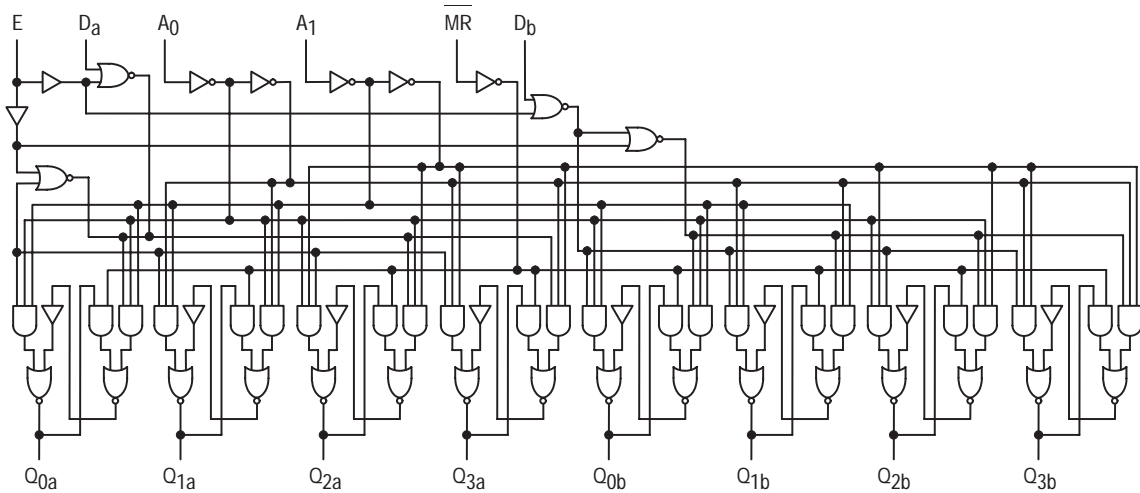
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F256

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F256

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OL} = -1.0 mA, V _{CC} = MIN
		74	2.7		V	I _{OL} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			42	mA	V _{CC} = MAX
				60	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F256

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to 70°C V _{CC} = 5.0 V ± 5% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay E to Q _n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay D _n to Q _n	3.5 3.0	9.0 7.0	3.5 2.5	11.5 8.5	3.5 2.5	10 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _n to Q _n	3.5 4.0	14 9.5	3.5 4.0	15.5 11	3.5 4.0	14.5 10	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	9.0	4.5	11.5	4.5	10	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V		T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		T _A = 0 to 70°C V _{CC} = 5.0 V ± 5%		
		Min	Max	Min	Max	Min	Max	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to E	4.0 4.0		5.0 5.0		4.0 4.0		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW D _n to E	2.0 2.0		2.0 2.0		2.0 2.0		ns
t _S (H) t _S (L)	Setup Time, HIGH or LOW A to E(a)	4.0 4.0		4.0 4.0		4.0 4.0		ns
t _H (H) t _H (L)	Hold Time HIGH or LOW A to E(b)	0 0		0 0		0 0		ns
t _W	E Pulse Width	4.0		4.0		4.0		ns
t _W	MR Pulse Width	4.0		4.0		4.0		ns

NOTES:

1. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

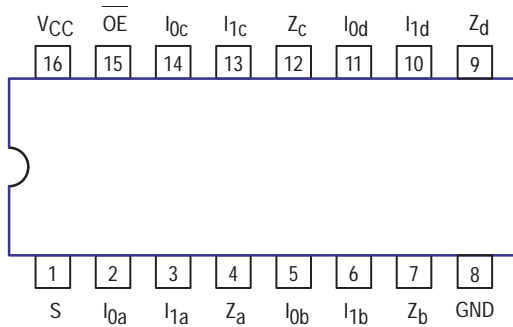


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

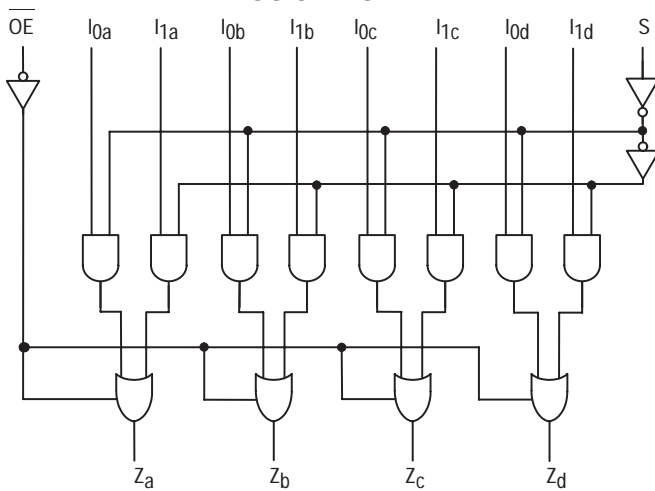
The MC74F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects
- AC Enhanced Version of the F257

CONNECTION DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

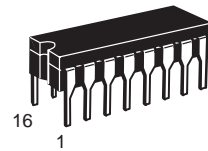
Output Enable	Select Input	Data Inputs		Outputs
OE	S	I ₀	I ₁	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

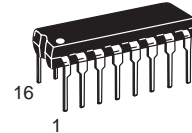
MC74F257A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

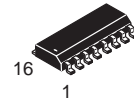
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

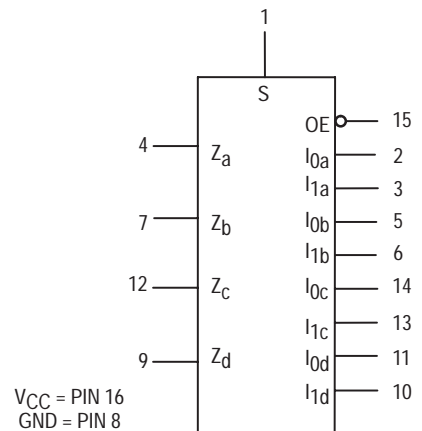


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

MC54FXXXAJ Ceramic
 MC74FXXXAN Plastic
 MC74FXXXAD SOIC

LOGIC SYMBOL



MC74F257A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			–3.0	mA
I _{OL}	Output Current — Low	74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			–1.2	V	I _{IN} = –18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.4	3.3	V	I _{OH} = –3.0 mA	V _{CC} = 4.50 V
		74	2.7	3.3	V	I _{OH} = –3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			–50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			–0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	–60		–150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current		9.0	15	mA	S, I _{1x} = 4.5 V OE, I _{0x} = GND	V _{CC} = MAX
I _{CCL}			14.5	22		I _{1x} = 4.5 V OE, I _{0x} , S = GND	
I _{CCZ}			15	23		S, I _{0x} = GND OE, I _{1x} = 4.5 V	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The F257A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

$$Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$Z_d = OE \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable input (OE) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

MC74F257A

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	1.5	5.5	1.5	6.0	ns
t _{PHL}	I _n to Z _n	2.0	5.5	2.0	6.0	
t _{PLH}	Propagation Delay	3.0	9.5	3.0	10.5	ns
t _{PHL}	S to Z _n	2.5	7.0	2.5	8.0	
t _{PZH}	Output Enable Time	2.0	6.5	2.0	7.0	ns
t _{PZL}		2.5	7.0	2.5	8.0	
t _{PHZ}	Output Disable Time	2.0	6.0	2.0	7.0	ns
t _{PLZ}		2.0	6.0	2.0	7.0	

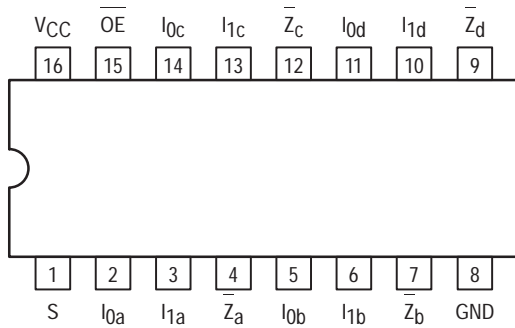


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

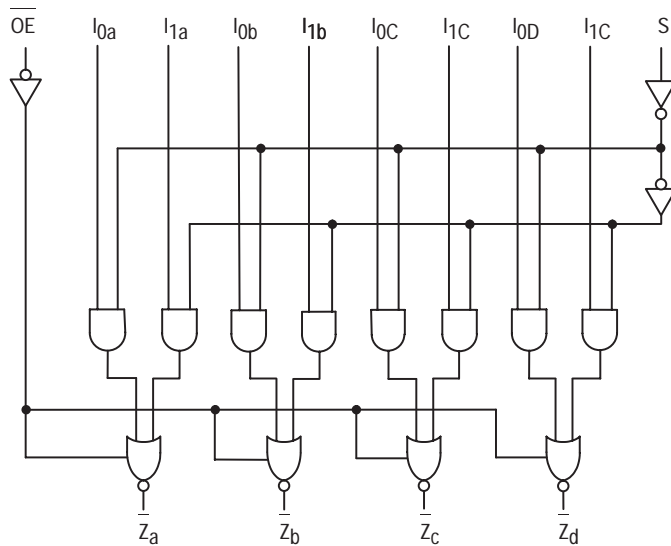
The MC74F258A is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common Data Select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs
- AC Enhanced Version of the F258

CONNECTION DIAGRAM (TOP VIEW)



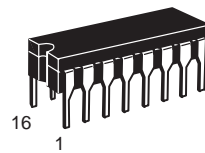
LOGIC DIAGRAM



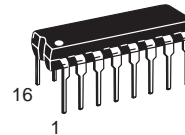
MC74F258A

QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

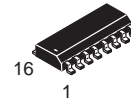
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

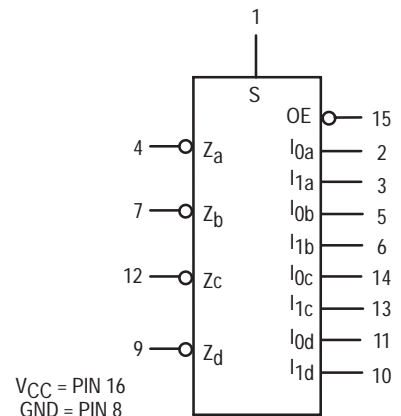


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXAJ Ceramic
MC74FXXXAN Plastic
MC74FXXXAD SOIC

LOGIC SYMBOL



MC74F258A

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
OE	S	I ₀	I ₁	Z
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-3.0	mA
I _{OL}	Output Current — Low	74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
		74	2.4				V _{CC} = MIN
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current		6.2	9.5	mA	S, I _{1X} = 4.5 V OE, I _{0X} = GND	V _{CC} = MAX
I _{CCL}			15.1	23		I _{1X} = 4.5 V OE, I _{0X} , S = GND	
I _{CCZ}			11.3	17		S, I _{0X} = GND OE, I _{1X} = 4.5 V	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F258A

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	5.3	2.0	6.0	ns
t _{PHL}	I _n to \bar{Z}_n	1.0	4.0	1.0	5.0	
t _{PLH}	Propagation Delay	3.0	7.5	3.0	8.5	ns
t _{PHL}	S to \bar{Z}_n	2.5	7.0	2.5	8.0	
t _{PZH}	Output Enable Time	2.0	6.0	2.0	7.0	ns
t _{PZL}		2.5	7.0	2.5	8.0	
t _{PHZ}	Output Disable Time	2.0	6.0	2.0	7.0	ns
t _{PLZ}		1.5	6.0	1.5	7.0	

FUNCTIONAL DESCRIPTION

The F258A is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{aligned}\bar{Z}_a &= \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Z}_b &= \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Z}_c &= \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Z}_d &= \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})\end{aligned}$$

When the Output Enable input (OE) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.



8-BIT ADDRESSABLE LATCH

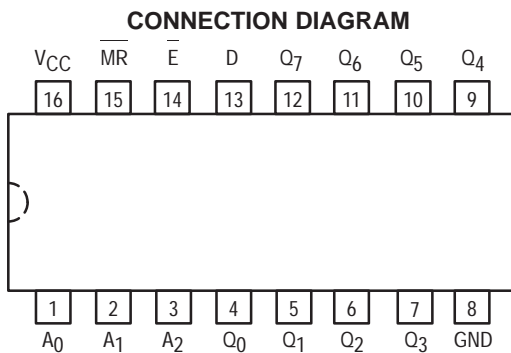
The MC54/74F259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

FUNCTIONAL DESCRIPTION

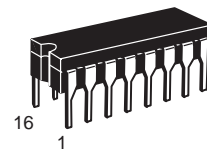
The MC54/74F259 has four modes of operation as shown in the Mode Select Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All the latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC54/74F259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the MC54/74F259.

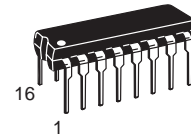


MC54/74F259

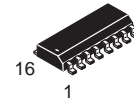
8-BIT ADDRESSABLE LATCH FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

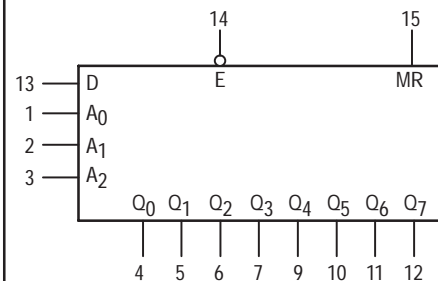


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

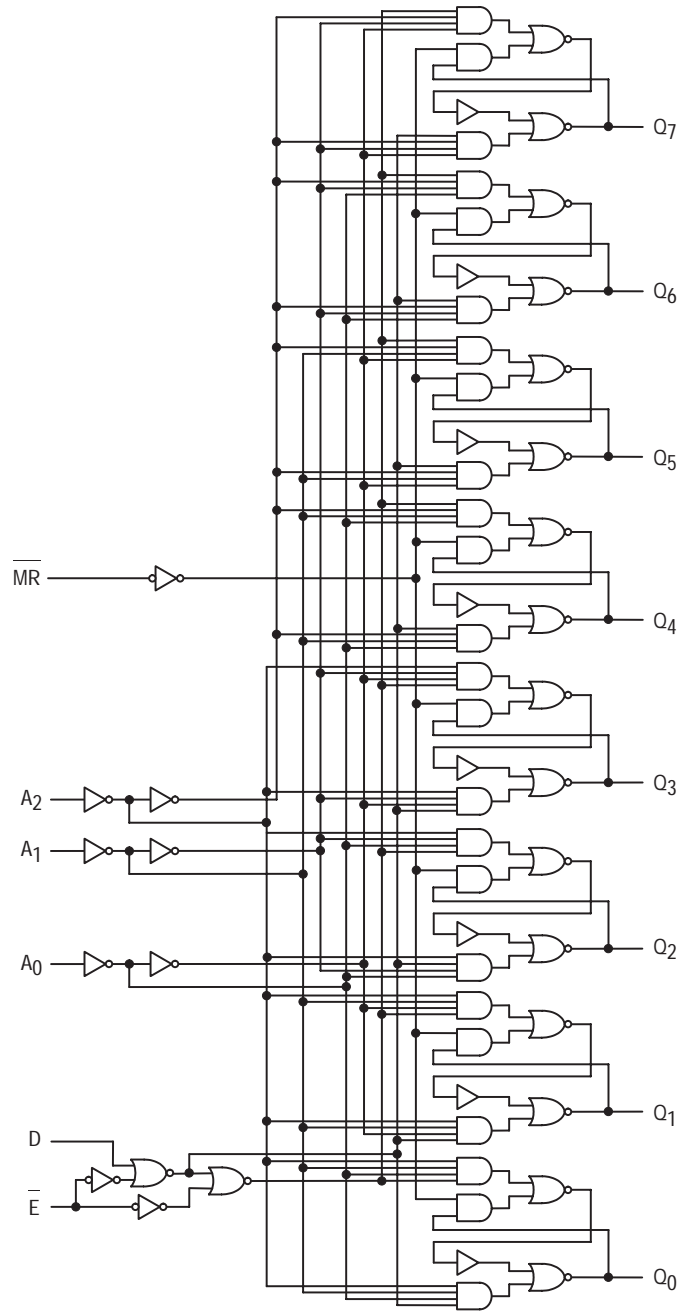
LOGIC SYMBOL



MC54/74F259

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F259

MODE SELECT TABLE

E	MR	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level

L = LOW Voltage Level

FUNCTION TABLE

Operating Mode	Inputs						Outputs							
	MR	E	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
L	L	d	H	H	H	L	L	L	L	L	L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable Latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d	

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition.

q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

MC54/74F259

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OL} = -1.0 mA, V _{CC} = MIN
		74	2.7		V	I _{OL} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			46	mA	V _{CC} = MAX
				75	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 to + 125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to + 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay E to Q _n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.0	ns
t _{PLH} t _{PHL}	Propagation Delay D _n to Q _n	3.5 3.0	9.0 6.5	3.5 2.5	11.5 8.5	3.5 2.5	10 7.0	ns
t _{PLH} t _{PHL}	Propagation Delay A _n to Q _n	3.5 4.0	13 9.0	3.5 4.0	15.5 11	3.5 4.0	14.5 9.5	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	9.0	4.5	11.5	4.5	10	ns

MC54/74F259

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0 \pm 10\%$		$T_A = 0\text{ to }+70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Max	Min	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW D_n to E	4.0 4.0		5.0 5.0		4.0 4.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW D_n to E	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW A to E(a)	4.0 4.0		4.0 4.0		4.0 4.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW A to E(b)	0 0		0 0		0 0		ns
t_W	E Pulse Width	4.0		4.0		4.0		ns
t_W	MR Pulse Width	4.0		4.0		4.0		ns

- a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

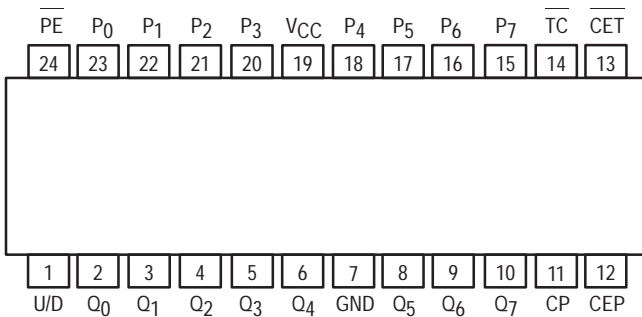


8-BIT BIDIRECTIONAL BINARY COUNTER

The MC74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

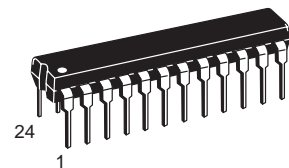
- Synchronous Counting and Loading
- Built-In Lookahead Carry Capability
- Count Frequency 115 MHz Typical
- Supply Current 95 mA Typical

PIN ASSIGNMENT

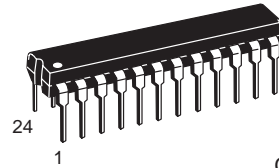


MC74F269

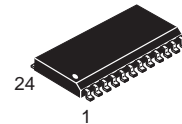
8-BIT BIDIRECTIONAL BINARY COUNTER FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	74	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0	mA
I _{OL}	Output Current — Low	74			20	mA

MC74F269

FUNCTION TABLE

Operating Mode	Inputs						Outputs	
	CP	U/D	CEP	CET	PE	P _n	Q _n	TC
Parallel Load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold Do Nothing	↑	X	h	X	h	X	q _n	(a)
	↑	X	X	h	h	X	q _n	H

H = HIGH voltage level steady state

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level steady state

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

X = Don't care

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

(a) = The TC is LOW when CET is LOW and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs HIGH and Terminal Count Down is with all Q_n outputs LOW.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

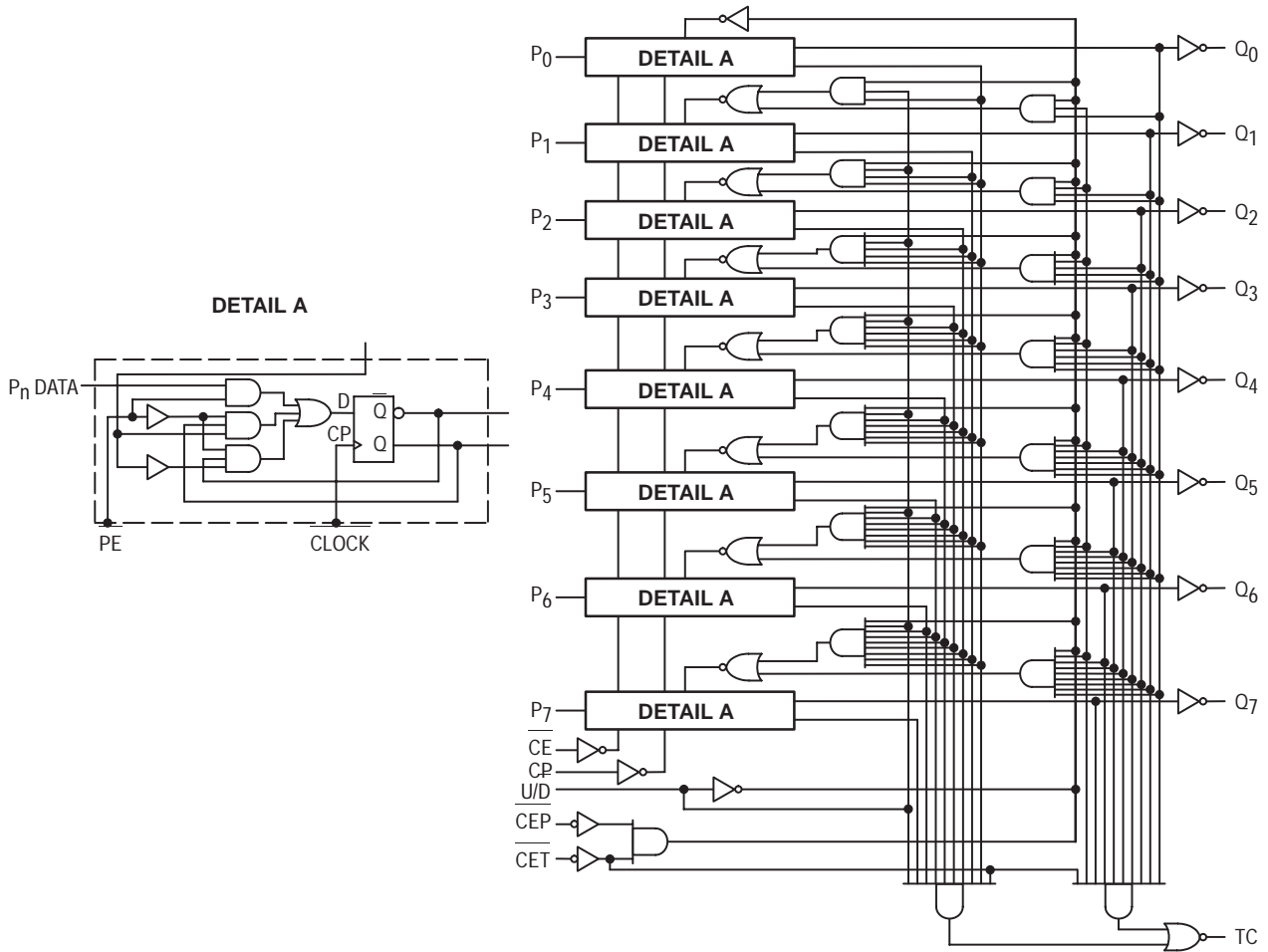
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{OH}	Output HIGH Voltage	74	2.5			V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
			2.7	3.4				V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = 4.5 V	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{IH}	Input HIGH Current				100	μA	V _{CC} = MAX	V _{IN} = 7.0 V
					20			V _{IN} = 2.7 V
I _{IL}	Input LOW Current				-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Total Supply Current (total)		I _{CCH}	93	120	mA	V _{CC} = MAX	(Note 3)
			I _{CCL}		98			125

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.
- PE = CET = CEP = U/D = GND; P_n = 4.5 V; CP = ↑
- PE = CET = CEP = U/D = GND; CP = ↑

MC74F269

LOGIC DIAGRAM



MC74F269

AC ELECTRICAL CHARACTERISTICS

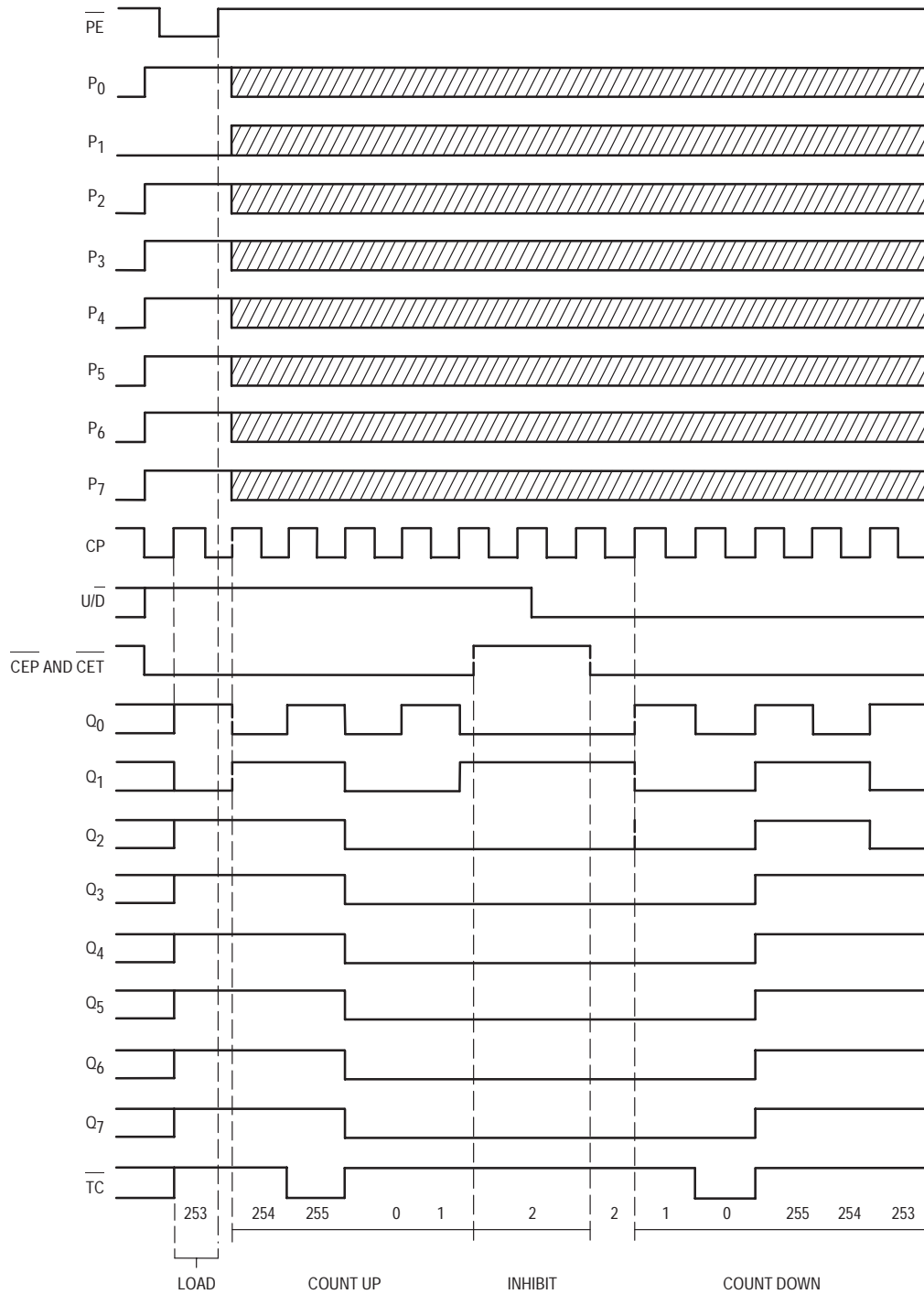
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100			85		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n (Load) PE = LOW	3.0 4.0	5.5 5.0	9.0 9.0	3.0 4.0	9.5 9.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n (Count) PE = HIGH	3.0 4.5	6.0 7.0	9.0 10	2.5 4.5	10 10.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to TC	4.5 5.0	7.5 7.5	10 10	4.5 5.0	10.5 11	ns
t _{PLH} t _{PHL}	Propagation Delay CET to TC	3.5 3.5	5.0 5.5	9.0 9.0	3.5 3.5	10 10	ns
t _{PLH} t _{PHL}	Propagation Delay U/D to TC	4.0 4.5	6.0 5.5	9.0 9.5	4.0 4.5	10 10	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _S (H) t _S (L)	Set-up Time, HIGH or LOW P to CP	2.0 2.0			2.5 2.5			ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW P to CP	1.0 1.0			1.0 1.0			ns
t _S (H) t _S (L)	Set-up Time, HIGH or LOW PE to CP	5.0 5.5			5.5 6.5			ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW PE to CP	0 0			0 0			ns
t _S (H) t _S (L)	Set-up Time, HIGH or LOW CET, CEP to CP	4.5 4.5			5.5 5.5			ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW CET, CEP to CP	0 0			0 0			ns
t _S (H) t _S (L)	Set-up Time, HIGH or LOW U/D to CP	6.0 7.0			7.0 8.0			ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW U/D to CP	0 0			0 0			ns
t _W (H) t _W (L)	Clock Pulse Width CP	4.0 4.5			4.0 5.0			ns

MC74F269

TIMING DIAGRAM

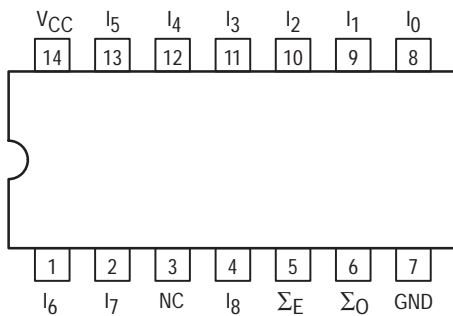




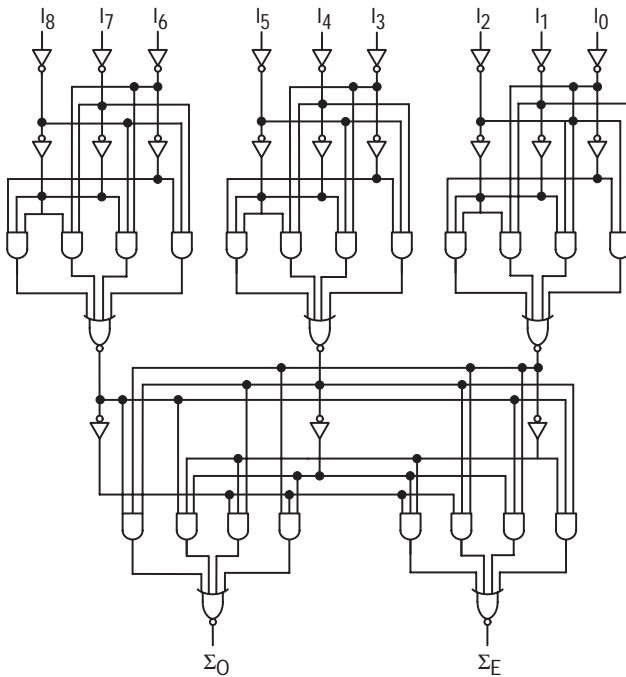
9-BIT PARITY GENERATOR/ CHECKER

The MC54/74F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

CONNECTION DIAGRAM



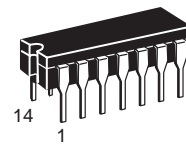
LOGIC DIAGRAM



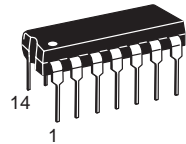
NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F280

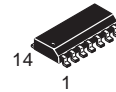
**9-BIT PARITY
GENERATOR/CHECKER**
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**

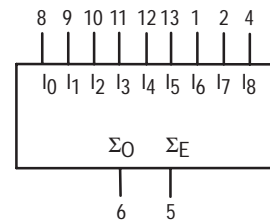


**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

MC54/74F280

FUNCTION TABLE

Number of HIGH Inputs I_0-I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level; L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ MA}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$
		74	2.7	3.4	V	$I_{OH} = 1.0 \text{ mA}$ $V_{CC} = 4.75 \text{ V}$
V_{OL}	Output Low Voltage		0.35	0.5	V	$I_{OL} = 20 \text{ mA}$ $V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				100	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5 \text{ V}$
I_{OS}	Short Circuit Current (Note 2)	-60		-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current		25	38	mA	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F280

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.5	15	4.5	20	4.5	16	ns
t _{PHL}	I _n to ΣE	4.5	16	4.5	21	4.5	17	
t _{PLH}	Propagation Delay	4.5	15	4.5	20	4.5	16	ns
t _{PHL}	I _n to ΣO	4.5	16	4.5	21	4.5	17	



4-BIT BINARY FULL ADDER (With Fast Carry)

The MC54/74F283 high-speed 4-bit binary full adder with internal carry lookahead, accepts two 4-bit binary words (A_0 – A_3 , B_0 – B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0 – S_3) and the Carry output (C_4) from the most significant bit. The F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

FUNCTIONAL DESCRIPTION

The F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0 . The binary sum appears on the Sum (S_0 – S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

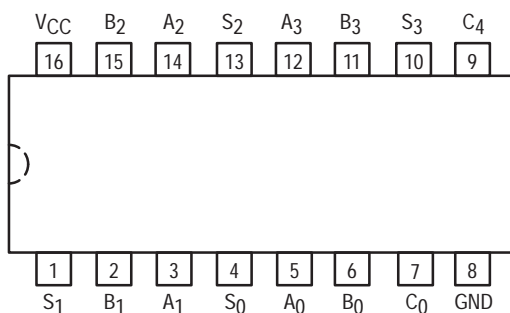
$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0 , A_0 , B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if C_0 is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3 , B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2 , B_2 , S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2 . Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2 . Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0 , S_1 and S_2 present a binary number equal to the number of inputs I_1 – I_5 that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1 – I_5 are true, the output M_5 is true.

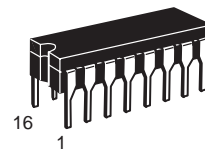
CONNECTION DIAGRAM



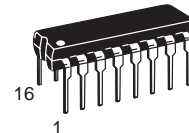
MC54/74F283

4-BIT BINARY FULL ADDER (With Fast Carry)

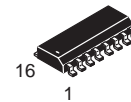
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

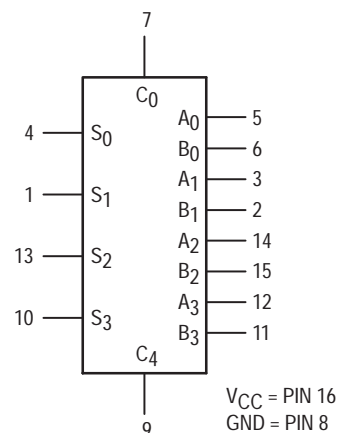


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

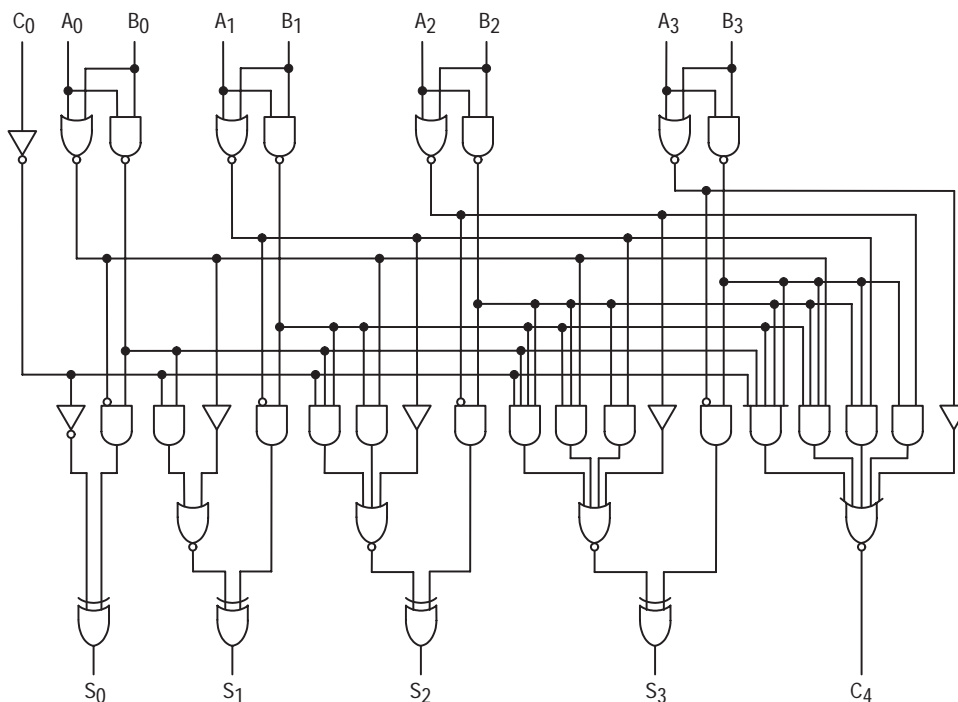
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



MC54/74F283

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74	—	—	-1.0	mA
I _{OL}	Output Current — Low	54, 74	—	—	20	mA

Figure A. Active-HIGH versus Active-LOW Interpretation

	C ₀	A ₀	A ₁	A ₂	A ₃	B ₀	B ₁	B ₂	B ₃	S ₀	S ₁	S ₂	S ₃	C ₄
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

MC54/74F283

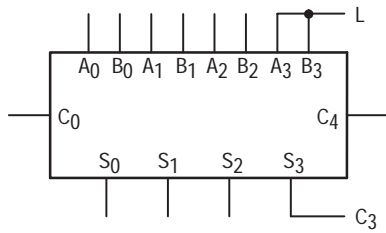


Figure B. 3-Bit Adder

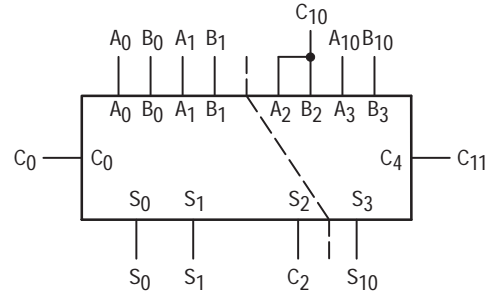


Figure C. 2-Bit and 1-Bit Adders

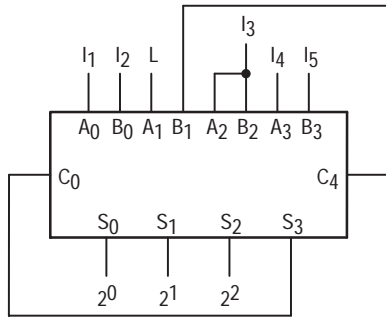


Figure D. 5-Input Encoder

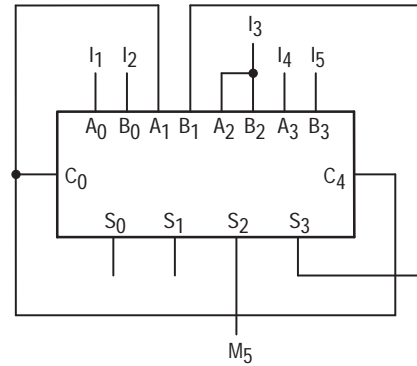


Figure E. 5-Input Majority Gate

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current C ₀ Input			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
	A and B Inputs			-1.2	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		36	55	mA	Inputs = 4.5 V	V _{CC} = MAX

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F283

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay C ₀ to S _n	3.5 4.0	7.0 7.0	9.5 9.5	3.5 4.0	14 14	3.5 4.0	10.5 10.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _n or B _n to S _n	3.0 3.5	7.0 7.0	9.5 9.5	3.0 3.5	14 14	3.0 3.5	10.5 10.5	ns
t _{PLH} t _{PHL}	Propagation Delay C ₀ to C ₄	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	10.5 10	3.5 3.0	8.5 8.0	ns
t _{PLH} t _{PHL}	Propagation A _n or B _n to C ₄	3.0 3.0	5.7 5.3	7.5 7.0	3.0 3.0	10.5 10	3.0 3.0	8.5 8.0	ns



8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

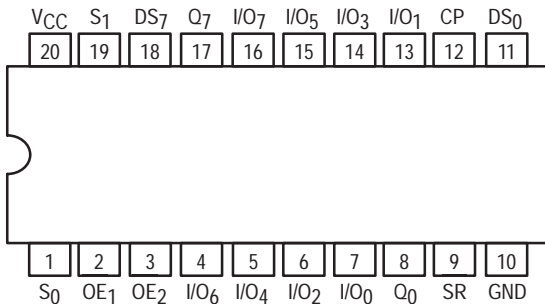
The MC74F323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the F299 with the exception of Synchronous Reset.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Four modes of operation are possible: hold (store), shift left, shift right and parallel load. All modes are activated on the LOW-to-HIGH transition of the clock.

- Common I/O For Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Parallel Load and Store
- Separate Continuous Inputs and Outputs from Q₀ and Q₇ Allow Easy Cascading
- Fully Synchronous Reset
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects

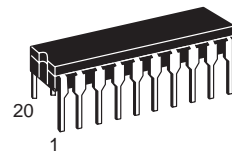
CONNECTION DIAGRAM



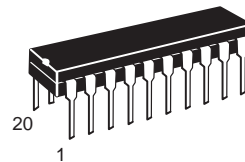
MC74F323

8-INPUT SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

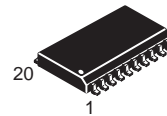
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			-1.0/-3.0	mA
I _{OL}	Output Current — Low	74			20/24	mA

MC74F323

FUNCTION TABLE

Inputs				Response
SR	S ₁	S ₀	CP	
L	X	X	↑	Synchronous Reset: Q ₀ –Q ₇ = LOW
H	H	H	↑	Parallel Load: I/O _n → Q _n
H	L	H	↑	Shift Right: DS ₀ → Q ₀ , Q ₀ → Q ₁ , etc.
H	H	L	↑	Shift Left: DS ₇ → Q ₇ , Q ₇ → Q ₆ , etc.
H	L	L	X	Hold

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↑ = LOW-to-HIGH clock transition.

FUNCTIONAL DESCRIPTION

The MC74F323 contains eight edge-triggered D-type flips-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q₀ and Q₇ are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on SR overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other

state changes are initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE₁ or OE₂ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S₀ and S₁ in preparation for a parallel load operation.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	Q ₀ /Q ₇	74	2.5		V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
			74	2.7				V _{CC} = 4.75 V
		I/O	74	2.7	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
			74	2.4				V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	Q ₀ /Q ₇			V	I _{OL} = 20 mA	V _{CC} = MIN	
		I/O						I _{OL} = 24 mA
I _{IH}	Input HIGH Current	Q ₀ /Q ₇			μA	V _{CC} = MAX, V _{IN} = 2.7 V		
		I/O						20
		Q ₀ /Q ₇			mA	V _{CC} = MAX	V _{IN} = 7.0 V	
		I/O					1.0	V _{IN} = 5.5 V
I _{IL}	Input LOW Current	S ₀ , S ₁			mA	V _{CC} = MAX, V _{IN} = 0.5 V		
		Other Inputs						-1.2
I _{OZH}	Off-State Output Current, High-Level Voltage Applied				70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V
					1.0			mA
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied				-0.6	mA	V _{CC} = MAX, V _{OUT} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)				-60	mA	V _{CC} = MAX	V _{OUT} = 0 V
I _{CC}	Total Supply Current				-150			95

NOTES:

- For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F323

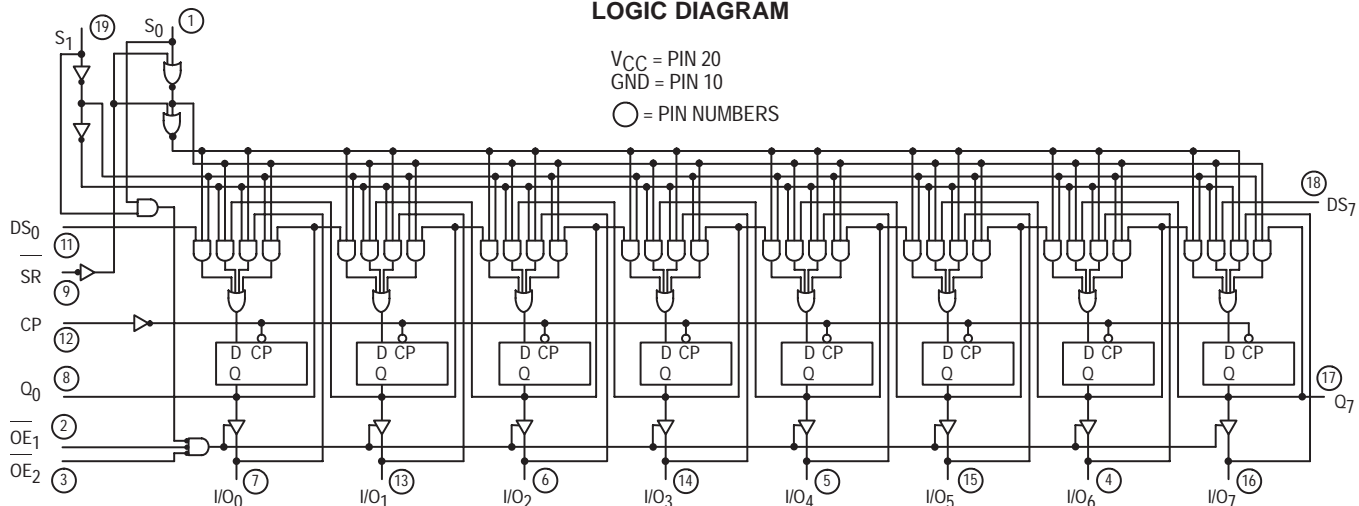
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
f _{MAX}	Maximum Input Frequency	70		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	3.5	9.0	3.5	10	ns
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	3.5	9.0	3.5	10	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	3.5	8.0	3.5	9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time to HIGH or LOW Level	2.0	6.0	2.0	7.0	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{s(H)} t _{s(L)}	Set-Up Time, HIGH or LOW S ₀ or S ₁ to CP	8.5			8.5		ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW S ₀ or S ₁ to CP	0.0			0.0		ns
t _{s(H)} t _{s(L)}	Set-Up Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0			5.0		ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	2.0			2.0		ns
t _{s(H)} t _{s(L)}	Set-Up Time, HIGH or LOW SR to CP	10			10		ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW SR to CP	0.0			0.0		ns
t _{w(H)} t _{w(L)}	CP Pulse Width, HIGH or LOW	7.0			7.0		ns

LOGIC DIAGRAM





4-BIT SHIFTER (With 3-State Outputs)

The MC54/74F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable (OE) inputs as a third Select level. With appropriate interconnections, the F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

- Linking Inputs for Word Expansion
- 3-State Outputs for Extending Shift Range

FUNCTIONAL DESCRIPTION

The F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 7-bit data word is introduced at the I_n inputs and is shifted according to the code applied to the select inputs S_0, S_1 . Outputs O_0-O_3 are 3-state, controlled by an active-LOW output enable (OE). When OE is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high-impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC EQUATIONS

$$O_0 = \overline{S_0} \overline{S_1} I_0 + S_0 \overline{S_1} I_{-1} + \overline{S_0} S_1 I_{-2} + S_0 S_1 I_{-3}$$

$$O_1 = \overline{S_0} \overline{S_1} I_1 + S_0 \overline{S_1} I_0 + \overline{S_0} S_1 I_{-1} + S_0 S_1 I_{-2}$$

$$O_2 = \overline{S_0} \overline{S_1} I_2 + S_0 \overline{S_1} I_1 + \overline{S_0} S_1 I_0 + S_0 S_1 I_{-1}$$

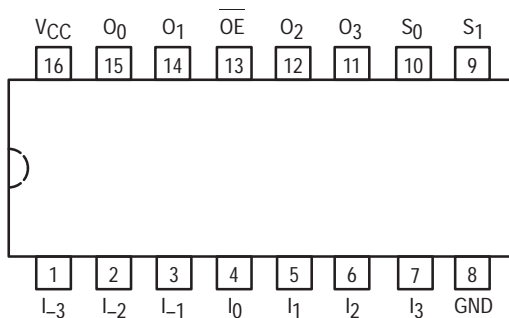
$$O_3 = S_0 S_1 I_3 + S_0 S_1 I_2 + S_0 S_1 I_1 + S_0 S_1 I_0$$

TRUTH TABLE

Inputs			Outputs			
OE	S_1	S_0	O_0	O_1	O_2	O_3
H	X	X	Z	Z	Z	Z
L	L	L	I_0	I_1	I_2	I_3
L	L	H	I_{-1}	I_0	I_1	I_2
L	H	L	I_{-2}	I_{-1}	I_0	I_1
L	H	H	I_{-3}	I_{-2}	I_{-1}	I_0

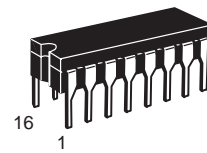
H = HIGH Voltage Level Z = High Impedance
L = LOW Voltage Level X = Immaterial

CONNECTION DIAGRAM

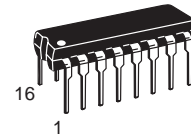


MC54/74F350

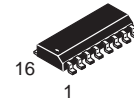
**4-BIT SHIFTER
(With 3-State Outputs)**
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

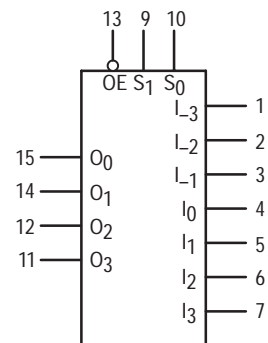


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

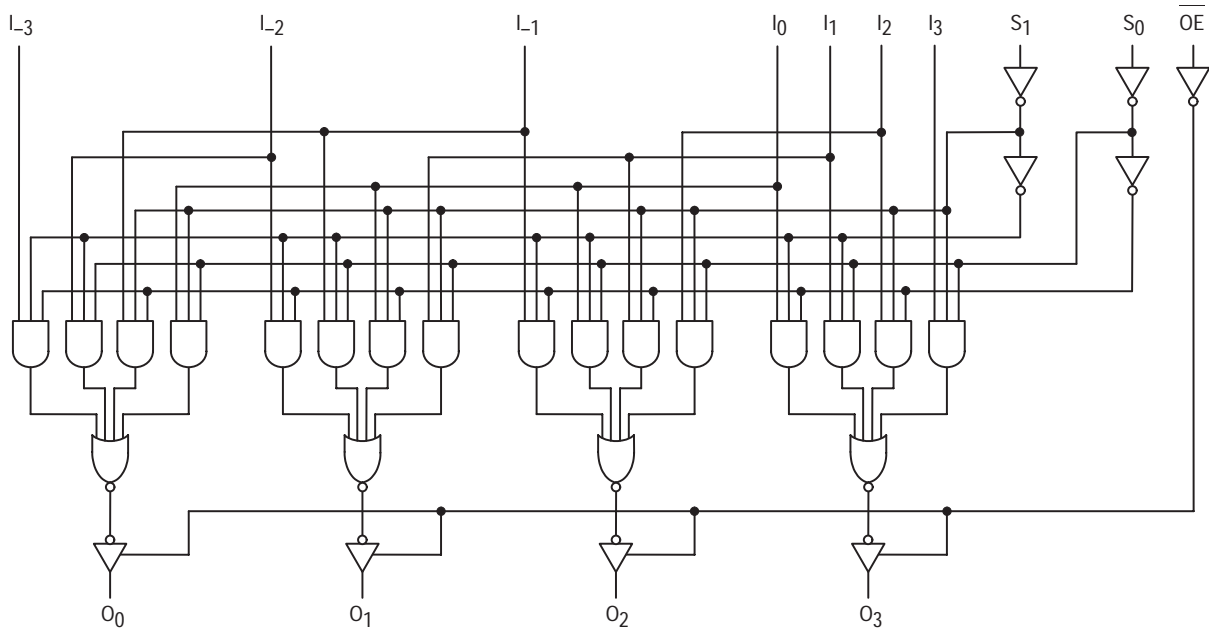
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MC54/74F350

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74	—	—	-3.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3	V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 24$ mA	$V_{CC} = \text{MIN}$
I_{OZH}	Output OFF Current — HIGH			50	μA	$V_{OUT} = 2.7$ V	$V_{CC} = \text{MAX}$
I_{OZL}	Output OFF Current — LOW			-50	μA	$V_{OUT} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7$ V	$V_{CC} = \text{MAX}$
				100		$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current			-1.2	mA	$V_{IN} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} = \text{MAX}$
I_{CCH}	Power Supply Current		22	35	mA	Outputs HIGH	$V_{CC} = \text{MAX}$
I_{CCL}			26	41		Outputs LOW	
I_{CCZ}			26	42		Outputs OFF	

NOTES: 1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.

2. Not more than one output should be shorted at a time, nor for more than 1 second.

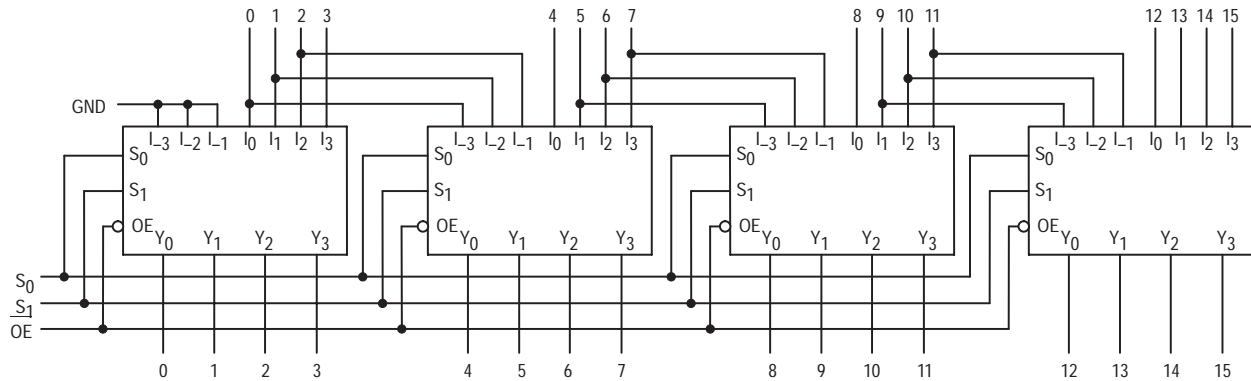
MC54/74F350

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0\text{ to }+70^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay I_n to O_n	3.0 2.5	6.0 5.5	3.0 2.5	7.5 7.0	3.0 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_n to O_n	4.0 3.0	10 8.5	4.0 3.0	13.5 10	4.0 3.0	11 9.5	ns
t_{PZH} t_{PZL}	Output Enable Time	2.5 4.0	7.0 9.0	2.5 4.0	10.5 11	2.5 4.0	8.0 10	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 1.5	5.5 5.5	2.0 1.5	7.0 9.0	2.0 1.5	6.5 6.5	ns

APPLICATIONS

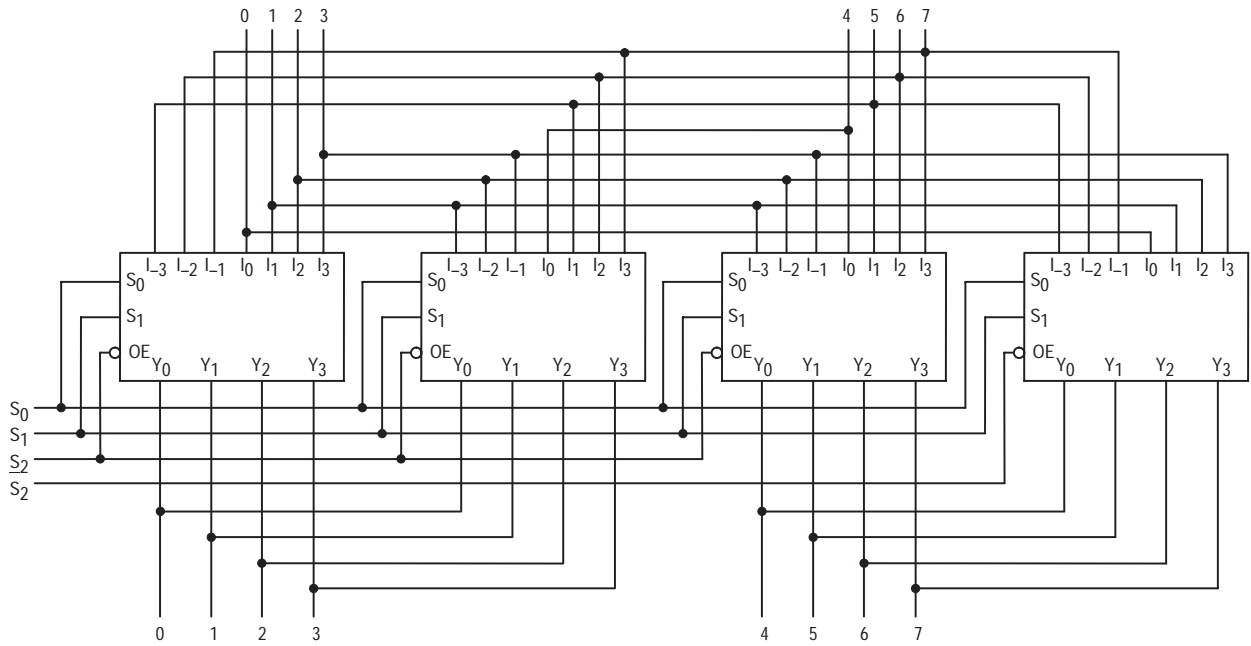
16-Bit Shift-Up 0 to 3 Pieces, Zero Backfill



S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

MC54/74F350

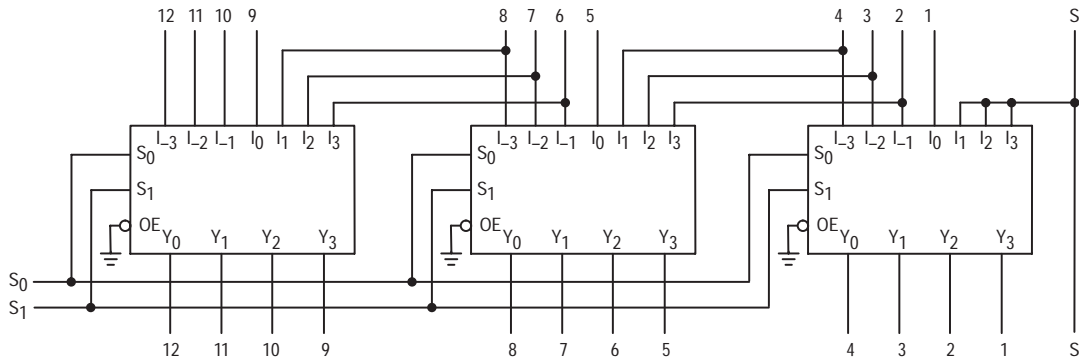
8-Bit End Around Shift 0 to 7 Pieces



S ₂	S ₁	S ₀	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4

S ₂	S ₁	S ₀	
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-Bit Twos Complement Scaler



S ₁	S ₀	SCALE
L	L ÷ 8	1/8
L	H ÷ 4	1/4
H	L ÷ 2	1/2
H	H NO CHANGE	1

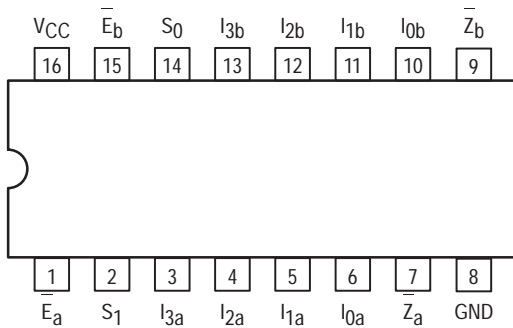


DUAL 4-INPUT MULTIPLEXER

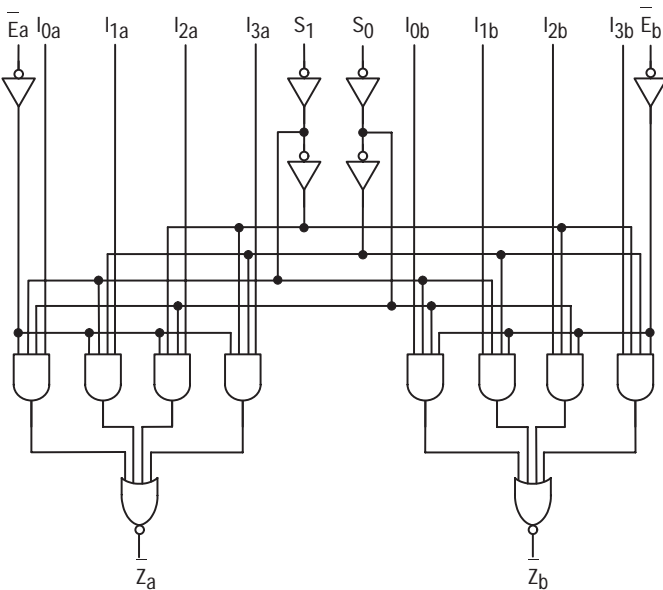
The MC54/74F352 is a very high speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The F352 is the functional equivalent of the F153 except with inverted outputs.

- Inverted Version of the F153
- Separate Enables for Each Multiplexer
- Input Clamp Diode Limits High-Speed Termination Effects

CONNECTION DIAGRAM (TOP VIEW)



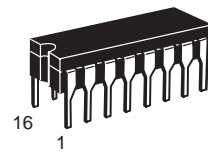
LOGIC DIAGRAM



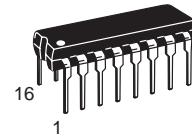
MC54/74F352

DUAL 4-INPUT MULTIPLEXER

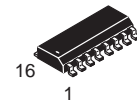
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

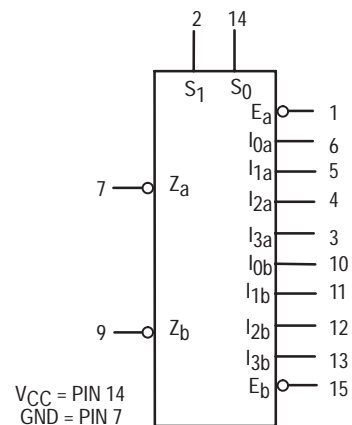


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



MC54/74F352

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	- 55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

FUNCTIONAL DESCRIPTION

The F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active-LOW Enables (E_a, E_b) which can be used to strobe the outputs independently. When the Enables (E_a, E_b) are HIGH, the corresponding outputs (Z_a, Z_b) are forced HIGH.

The logic equations for the outputs are shown below:

$$\bar{Z}_a = E_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot S_1 \cdot \bar{S}_0 + I_{2a} \cdot S_1 \cdot S_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = E_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot S_1 \cdot \bar{S}_0 + I_{2b} \cdot S_1 \cdot S_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

FUNCTION TABLE

Select Inputs		Inputs (a or b)					Output
S ₀	S ₁	E	I ₀	I ₁	I ₂	I ₃	Z
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

MC54/74F352

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current		9.3	14	mA	V _{IN} = GND	V _{CC} = MAX
I _{CCL}			13.3	20		V _{IN} = HIGH	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	7.4	11	3.0	14	3.0	12.5	ns
t _{PHL}	S _n to \bar{Z}_n	3.0	7.0	8.5	2.5	11	2.5	9.5	
t _{PLH}	Propagation Delay	2.5	5.0	7.0	2.0	10	2.0	8.0	ns
t _{PHL}	\bar{E}_n to \bar{Z}_n	3.0	5.0	7.0	2.5	9.0	2.5	8.0	
t _{PLH}	Propagation Delay	2.5	4.9	7.0	2.0	9.0	2.0	8.0	ns
t _{PHL}	I _n to \bar{Z}_n	1.5	3.0	3.5	1.0	5.0	1.0	4.0	



DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74F353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus-oriented systems.

- Inverted Version of F253
- Multifunction Capability
- Separate Enables for Each Multiplexer

FUNCTIONAL DESCRIPTION

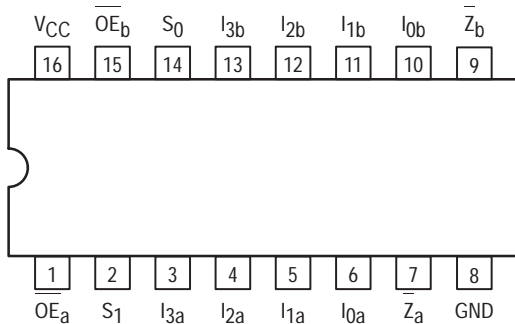
The MC54/74F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output enable (OE_a, OE_b) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\bar{Z}_a = \overline{OE_a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = \overline{OE_b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

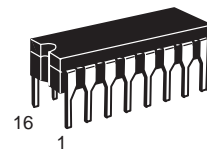
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

CONNECTION DIAGRAM (TOP VIEW)

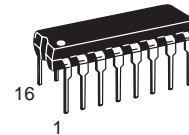


MC54/74F353

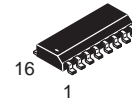
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

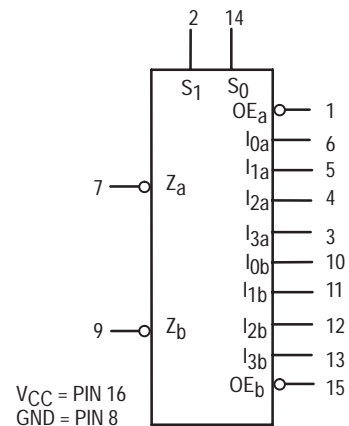


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



MC54/74F353

FUNCTION TABLE

Select Inputs		Data Inputs				Output Enable	Output
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	OE	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S₀ and S₁ are common to both sections.

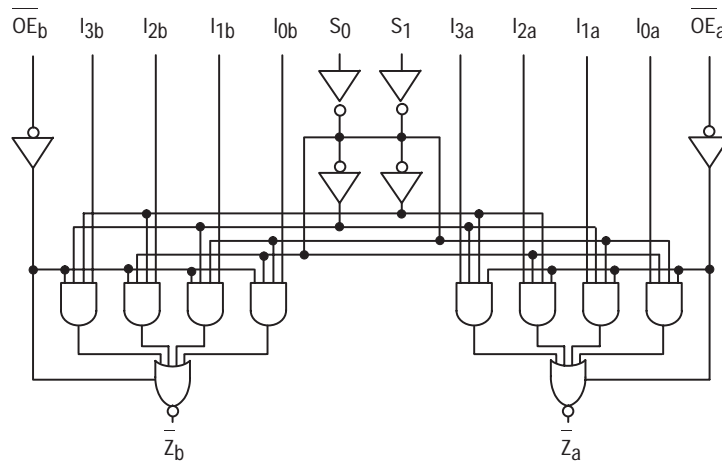
H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

(Z) = High Impedance

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

MC54/74F353

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCH}	Power Supply Current		9.3	14	mA	I _n , S _n , OE _n = GND	V _{CC} = MAX
I _{CCL}			13.3	20		I _n , S _n = GND	
I _{CCZ}			15	23		OE _n = 4.5 V	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

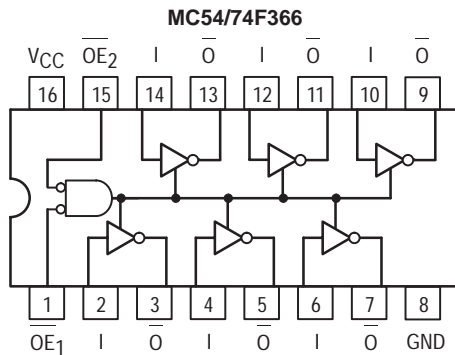
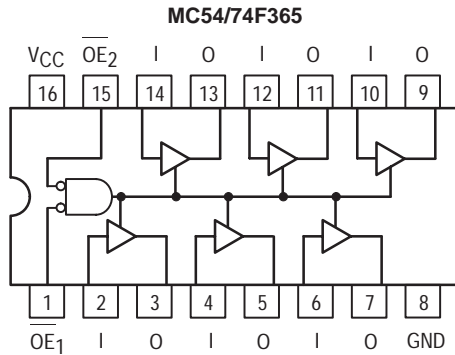
AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.5	11	3.0	14	3.0	12.5	ns
t _{PHL}	S _n to \bar{Z}_n	3.0	8.5	2.5	11	2.5	9.5	
t _{PLH}	Propagation Delay	2.5	7.0	2.0	9.0	2.0	8.0	ns
t _{PHL}	I _n to \bar{Z}_n	1.0	3.5	1.0	5.0	1.0	4.0	
t _{PZH}	Output Enable Time	3.0	8.0	3.0	10.5	3.0	9.0	ns
t _{PZL}		3.5	8.0	3.0	10.5	3.0	9.0	
t _{PHZ}	Output Disable Time	2.0	5.0	2.0	7.0	1.5	6.0	
t _{PLZ}		2.0	6.0	1.5	8.0	1.5	7.0	



HEX BUFFER/DRIVER GATED ENABLE NONINVERTING AND INVERTING, 3-STATE

CONNECTION DIAGRAM



FUNCTION TABLE

Inputs			Outputs	
OE ₁	OE ₂	I	O	O
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

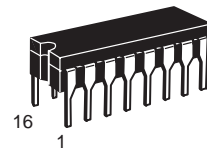
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54,74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-12	mA
		74			-15	
I _{OL}	Output Current — Low	54			48	mA
		74			64	

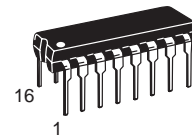
**MC54/74F365
MC54/74F366**

**F365
HEX BUFFER/DRIVER
GATED ENABLE
NONINVERTING, 3-STATE**

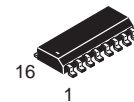
**F366
HEX BUFFER/DRIVER
GATED ENABLE
INVERTING, 3-STATE
FAST™ SCHOTTKY TTL**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**



**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

MC54/74F365 • MC54/74F366

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V _{OH}	Output HIGH Voltage	54,74	2.4	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
		54	2.0			V	I _{OH} = -12 mA	V _{CC} = 4.5 V
		74	2.0			V	I _{OH} = -15 mA	V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	54		0.35	0.55	V	I _{OL} = 48 mA	V _{CC} = MAX
		74		0.4	0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output OFF Current-HIGH			50		μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current-LOW			-50		μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20		μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		μA	V _{IN} = 7.0 V	V _{CC} = 0 V
I _{IL}	Input LOW Current			-20		μA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-100		-225		mA	V _{OUT} = GND	V _{CC} = MAX
I _{CC}	F365	I _{CC} H			35	mA	V _{CC} = MAX	
		I _{CC} L			62			
		I _{CC} Z			48			
	F366	I _{CC} H			25			
		I _{CC} L			62			
		I _{CC} Z			48			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

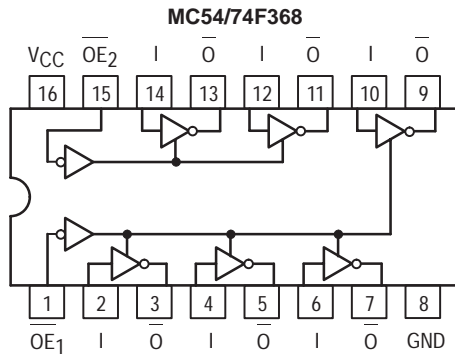
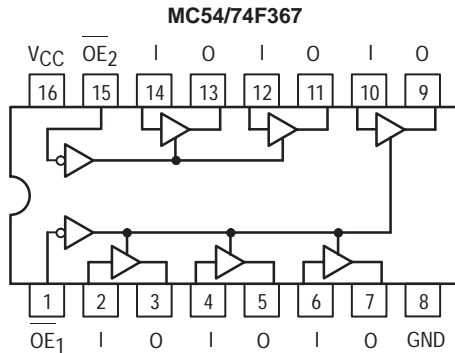
AC CHARACTERISTICS

Symbol	Parameter		54/74F			54F		74F		Unit
			T _A = +25°C			T _A = -55°C to +125°C		T _A = 0°C to +70°C		
			V _{CC} = +5.0 V			V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%		
			C _L = 50 pF			C _L = 50 pF		C _L = 50 pF		
Min	Typ	Max	Min	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	F365	2.0	4.5	6.5	2.0	8.0	2.0	7.0	ns
t _{PHL}	I _n to O _n		3.0	5.5	7.0	3.0	8.5	3.0	7.5	
t _{PLH}	Propagation Delay	F366	2.0	5.0	6.5	2.0	8.5	2.0	7.5	ns
t _{PHL}	I _n to O _n		1.0	3.0	5.0	1.0	6.5	1.0	5.5	
t _{PZH}	Output Enable Time		3.0	6.5	9.5	3.0	11	3.0	10	ns
t _{PZL}	to HIGH and LOW Level		4.0	6.0	9.0	4.0	10.5	4.0	9.5	
t _{PHZ}	Output Disable Time		2.5	4.5	6.5	2.5	8.0	2.5	7.0	ns
t _{PLZ}	from HIGH and LOW Level		1.5	4.0	6.0	1.5	7.5	1.5	6.5	



HEX BUFFER/DRIVER 4-BIT PLUS 2-BIT, NONINVERTING AND INVERTING, 3-STATE

CONNECTION DIAGRAMS



FUNCTION TABLE

Inputs		Outputs	
OE	I	O	O
L	L	L	H
L	H	H	L
H	X	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

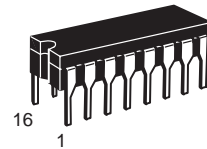
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-12	mA
		74			-15	
I _{OL}	Output Current — Low	54			48	mA
		74			64	

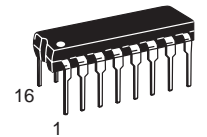
**MC54/74F367
MC54/74F368**

**F367
HEX BUFFER/DRIVER
4-BIT PLUS 2-BIT,
NONINVERTING 3-STATE**

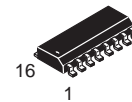
**F368
HEX BUFFER/DRIVER
4-BIT PLUS 2-BIT,
INVERTING 3-STATE
FAST™ SCHOTTKY TTL**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**



**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

MC54/74F367 • MC54/74F368

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V	
		74	2.7	3.4	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V	
		54	2.0		V	I _{OH} = -12 mA	V _{CC} = 4.5 V	
		74	2.0		V	I _{OH} = -15 mA	V _{CC} = 4.5 V	
V _{OL}	Output LOW Voltage	54		0.35	0.55	V	I _{OL} = 48 mA	V _{CC} = MAX
		74		0.4	0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX	
I _{OZL}	Output Off Current LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX	
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX	
				100		V _{IN} = 7.0 V	V _{CC} = 0 V	
I _{IL}	Input LOW Current			-20	μA	V _{IN} = 0.5 V	V _{CC} = MAX	
I _{OS}	Output Short Circuit Current (Note 2)	-100		-225	mA	V _{OUT} = GND	V _{CC} = MAX	
I _{CC}	F367	I _{CCH}			35	mA	V _{CC} = MAX	
		I _{CCL}			62			
		I _{CCZ}			48			
	F368	I _{CCH}			25			
		I _{CCL}			62			
		I _{CCZ}			48			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit		
		T _A = +25°C			T _A = -55°C to +125°C		T _A = 0°C to +70°C				
		V _{CC} = +5.0 V			V _{CC} = 5.0 V ± 10%		V _{CC} = 5.0 V ± 10%				
		C _L = 50 pF			C _L = 50 pF		C _L = 50 pF				
		Min	Typ	Max	Min	Max	Min	Max			
t _{PLH}	Propagation Delay	F367		2.0	4.5	6.5	2.0	8.0	2.0	7.0	ns
t _{PHL}	I _n to O _n	3.0	5.5	7.0	3.0	8.5	3.0	7.5			
t _{PLH}	Propagation Delay	F368		2.0	5.0	6.5	2.0	8.5	2.0	7.5	ns
t _{PHL}	I _n to \bar{O}_n	1.0	3.0	5.0	1.0	6.5	1.0	5.5			
t _{PZH}	Output Enable Time	2.5	5.5	7.5	2.5	9.5	2.5	8.5	ns		
t _{PZL}	to HIGH and LOW Level	3.0	6.5	8.5	3.0	10	3.0	9.0			
t _{PHZ}	Output Disable Time	2.5	4.5	6.5	2.5	8.0	2.5	7.0	ns		
t _{PLZ}	from HIGH and LOW Level	1.5	4.0	6.0	1.5	7.5	1.5	6.5			

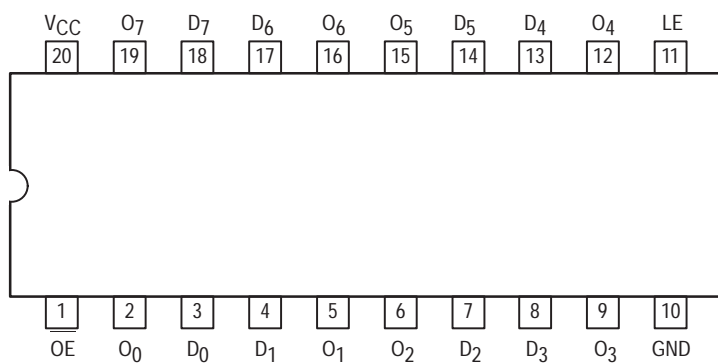


OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

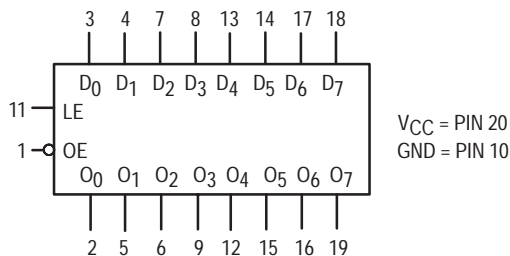
The MC54/74F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- ESD > 4000 Volts

CONNECTION DIAGRAM (TOP VIEW)



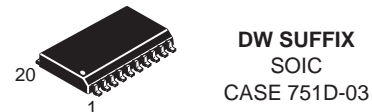
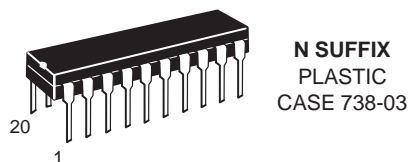
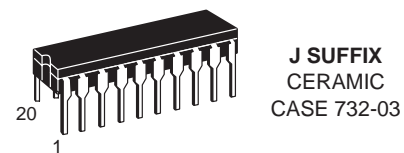
LOGIC SYMBOL



MC54/74F373

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

FAST™ SCHOTTKY TTL



ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — HIGH	54, 74			-3.0	mA
I _{OL}	Output Current — LOW	54, 74			24	mA

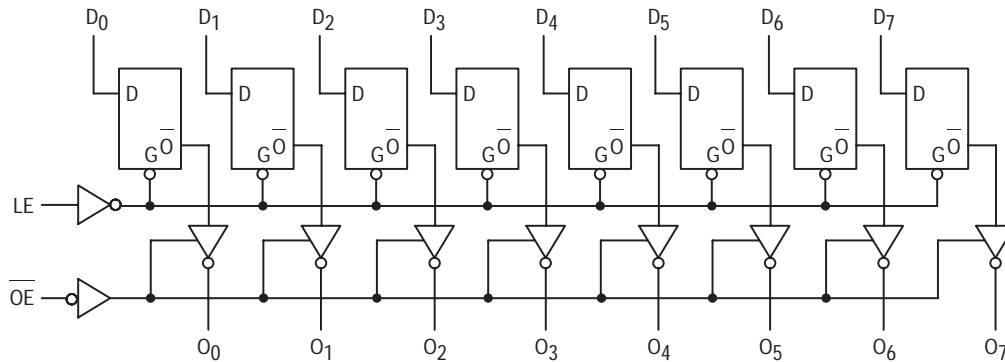
MC54/74F373

FUNCTIONAL DESCRIPTION

The F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent; i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs one setup time

preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are in the bi-state mode. When OE is HIGH the buffers are in the high impedance mode, but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18 \text{ mA}$	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	$I_{OH} = -3.0 \text{ mA}$	$V_{CC} = 4.5 \text{ V}$
		74	2.7	3.3	V	$I_{OH} = -3.0 \text{ mA}$	$V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	$V_{CC} = \text{MIN}$
I_{OZH}	Output OFF Current — HIGH			50	μA	$V_{OUT} = 2.7 \text{ V}$	$V_{CC} = \text{MAX}$
I_{OZL}	Output OFF Current — LOW			-50	μA	$V_{OUT} = 0.5 \text{ V}$	$V_{CC} = \text{MAX}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7 \text{ V}$	$V_{CC} = \text{MAX}$
				100	μA	$V_{IN} = 7.0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5 \text{ V}$	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{CCZ}	Power Supply Current (All Outputs OFF)		35	55	mA	$OE = 4.5 \text{ V}$ $D_n, LE = \text{GND}$	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F373

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	5.3	7.0	3.0	8.5	3.0	8.0	ns
t _{PHL}	D _n to O _n	2.0	3.7	5.0	2.0	7.0	2.0	6.0	
t _{PLH}	Propagation Delay	5.0	9.0	11.5	5.0	15	5.0	13	ns
t _{PHL}	LE to O _n	3.0	5.2	7.0	3.0	8.5	3.0	8.0	
t _{PZH}	Output Enable Time	2.0	5.0	11	2.0	13.5	2.0	12	ns
t _{PZL}		2.0	5.6	7.5	2.0	10	2.0	8.5	
t _{PHZ}	Output Disable Time	1.5	4.5	6.5	1.5	10	1.5	7.5	ns
t _{PLZ}		1.5	3.8	6.0	1.5	7.0	1.5	6.0	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0			2.0		2.0		ns
t _S (L)	D _n to LE	2.0			2.0		2.0		
t _H (H)	Hold Time, HIGH or LOW	3.0			3.0		3.0		
t _H (L)	D _n to LE	3.0			3.0		3.0		ns
t _W (H)	LE Pulse Width, HIGH	6.0			6.0		6.0		

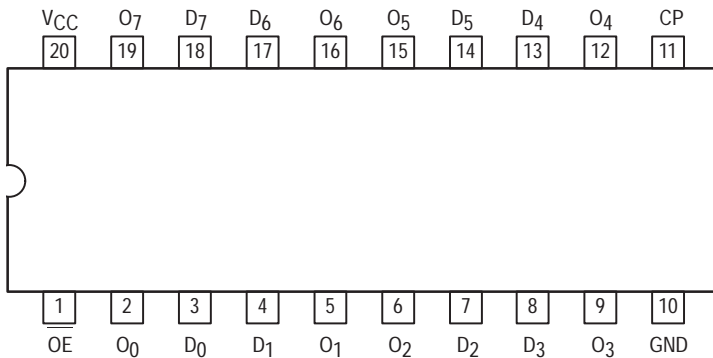


OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC54/74F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

- Edge-triggered D-Type Inputs
- Buffered Positive Edge-triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- ESD > 4000 Volts

CONNECTION DIAGRAM (TOP VIEW)



FUNCTION TABLE

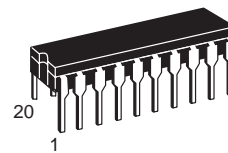
Inputs		Outputs	
D _n	CP	OE	O _n
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

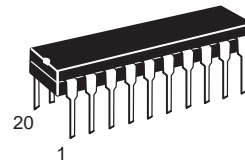
MC54/74F374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

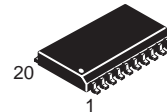
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03

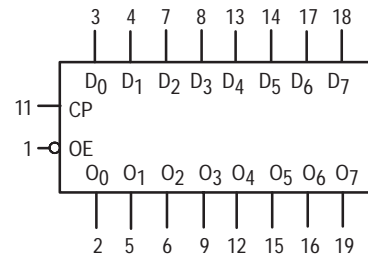


DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXDW SOIC

LOGIC SYMBOL



V_{CC} = PIN 20
 GND = PIN 10

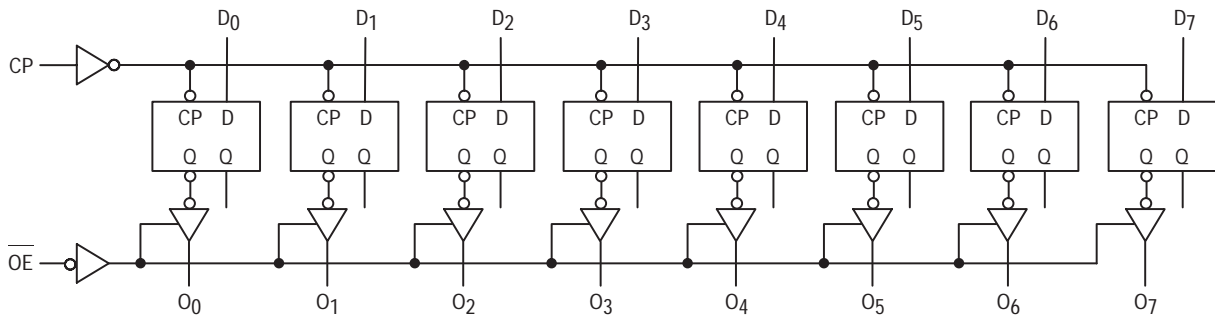
MC54/74F374

FUNCTIONAL DESCRIPTION

The F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the

LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.3	V	$I_{OH} = -3.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 24$ mA	$V_{CC} = \text{MIN}$
I_{OZH}	Output OFF Current — HIGH			50	μ A	$V_{OUT} = 2.7$ V	$V_{CC} = \text{MAX}$
I_{OZL}	Output OFF Current — LOW			-50	μ A	$V_{OUT} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{IH}	Input HIGH Current			20	μ A	$V_{IN} = 2.7$ V	$V_{CC} = \text{MAX}$
				100	μ A	$V_{IN} = 7.0$ V	$V_{CC} = \text{MAX}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} = \text{MAX}$
I_{CCZ}	Power Supply Current (All Outputs OFF)		55	86	mA	$\overline{D}_n = \text{GND}$ $\text{OE} = 4.5$ V	$V_{CC} = \text{MAX}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F374

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — HIGH	54, 74			-3.0	mA
I _{OL}	Output Current — LOW	54, 74			24	mA

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100			60		70		MHz
t _{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10	ns
t _{PHL}	CP to O _n	4.0	6.5	8.5	4.0	11	4.0	10	
t _{PZH}	Output Enable Time	2.0	9.0	11.5	2.0	14	2.0	12.5	ns
t _{PZL}		2.0	5.8	7.5	2.0	10	2.0	8.5	
t _{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	ns
t _{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0			2.5		2.0		ns
t _S (L)	D _n to CP	2.0			2.0		2.0		
t _H (H)	Hold Time, HIGH or LOW	2.0			2.0		2.0		
t _H (L)	D _n to CP	2.0			2.5		2.0		
t _W (H)	CP Pulse Width,	7.0			7.0		7.0		ns
t _W (L)	HIGH or LOW	6.0			6.0		6.0		

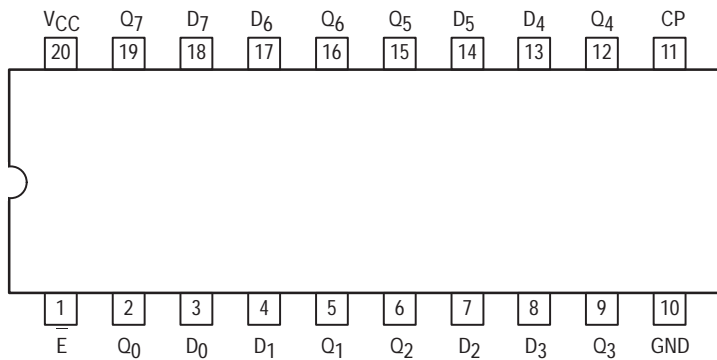


OCTAL D FLIP-FLOP WITH ENABLE

The MC74F377 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with individual D inputs and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable (E) is LOW. This device is supplied in a 20-pin package.

- High Impedance NPN Base Inputs for Reduced Loading (20 μ A in HIGH and LOW States)
- Ideal for Addressable Register Applications
- Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- See: MC74F373 for Transparent Latch Version
MC74F374 for 3-State Version

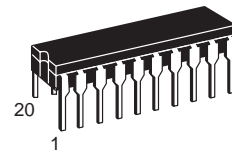
CONNECTION DIAGRAM (TOP VIEW)



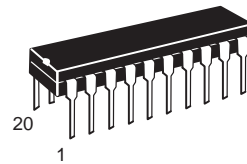
MC74F377

OCTAL D FLIP-FLOP WITH ENABLE

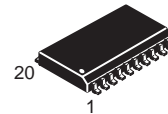
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	\bar{E}	D _n	Q _n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH voltage level steady state; h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition; L = LOW voltage level steady state; l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition; X = Don't Care; ↑ = LOW-to-HIGH clock transition

MC74F377

FUNCTIONAL DESCRIPTION

The MC74F377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Enable (E) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

The E input must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — HIGH	74			-1.0	mA
I _{OL}	Output Current — LOW	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	2.5	2.5		V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		2.7	2.7				V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
I _{IL}	Input LOW Current			-20	μA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Total Supply Current	I _{CC} H	55	72	mA	D _n = 4.5 V, CP = ↑, E = GND	V _{CC} = MAX
		I _{CC} L	70	90	mA	D _n = E = GND, CP = ↑	

NOTES:

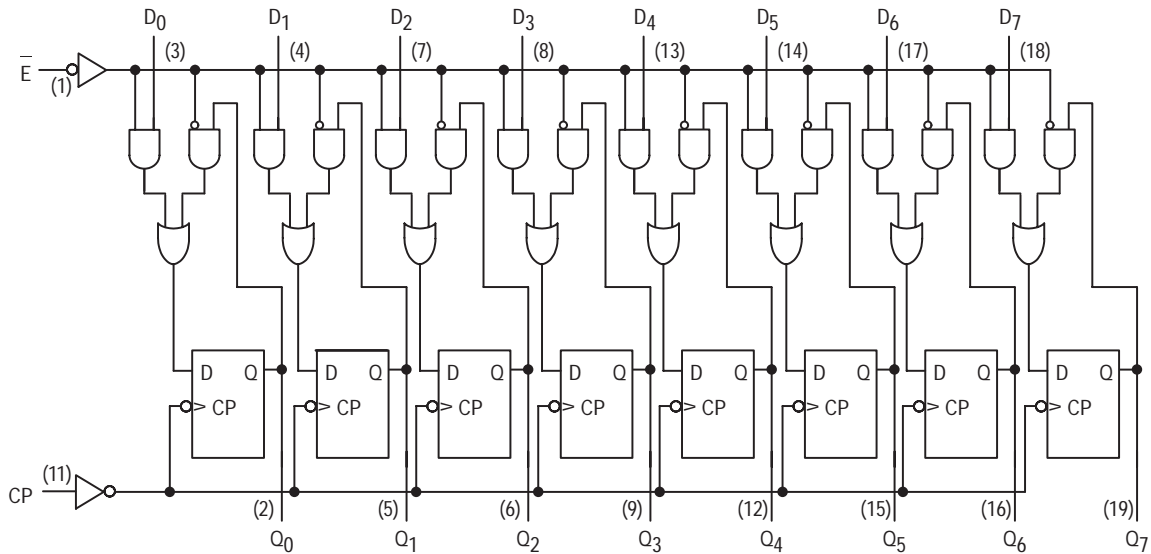
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0 to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	110	120		100		MHz
t _{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10	ns
t _{PHL}	CP to Q _n	4.0	7.0	9.0	4.0	10.5	

MC74F377

LOGIC DIAGRAM



V_{CC} = PIN 20
GND = PIN 10

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C			T _A = 0°C to +70°C			
		V _{CC} = 5.0 V			V _{CC} = 5.0 V ± 10%			
		C _L = 50 pF			C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _s (H)	Setup Time, HIGH or LOW	3.0			3.0			ns
t _s (L)	D _n to CP	3.0			3.0			
t _h (H)	Hold Time, HIGH or LOW	1.0			1.0			ns
t _h (L)	D _n to CP	1.0			1.0			
t _s (H)	Setup Time, HIGH or LOW	2.5			2.5			ns
t _s (L)	\bar{E} to CP	4.0			4.0			
t _h (H)	Hold Time, HIGH or LOW	0			0			ns
t _h (L)	\bar{E} to CP	0			0			
t _w (H)	Clock Pulse Width	4.0			5.0			ns
t _w (L)	HIGH or LOW	4.0			5.0			



PARALLEL D REGISTER WITH ENABLE

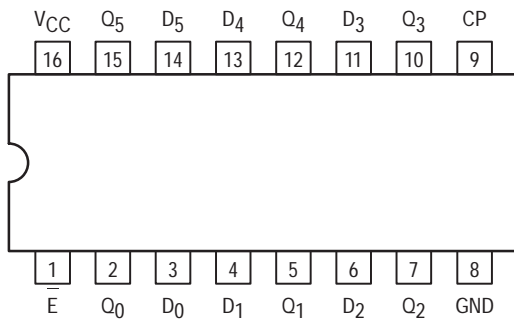
The MC54/74F378 is a 6-bit register with a buffered common enable. This device is similar to the F174 but with common Enable rather than common Master Reset.

The F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable (E) inputs are common to all flip-flops.

When the E input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the E input is HIGH the register will retain the present data independent of the CP input. This circuit is designed to prevent false clocking by transitions on the E input.

- 6-Bit High-Speed Parallel Register
- Positive Edge-Triggered D-Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM (TOP VIEW)



FUNCTION TABLE

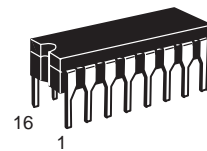
Inputs			Output
E	CP	D _n	Q _n
H		X	No Change
L		H	H
L		L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

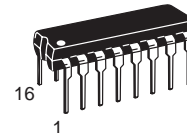
MC54/74F378

PARALLEL D REGISTER WITH ENABLE

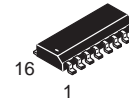
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

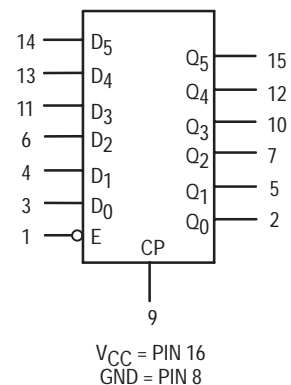


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

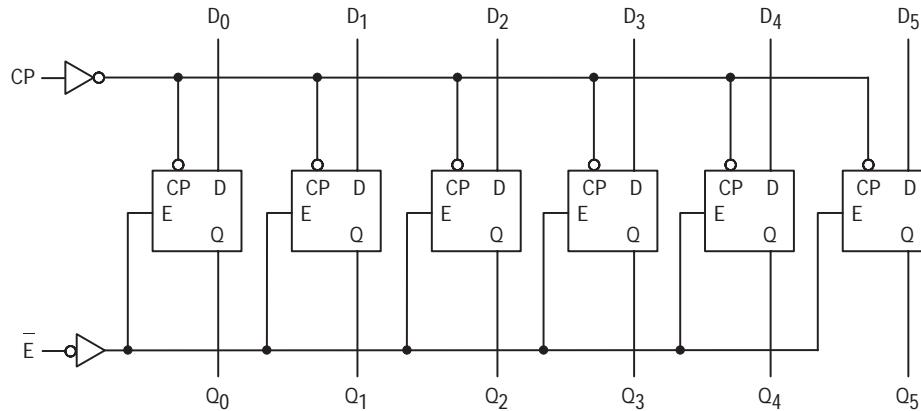
MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F378

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — HIGH	54, 74			-1.0	mA
I _{OL}	Output Current — LOW	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OL} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7		V	I _{OL} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		30	45	mA	V _{CC} = MAX, V _{CP} = 0 V

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F378

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = 5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Input Frequency	80	140		80		80		MHz
t _{PLH}	Propagation Delay	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t _{PHL}	CP to Q _n	3.5	6.0	8.5	3.5	10.5	3.5	9.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = 5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.0			4.0		4.0		ns
t _S (L)	D _n to CP	4.0			4.0		4.0		
t _H (H)	Hold Time, HIGH or LOW	0			0		0		
t _H (L)	D _n to CP	0			0		0		ns
t _S (H)	Setup Time, HIGH or LOW	6.0			6.0		6.0		
t _S (L)	E to CP	6.0			6.0		6.0		
t _H (H)	Hold Time, HIGH or LOW	2.0			2.0		2.0		ns
t _H (L)	E to CP	2.0			2.0		2.0		
t _W (H)	CP Pulse Width, HIGH or LOW	4.0			4.0		4.0		ns
t _W (L)		6.0			6.0		6.0		



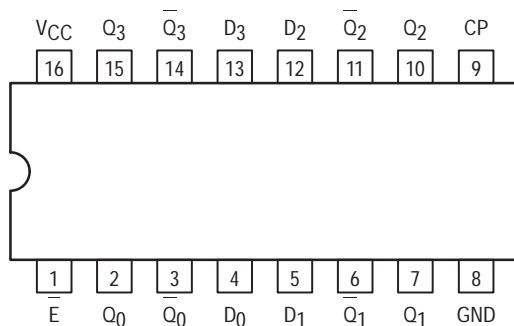
QUAD PARALLEL REGISTER

The MC54/74F379 is a 4-bit register with a buffered common enable. This device is similar to the F175 but features the common Enable rather than common Master Reset.

The F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock (CP) and Enable (E) inputs are common to all flip-flops. When E is HIGH, the register will retain the present data independent of the CP input. The \bar{D}_n and E inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed. This circuit is designed to prevent false clocking by transitions on the E input.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Buffered Common Enable Input
- True and Complement Outputs

CONNECTION DIAGRAM (TOP VIEW)



FUNCTION TABLE

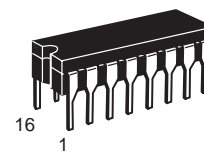
Inputs		Outputs		
E	CP	\bar{D}_n	Q_n	\bar{Q}_n
H		X	NC	NC
L		H	H	L
L		L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change

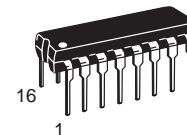
MC54/74F379

QUAD PARALLEL REGISTER WITH ENABLE

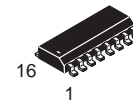
FAST™ SCHOTTKY TTL



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08

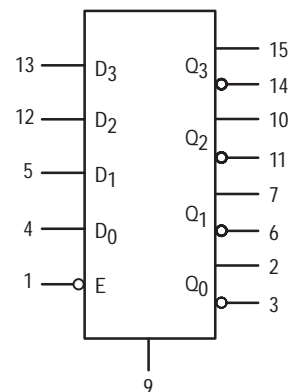


D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXD SOIC

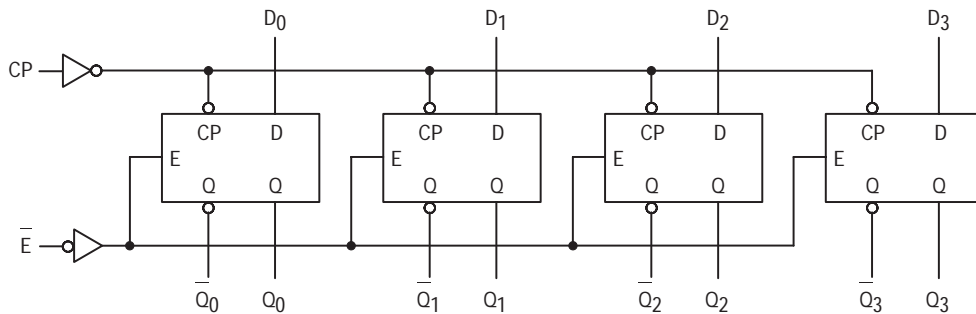
LOGIC SYMBOL



V_{CC} = PIN 16
 GND = PIN 8

MC54/74F379

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — HIGH	54, 74			-1.0	mA
I_{OL}	Output Current — LOW	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54, 74	2.5		V	$I_{OL} = -1.0 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$
		74	2.7		V	$I_{OL} = -1.0 \text{ mA}$, $V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 20 \text{ mA}$, $V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5 \text{ V}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0 \text{ V}$
I_{CC}	Power Supply Current		28	40	mA	$V_{CC} = \text{MAX}$, $D = \bar{E} = \text{GND}$, $CP = \text{⏏}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F379

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	140		90		100		MHz
t_{PLH}	Propagation Delay	3.5	5.0	6.5	3.5	8.5	3.5	7.5	ns
t_{PHL}	CP to Q_n, \bar{Q}_n	5.0	6.5	8.5	5.0	10.5	5.0	9.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Typ	Max	Min	max	Min	Max	
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	3.0			3.0		3.0		ns
$t_{\text{S}}(\text{L})$	D_n to CP	3.0			3.0		3.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	1.0			1.0		1.0		ns
$t_{\text{H}}(\text{L})$	D_n to CP	1.0			1.0		1.0		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	6.0			6.0		6.0		ns
$t_{\text{S}}(\text{L})$	\bar{E} to CP	6.0			6.0		6.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	2.0			2.0		2.0		ns
$t_{\text{H}}(\text{L})$	\bar{E} to CP	2.0			2.0		2.0		
$t_{\text{W}}(\text{H})$	CP Pulse Width, HIGH or LOW	4.0			4.0		4.0		ns
$t_{\text{W}}(\text{L})$		5.0			5.0		5.0		

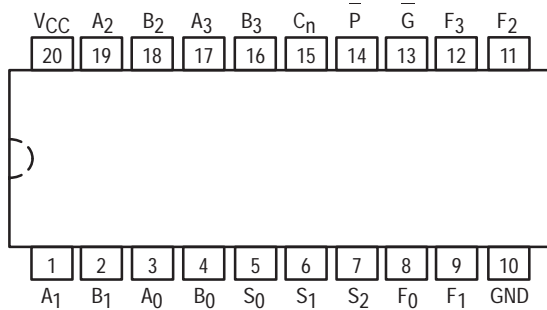


4-BIT ARITHMETIC LOGIC UNIT

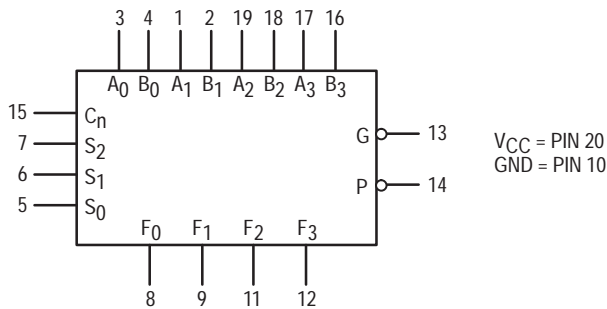
The MC54/74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. Carry Propagate and Generate outputs are provided for use with the F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the F382 ALU data sheet.

- Low Input Loading Minimizes Drive Requirements
- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- Carry Generate and Propagate Outputs for use with Carry Lookahead Generator

CONNECTION DIAGRAM

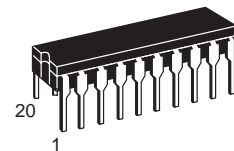


LOGIC SYMBOL

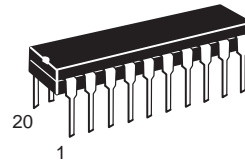


MC54/74F381

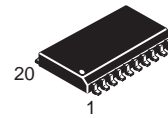
4-BIT ARITHMETIC LOGIC UNIT FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

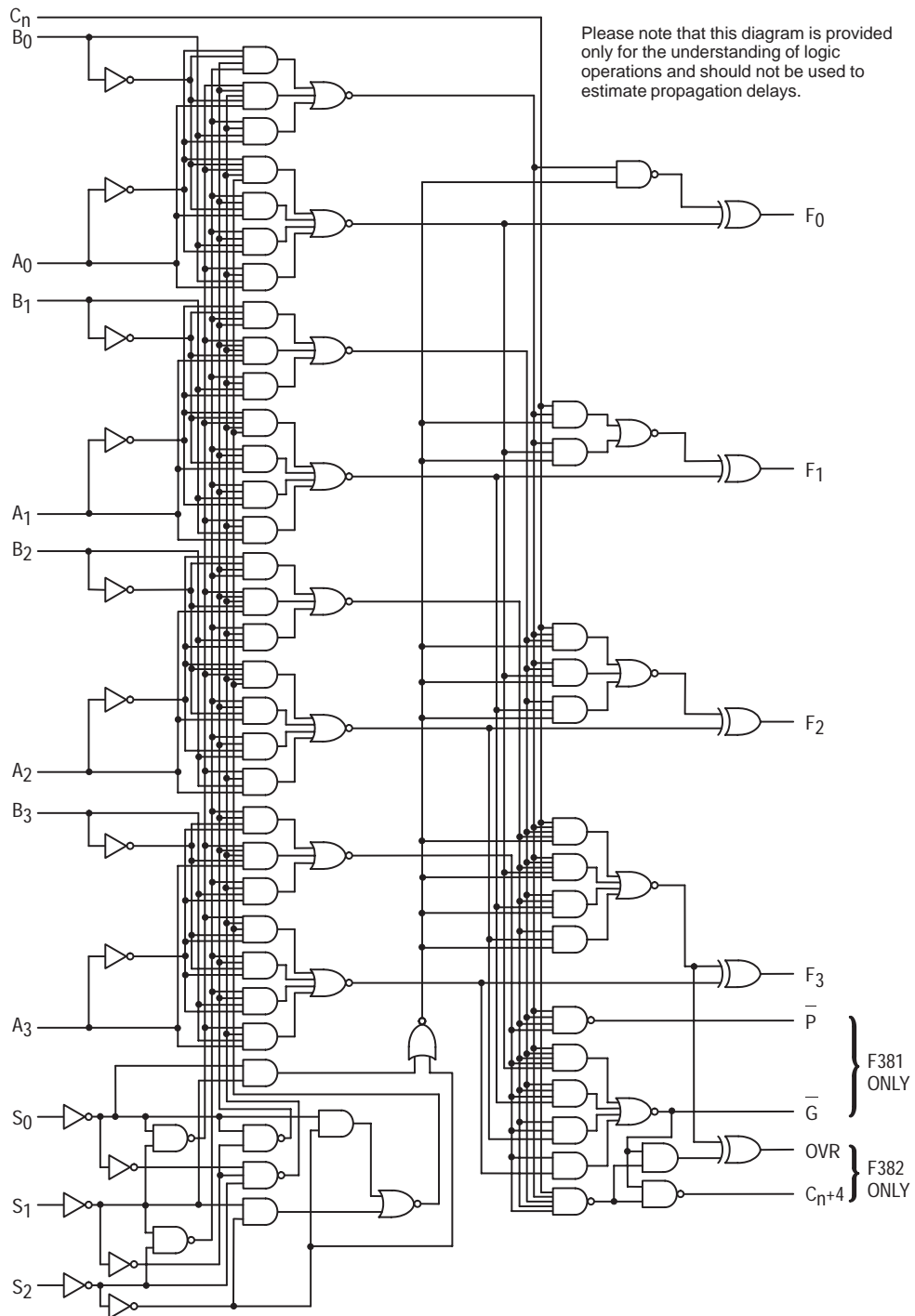
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F381

LOGIC DIAGRAM



MC54/74F381

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current S ₀ -S ₂ Inputs			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
	Other Inputs			-2.4	mA	V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		59	89	mA	S ₀ -S ₂ = GND; Other Inputs HIGH	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs S₀-S₂ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active-HIGH or active-LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active-HIGH oper-

ands, LOW for active-LOW operands) into the C_n input of the least significant package.

The Carry Generate (G) and Carry Propagate (P) outputs supply input signals to the F182 carry lookahead generator for expansion to longer word length, as shown in Figure 1. Note that an F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Figure 2.

FUNCTION SELECT TABLE

Select			Operation
S ₀	S ₁	S ₂	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level

L = LOW Voltage Level

MC54/74F381

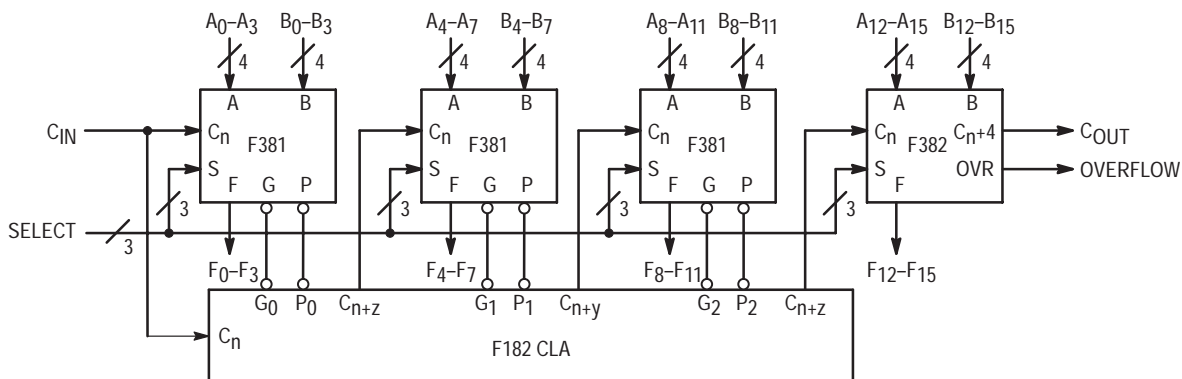


Figure 1. 16-Bit Lookahead Carry ALU Expansion

Path Segment	Toward F	Output $C_n + 4, OVR$
A_i or B_i to P	7.2 ns	7.2 ns
P_i to C_{n+j} (F182)	6.2 ns	6.2 ns
C_n to F	8.1 ns	—
C_n to C_{n+4}, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

Figure 2. 16-Bit Delay Tabulation

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0\text{ to }+70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	2.5	8.1	12	2.5	15	2.5	13	ns
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0	10.4	15	4.0	18	4.0	16	ns
t_{PLH} t_{PHL}	Propagation S_i to F_i	4.5	8.3	20	4.5	23.5	4.5	21.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to G	3.0	6.4	9.0	3.0	12	3.0	10	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_i to P	2.5	7.2	10.5	2.5	13.5	2.5	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_i to G or P	4.0	7.8	12	4.0	15	4.0	13	ns

MC54/74F381

TRUTH TABLE

FUNCTION	INPUTS						OUTPUTS							
	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	G	P		
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0		
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0		
				0	0	1	0	1	1	1	0	0		
				0	1	0	0	0	0	0	0	1	1	
				0	1	1	1	1	1	1	1	1	0	
				1	0	0	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	1	1	0	0
				1	1	0	1	0	0	1	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0		
				0	0	1	0	0	0	0	0	1	1	
				0	1	0	0	1	1	1	1	0	0	
				0	1	1	1	1	1	1	1	1	0	
				1	0	0	0	0	0	0	0	0	1	0
				1	0	1	1	1	0	0	0	0	1	1
				1	1	0	1	0	1	1	1	1	0	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1		
				0	0	1	1	1	1	1	1	1	0	
				0	1	0	1	1	1	1	1	1	0	
				0	1	1	1	0	1	1	1	0	0	
				1	0	0	0	1	0	0	0	1	1	
				1	0	1	1	0	0	0	0	1	0	
				1	1	0	0	0	0	0	0	1	0	
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	1	1		
				X	1	0	1	1	1	1	1	1		
				X	1	1	0	0	0	0	0	0		
A+B	1	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	1	1		
				X	1	0	1	1	1	1	1	1		
				X	1	1	1	1	1	1	1	1		
AB	0	1	1	X	0	0	0	0	0	0	0	0		
				X	0	1	0	0	0	0	0	1		
				X	1	0	0	0	0	0	0	0		
				X	1	1	1	1	1	1	1	1		
PRESET	1	1	1	X	0	0	1	1	1	1	1	1		
				X	0	1	1	1	1	1	1	1		
				X	1	0	1	1	1	1	1	1		
				X	1	1	1	1	1	1	1	0		

1 = HIGH Voltage Level
 0 = LOW Voltage Level
 X = Immaterial

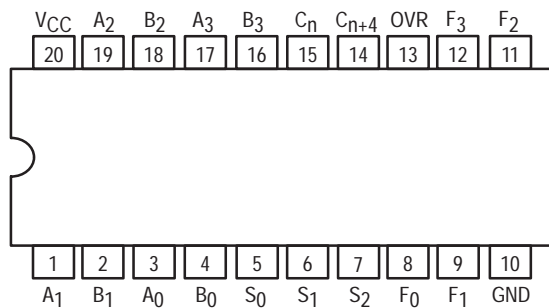


4-BIT ARITHMETIC LOGIC UNIT

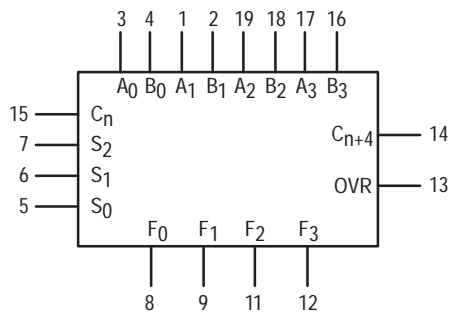
The MC54/74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the F381 data sheet.

- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- LOW Input Loading Minimizes Drive Requirements
- Carry Output for Ripple Expansion
- Overflow Output for Twos Complement Arithmetic

CONNECTION DIAGRAM

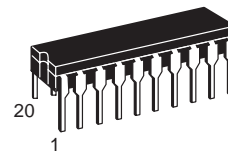


LOGIC SYMBOL

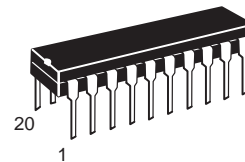


MC54/74F382

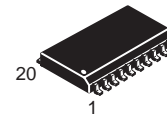
4-BIT ARITHMETIC LOGIC UNIT
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

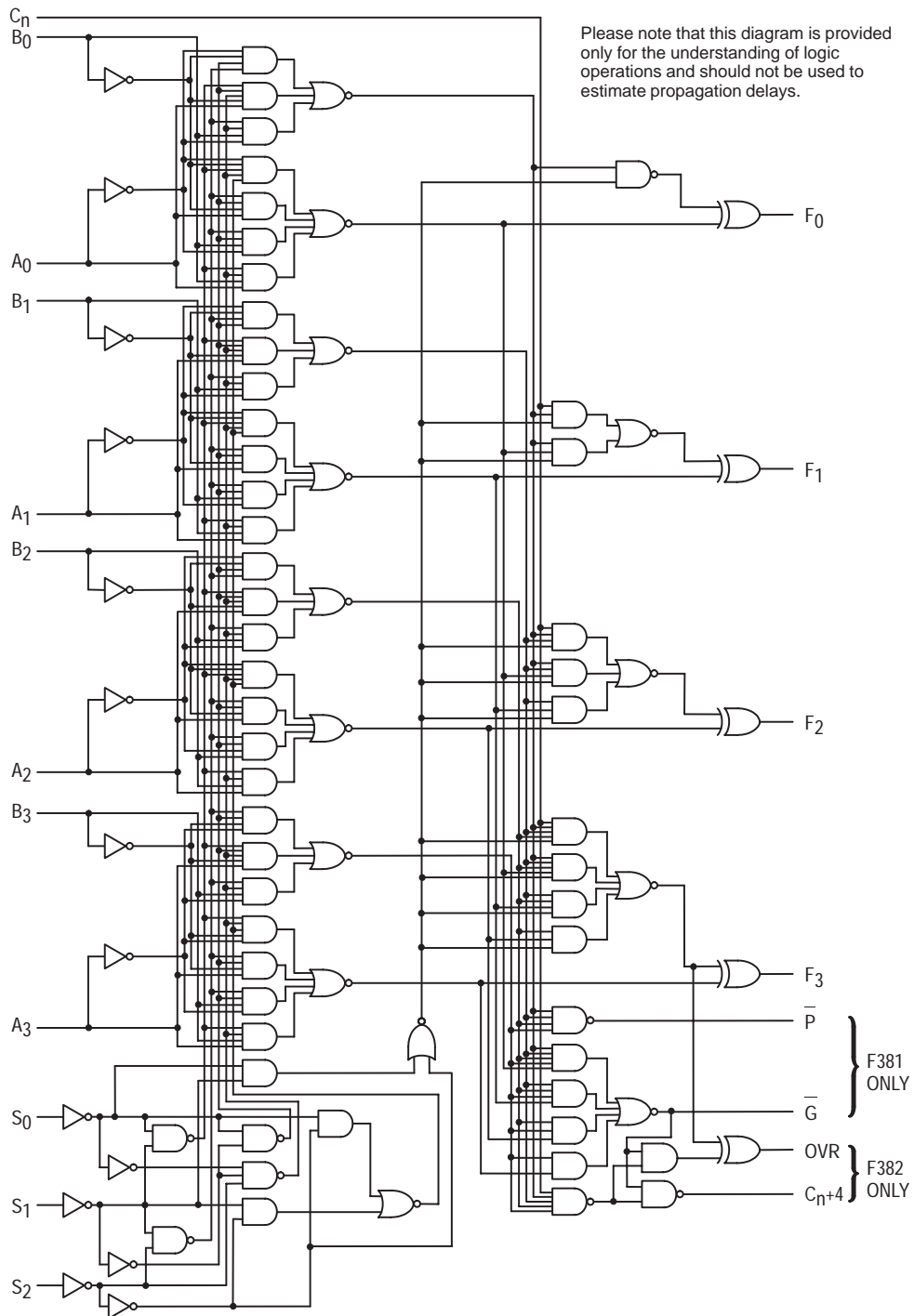
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F382

LOGIC DIAGRAM



MC54/74F382

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current S ₀ -S ₂ Inputs			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
	Other Inputs			-2.4	mA		
	C _n Input			-3.0	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		54	81	mA	S ₀ , C _n = HIGH; Other Inputs GND	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs S₀-S₂ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands,

LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in twos complement operation. Typical delays for Figure 1 are given in Figure 2.

FUNCTION SELECT TABLE

Select			Operation
S ₀	S ₁	S ₂	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A ⊕ B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level

L = LOW Voltage Level

MC54/74F382

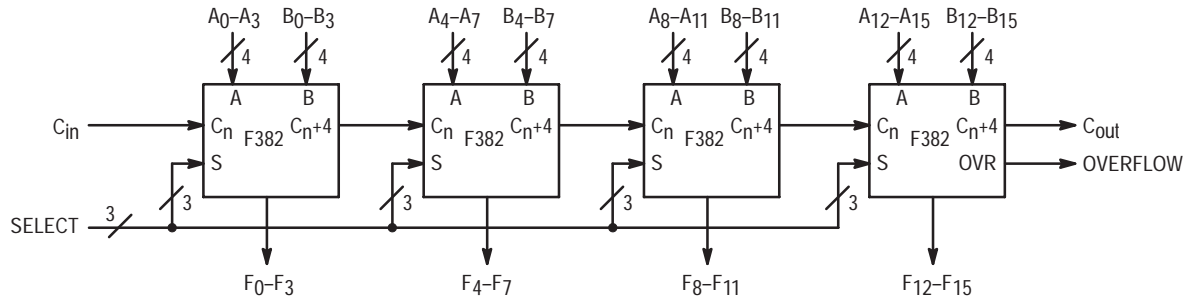


Figure 1. 16-Bit Ripple Carry ALU Expansion

Path Segment	Toward F	Output C_{n+4} , OVR
A_i or B_j to C_{n+4}	6.5 ns	6.5 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to C_{n+4}	6.3 ns	6.3 ns
C_n to F	8.1	—
C_n to C_{n+4} , OVR	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

Figure 2. 16-Bit Delay Tabulation

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0\text{ to }70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	3.0 2.5	8.1 5.7	12 8.0	3.0 2.5	15 11	3.0 2.5	13 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15 11	4.0 3.5	18 14	4.0 3.5	16 12	ns
t_{PLH} t_{PHL}	Propagation Delay S_j to F_i	6.0 4.0	11 8.2	15 20.5	6.0 4.0	21 23.5	6.0 4.0	16 21.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_j to C_{n+4}	3.5 3.0	6.0 6.5	8.5 9.0	3.5 3.0	11.5 12.5	3.5 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_j to OVR or C_{n+4}	7.0 4.5	12.5 9.0	16.5 12	7.0 4.5	19.5 15	7.0 4.5	17.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	2.5 2.5	5.6 6.3	8.0 9.0	2.5 2.5	11 12	2.5 2.5	9.0 10	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to OVR	3.5 3.5	8.0 7.1	11 10	3.5 3.5	14 13	3.5 3.5	12 11	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_j to OVR	6.5 5.5	11.5 8.0	15.5 10.5	6.5 5.5	18.5 13.5	6.5 5.5	16.5 11.5	ns

MC54/74F382

TRUTH TABLE

Function	INPUTS						OUTPUTS							
	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	OVR	C _{n+4}		
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1		
				1	X	X	0	0	0	0	1	1		
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0		
				0	0	1	0	1	1	1	0	1		
				0	1	0	0	0	0	0	0	0	0	
				0	1	1	1	1	1	1	1	0	0	
				1	0	0	0	0	0	0	0	0	1	
				1	0	1	1	1	1	1	1	0	1	
				1	1	0	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	1			
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0		
				0	0	1	0	0	0	0	0	0	0	
				0	1	0	0	1	1	1	1	0	1	
				0	1	1	1	1	1	1	1	0	0	
				1	0	0	0	0	0	0	0	0	0	1
				1	0	1	1	0	0	0	0	0	0	0
				1	1	0	1	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	0	1			
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0		
				0	0	1	1	1	1	1	0	0		
				0	1	0	1	1	1	1	0	0		
				0	1	1	0	1	1	1	0	1		
				1	0	0	0	0	0	0	0	0		
				1	0	1	0	0	0	0	0	0	1	
				1	1	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	0	1					
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	0	0		
				0	1	0	1	1	1	1	0	0		
				X	1	1	0	0	0	0	1	1		
				1	1	0	1	1	1	1	1	1		
A + B	1	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	0	0		
				X	1	0	1	1	1	1	0	0		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		
AB	0	1	1	X	0	0	0	0	0	0	1	1		
				X	0	1	0	0	0	0	0	0		
				X	1	0	0	0	0	0	1	1		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		
PRESET	1	1	1	X	0	0	1	1	1	1	0	0		
				X	0	1	1	1	1	1	0	0		
				X	1	0	1	1	1	1	0	0		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		

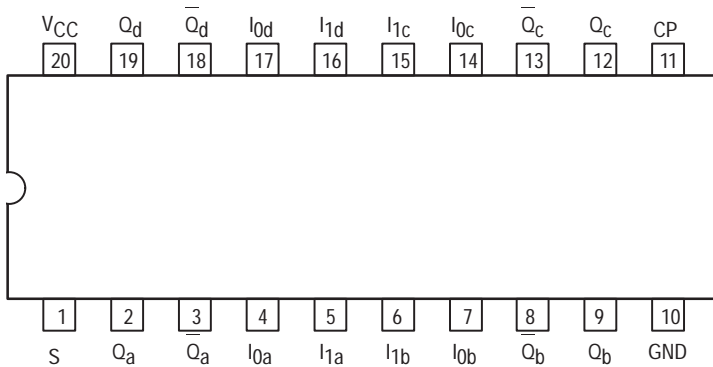
1 = HIGH Voltage Level
 0 = LOW Voltage Level
 X = Immaterial

QUAD 2-PORT REGISTER

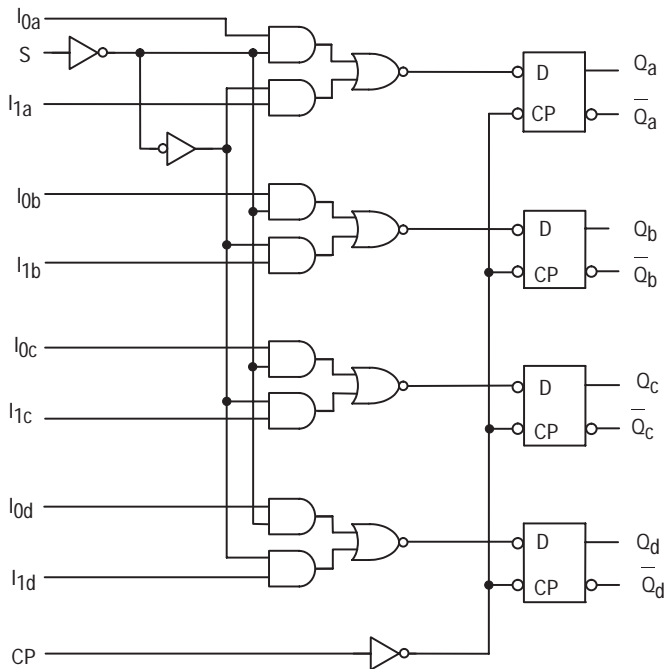
The MC54/74F398 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

- Select Inputs from Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complement Outputs

CONNECTION DIAGRAM (TOP VIEW)



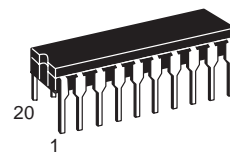
LOGIC DIAGRAM



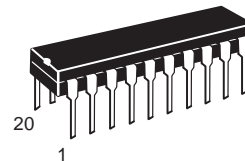
NOTES:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F398

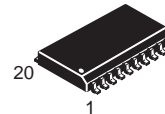
QUAD 2-PORT REGISTER FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

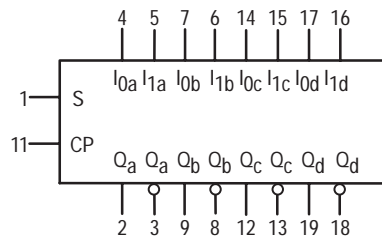


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

LOGIC SYMBOL



V_{CC} = PIN 20
GND = PIN 10

MC54/74F398

FUNCTIONAL DESCRIPTION

The MC54/74F398 is a high-speed quad 2-port register. It will select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-

type output register is fully edge-triggered. The Data inputs (I_{0x} , I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The MC54/74F398 has both Q and \bar{Q} outputs.

FUNCTION TABLE

Inputs			Outputs	
S	I_0	I_1	Q	\bar{Q}
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition

l = LOW Voltage Level; one setup time prior to the LOW-to-HIGH clock transition

X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current – High	54, 74			-1.0	mA
I_{OL}	Output Current – Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20$ mA	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μ A	$V_{IN} = 2.7$ V	$V_{CC} = \text{MAX}$
				100	μ A	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		25	38	mA	$V_{CC} = \text{MAX}$	$V_{IN} = \text{GND}$ $CP = \text{ } \int$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F398

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = -0°C to 70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		80		100		MHz
t _{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	9.5	3.0	8.5	ns
t _{PHL}	CP to Q or \bar{Q}	3.0	6.8	9.5	3.0	11.5	3.0	10.0	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0V			T _A = -55°C to +125°C V _{CC} = 5.0 V ±10%		T _A = -0°C to 70°C V _{CC} = 5.0 V ±10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0			4.5		3.0		ns
t _S (L)	I _n to CP	3.0			4.5		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0			1.5		1.0		ns
t _H (L)	I _n to CP	1.0			1.5		1.0		
t _S (H)	Setup Time, HIGH or LOW	7.5			10.5		8.5		ns
t _S (L)	S to CP	7.5			10.5		8.5		
t _H (H)	Hold Time, HIGH or LOW	0			0		0		ns
t _H (L)	S to CP	0			0		0		
t _w (H)	CP Pulse Width	4.0			4.0		4.0		ns
t _w (L)	HIGH or LOW	5.0			7.0		5.0		

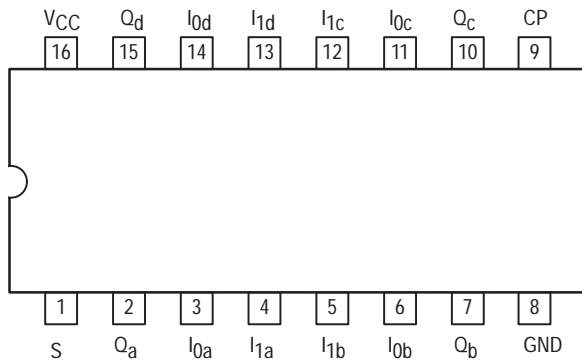


QUAD 2-PORT REGISTER

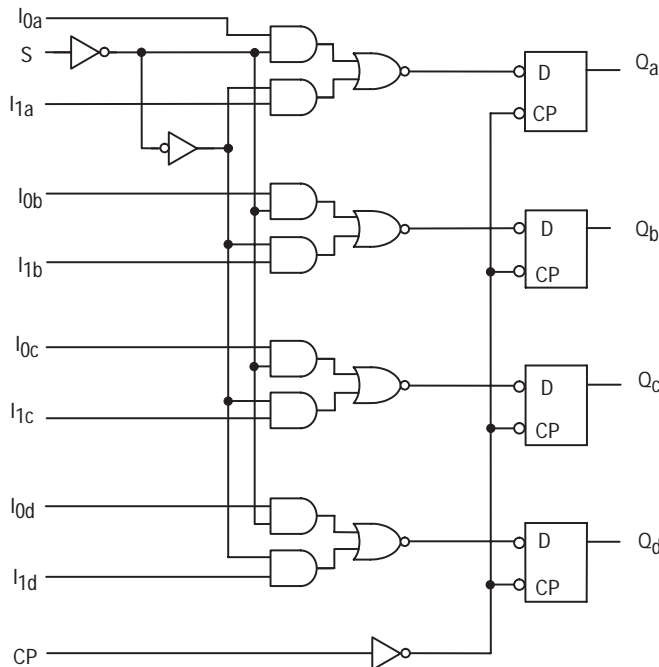
The MC54/74F399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The MC54/74F399 is the 16-pin version of the MC54/74F398, with only the Q outputs of the flip-flops available.

- Select Inputs from Two Data Sources
- Fully Positive Edge-Triggered Operation

CONNECTION DIAGRAM (TOP VIEW)



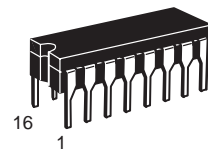
LOGIC DIAGRAM



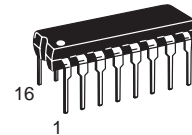
NOTE:
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MC54/74F399

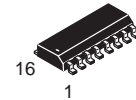
QUAD 2-PORT REGISTER
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

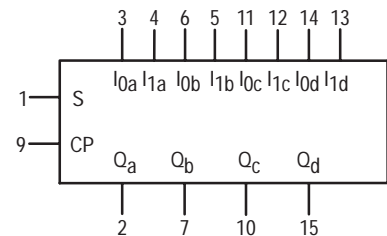


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MC54/74F399

FUNCTIONAL DESCRIPTION

The MC54/74F399 is a high-speed quad 2-port register. It will select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-

type output register is fully edge-triggered. The Data inputs (I_{0x} , I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTION TABLE

Inputs			Output
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

H = HIGH Voltage Level

L = LOW Voltage Level

h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition

X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.5$ V
		74	2.7	3.4	V	$I_{OH} = -1.0$ mA	$V_{CC} = 4.75$ V
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20$ mA	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7$ V	$V_{CC} = \text{MAX}$
				100	μA	$V_{IN} = 7.0$ V	
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5$ V	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0$ V	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		22	34	mA	$V_{CC} = \text{MAX}$	$V_{IN} = \text{GND}$ $CP = \sqrt{\quad}$

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F399

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = + 25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		80		100		MHz
t _{PLH}	Propagation Delay	3.0	5.7	7.5	3.0	9.5	3.0	8.5	ns
t _{PHL}	CP to Q	3.0	6.8	9.5	3.0	11.5	3.0	10.0	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0V			T _A = -55°C to + 125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0			4.5		3.0		ns
t _S (L)	I _n to CP	3.0			4.5		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0			1.5		1.0		ns
t _H (L)	I _n to CP	1.0			1.5		1.0		
t _S (H)	Setup Time, HIGH or LOW	7.5			9.5		8.5		ns
t _S (L)	S to CP	7.5			9.5		8.5		
t _H (H)	Hold Time, HIGH or LOW	0			0		0		ns
t _H (L)	S to CP	0			0		0		
t _w (H)	CP Pulse Width	4.0			4.0		4.0		ns
t _w (L)	HIGH or LOW	5.0			7.0		5.0		

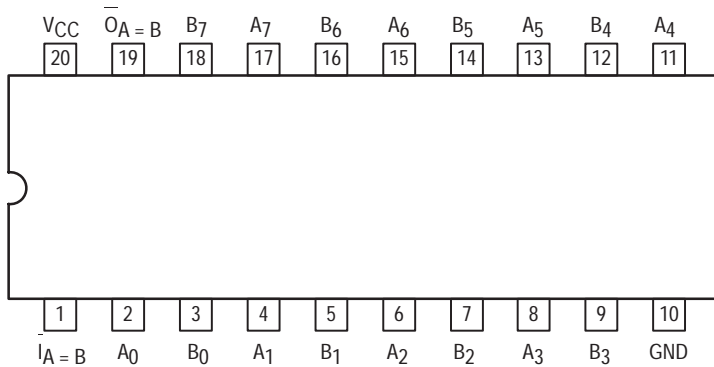


8-BIT IDENTITY COMPARATOR

The MC54/74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $I_A = B$ also serves as an active-LOW enable input.

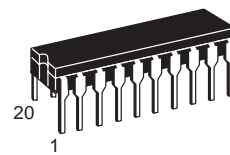
- Compares Two 8-Bit Words in 6.5 ns Typical
- Expandable to Any Word Length
- 20-Pin Package

CONNECTION DIAGRAM (TOP VIEW)

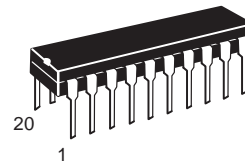


MC54/74F521

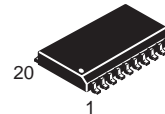
8-BIT IDENTITY COMPARATOR
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

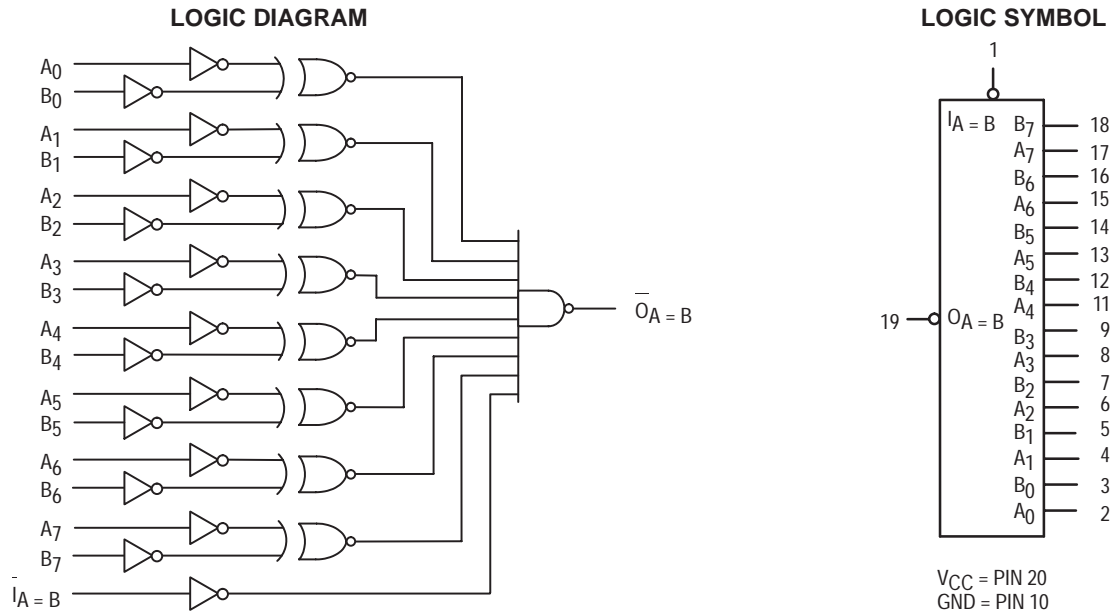
ORDERING INFORMATION

MC54FXXXJ Ceramic
 MC74FXXXN Plastic
 MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

MC54/74F521



NOTE:
This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	PARAMETER	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18 \text{ mA}$	$V_{CC} = \text{MIN}$
V_{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.5 \text{ V}$
		74	2.7	3.4	V	$I_{OH} = -1.0 \text{ mA}$	$V_{CC} = 4.75 \text{ V}$
V_{OL}	Output LOW Voltage		0.35	0.5	V	$I_{OL} = 20 \text{ mA}$	$V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7 \text{ V}$	$V_{CC} = \text{MAX}$
				100	μA	$V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5 \text{ V}$	$V_{CC} = \text{MAX}$
I_{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	$V_{OUT} = 0 \text{ V}$	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current		21	32	mA	$I_A = B = \text{GND}$	$V_{CC} = \text{MAX}$

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F521

FUNCTION TABLE

Inputs		Output
$\overline{I_A = B}$	A, B	$\overline{O_A = B}$
L	$A = B^*$	L
L	$A \neq B$	H
H	$A = B^*$	H
H	$A \neq B$	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 * $A_0 = B_0, A_1 = B_1, A_2 = B_2, \text{etc.}$

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	2.5	6.5	10	2.5	15	2.5	11	ns
t_{PHL}	A_n or B_n to $\overline{O_A = B}$	3.0	6.5	10	3.0	12	3.0	11	
t_{PLH}	Propagation Delay	2.5	4.5	6.5	2.5	8.5	2.5	7.5	ns
t_{PHL}	$\overline{I_A = B}$ to $\overline{O_A = B}$	3.5	5.0	9.0	3.5	10	3.5	10	

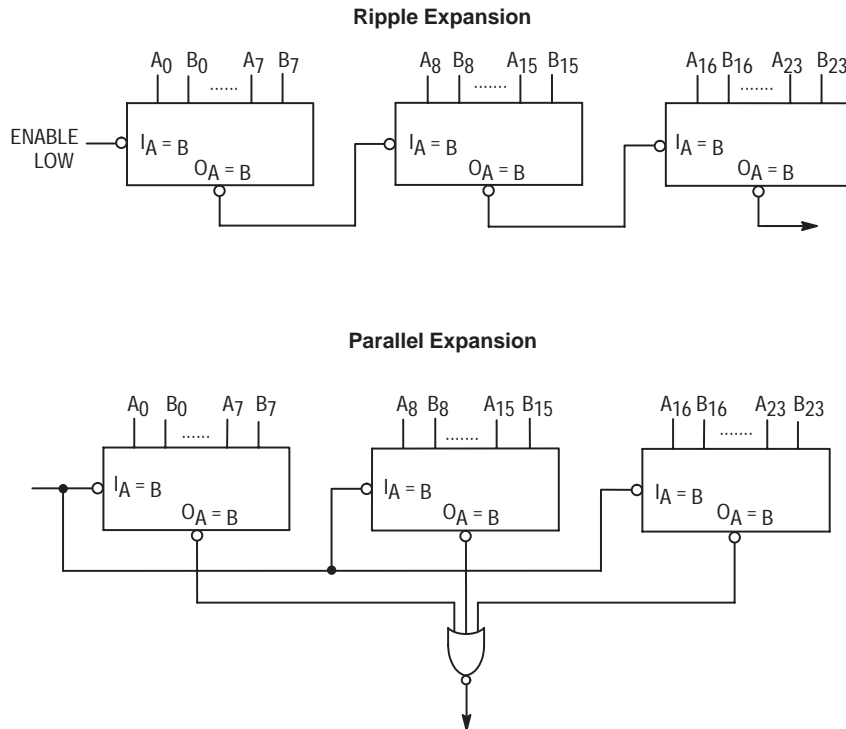


Figure 1. Applications

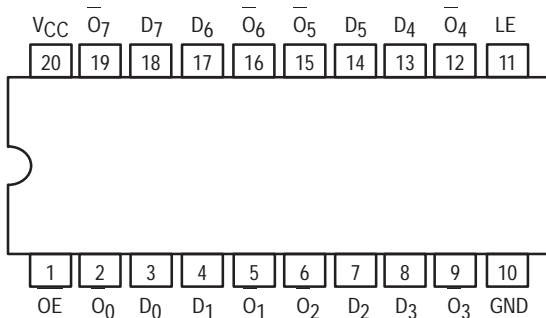


OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

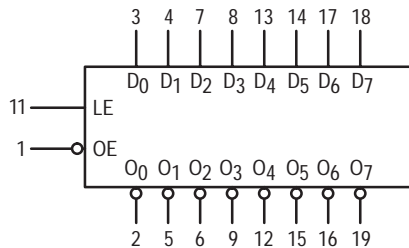
The MC54/74F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high-impedance state. The F533 is the same as the F373, except that the outputs are inverted. For description and logic diagram please see the F373 data sheet.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- ESD Protection > 4000 Volts

CONNECTION DIAGRAM



LOGIC SYMBOL

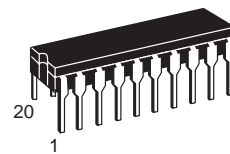


V_{CC} = PIN 20
GND = PIN 10

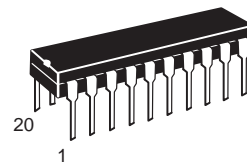
MC54/74F533

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

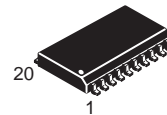
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74		-3.0	mA	
I _{OL}	Output Current — Low	54, 74		24	mA	

MC54/74F533

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCZ}	Power Supply Current		41	61	mA	OE = 4.5 V D _n , LE = Gnd	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay D _n to O _n	4.0 3.0	9.0 7.0	4.0 3.0	12 9.0	4.0 3.0	10 8.0	ns
t _{PLH} t _{PHL}	Propagation Delay LE to O _n	5.0 3.0	11 7.0	5.0 3.0	14 9.0	5.0 3.0	13 8.0	ns
t _{PZH} t _{PZL}	Output Enable Time	2.0 2.0	10 7.5	2.0 2.0	12.5 9.0	2.0 2.0	11 8.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time	1.5 1.5	6.5 5.5	1.5 1.5	8.5 7.5	1.5 1.5	7.0 6.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V		T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		
		Min	Max	Min	Max	Min	Max	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _n to LE	2.0 2.0		2.0 2.0		2.0 2.0		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW D _n to LE	3.0 3.0		3.0 3.0		3.0 3.0		ns
t _w (H)	LE Pulse Width HIGH	6.0		6.0		6.0		ns

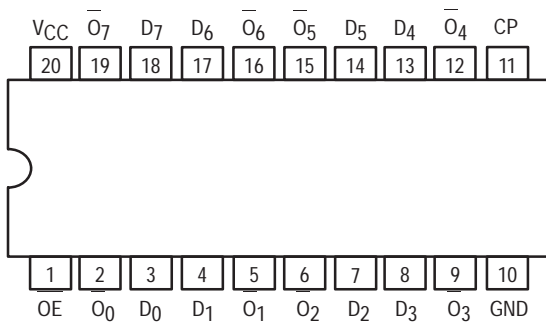


OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

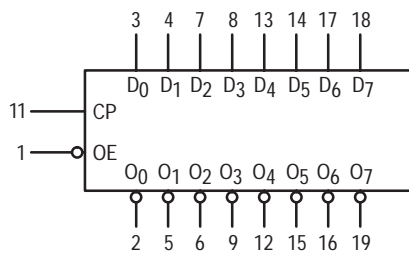
The MC54/74F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The F534 is the same as the F374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications

CONNECTION DIAGRAM



LOGIC SYMBOL

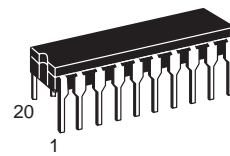


V_{CC} = PIN 20
GND = PIN 10

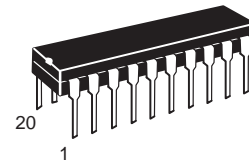
MC54/74F534

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

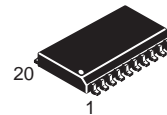
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

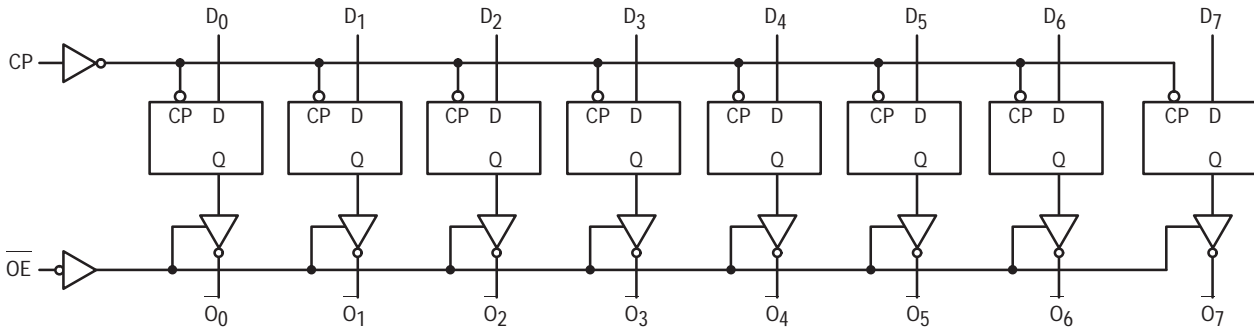
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74		-3.0	mA	
I _{OL}	Output Current — Low	54, 74		24	mA	

MC54/74F534

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the

LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCZ}	Power Supply Current		55	86	mA	D _n = Gnd OE = 4.5 V	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F534

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100			60		70		MHz
t _{pLH} t _{pHL}	Propagation Delay CP to O _n	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11	4.0 4.0	10 10	ns
t _{pZH} t _{pZL}	Output Enable Time	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14 10	2.0 2.0	12.5 8.5	ns
t _{pHZ} t _{pLZ}	Output Disable Time	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	2.0 2.0	8.0 6.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to CP	2.0 2.0			2.5 2.0		2.0 2.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to CP	2.0 2.0			2.0 2.5		2.0 2.0		
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns

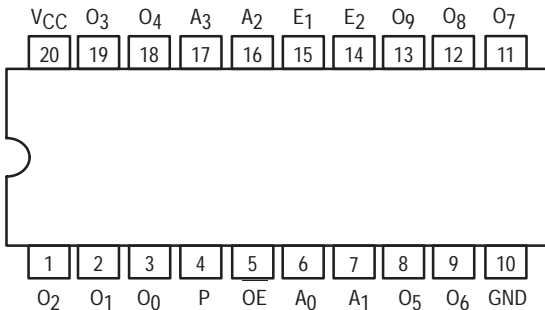


1-OF-10 DECODER WITH 3-STATE OUTPUTS

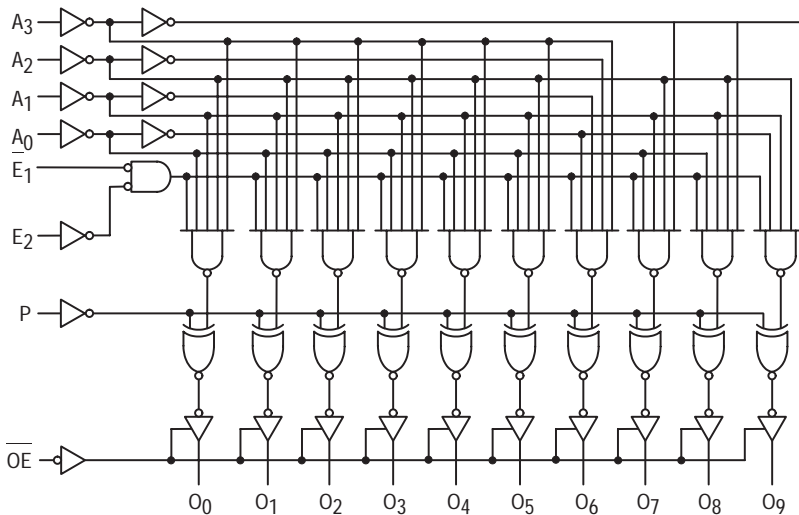
The MC54/74F537 is a one-of-ten decoder/demultiplexer with four active HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active LOW or active HIGH. The MC54/74F537 has 3-state outputs, and a HIGH signal on the Output Enable (OE) input forces all outputs to the high impedance state. Two input enables, active HIGH E₂ and active LOW E₁, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

- Demultiplexing Capability
- 3-State Outputs
- Multiple Input Enable for Expansion
- Polarity Control Input
- ESD Protection > 4000 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM

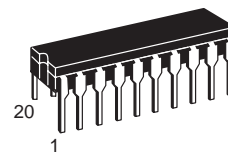


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

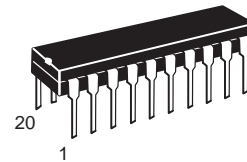
MC54/74F537

1-OF-10 DECODER WITH 3-STATE OUTPUTS

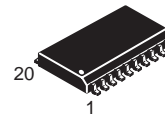
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

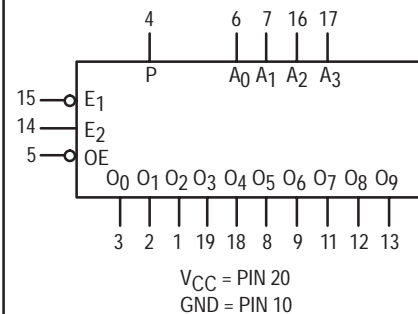


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

LOGIC SYMBOL



MC54/74F537

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4		V	I _{OH} = -3.0 mA V _{CC} = 4.5 V
		74	2.7		V	I _{OH} = -3.0 mA V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 24 mA V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CCZ}	Power Supply Current		44	66	mA	V _{CC} = MAX: A ₀ -A ₃ , E ₁ = GND OE, E ₂ , P = HIGH

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0 to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to O _n	4.0 2.5		14 11	3.5 2.0	19 15	3.5 2.0	16 12	ns
t _{PLH} t _{PHL}	Propagation Delay E ₁ to O _n	4.0 3.0		11 11	4.0 3.0	14 14	4.0 3.0	12 12	
t _{PLH} t _{PHL}	Propagation Delay E ₂ to O _n	6.0 4.0		11.5 11.5	5.0 4.0	15 14.5	5.0 4.0	13 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay P to O _n	5.0 3.5		16 11.5	5.0 3.5	21 13	4.5 3.5	17 12	
t _{PZH} t _{PZL}	Output Enable Time OE to O _n	2.5 4.0		7.0 8.0	2.5 4.0	11 10	2.5 4.0	8.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to O _n	1.5 1.5		6.0 6.5	1.0 1.0	8 8	1.0 1.0	7.0 7.0	

MC54/74F537

TRUTH TABLE

FUNCTION	INPUTS							OUTPUTS										
	OE	E ₁	E ₂	A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	O ₉	
HIGH Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	
Disable	L L	H X	X L	X X	X X	X X	X X	Outputs Equal P Input										
Active HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
	L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L	
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	
	L	L	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	
	L	L	H	L	H	H	X	H	X	L	L	L	L	L	L	L	L	
	L	L	H	L	H	H	X	X	L	L	L	L	L	L	L	L	L	
	Active LOW Output (P = H)	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
		L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
		L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
		L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
		L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
		L	L	H	L	H	H	L	H	H	H	H	L	H	H	H	H	H
L		L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L		L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L		L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L		L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

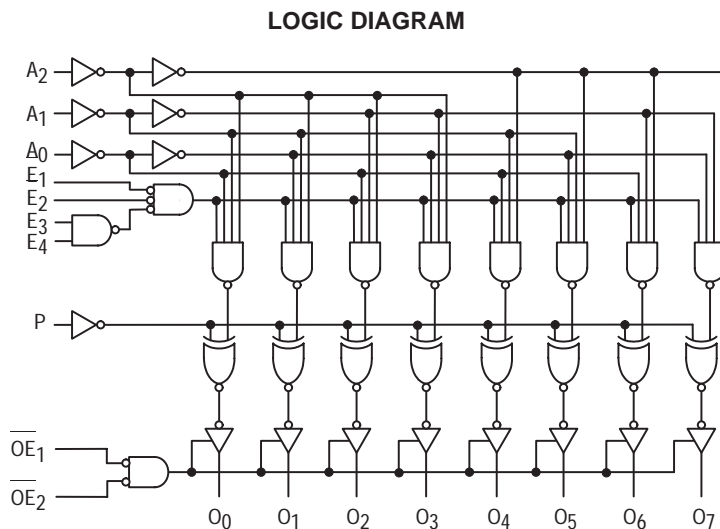
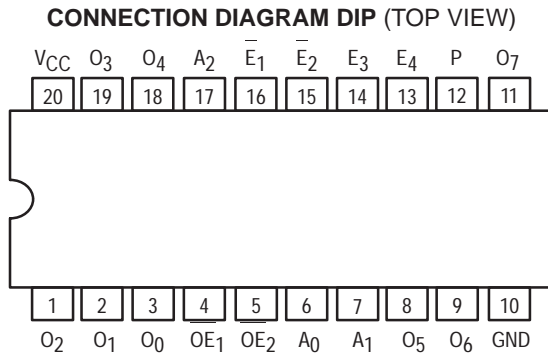
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance



1-OF-8 DECODER WITH 3-STATE OUTPUTS

The MC54/74F538 decoder/demultiplexer accepts three Address (A_0 – A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable (OE) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

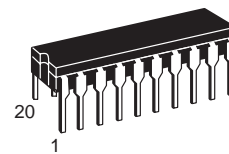
- Output Polarity Control
- Data Demultiplexing Capability
- Multiple Enables for Expansion
- 3-State Outputs
- ESD Protection > 4000 Volts



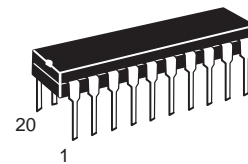
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F538

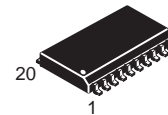
**1-OF-8 DECODER
WITH 3-STATE OUTPUTS**
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 732-03**



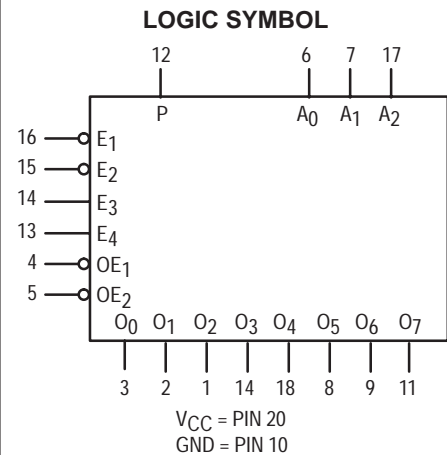
**N SUFFIX
PLASTIC
CASE 738-03**



**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC



MC54/74F538

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4		V	I _{OH} = -3.0 mA, V _{CC} = 4.5 V
		74	2.7		V	I _{OH} = -3.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 24 mA, V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V, V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V, V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CCZ}	Power Supply Current		37	56	mA	V _{CC} = MAX: A ₀ -A ₂ , E ₁ , E ₂ = GND OE ₁ , OE ₂ , E ₃ , E ₄ , P = HIGH

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0 to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to O _n	4.0 3.0	11 7.5	13 12.5	4.0 3.0	17 16.5	4.0 3.0	14 13.5	ns
t _{PLH} t _{PHL}	Propagation Delay E ₁ or E ₂ to O _n	4.0 3.0	8.5 6.5	12 12	3.5 3.0	15 14.5	3.5 3.0	13 12.5	
t _{PLH} t _{PHL}	Propagation Delay E ₃ or E ₄ to O _n	6.5 4.0	11 10	12.5 12.5	5.5 3.5	15.5 15	5.5 3.5	13.5 13	ns
t _{PLH} t _{PHL}	Propagation Delay P to O _n	4.5 3.5	11.5 11	15 11.5	4.0 3.5	18.5 12.5	4.0 3.5	16.5 12	
t _{PZH} t _{PZL}	Output Enable Time OE ₁ or OE ₂ to O _n	2.5 4.0	5.5 9.0	9.5 13.5	2.0 4.0	13 16	2.0 4.0	11 15	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE ₁ or OE ₂ to O _n	1.0 1.0	4.0 5.0	6.0 8.5	1.0 1.0	8.0 10.5	1.0 1.0	7.0 9.5	

MC54/74F538

TRUTH TABLE

FUNCTION	INPUTS									OUTPUTS							
	OE ₁	OE ₂	E ₁	E ₂	E ₃	E ₄	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

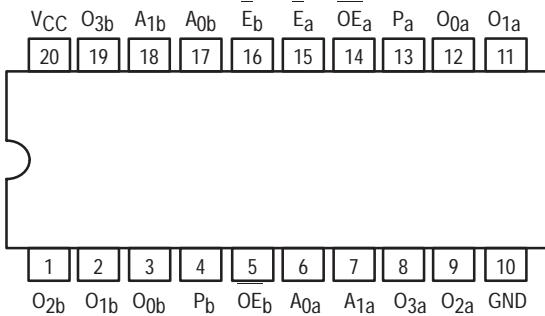


DUAL 1-OF-4 DECODER WITH 3-STATE OUTPUTS

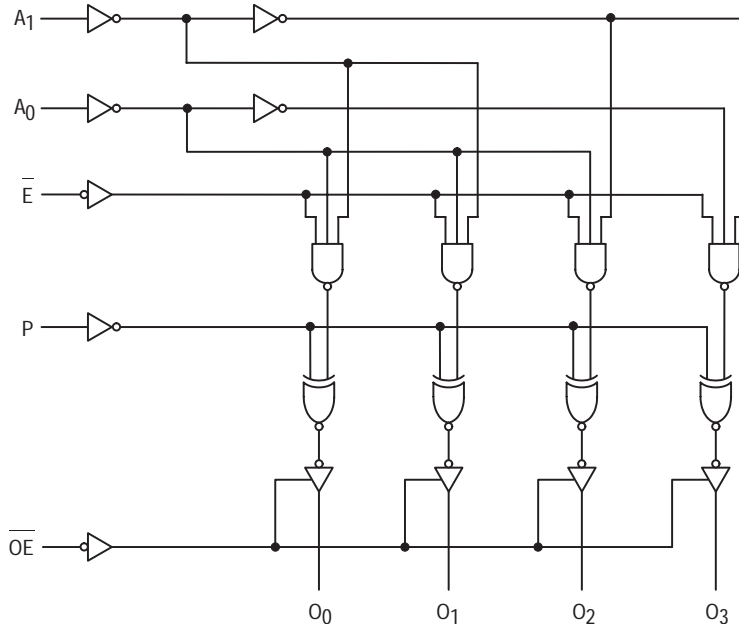
The MC54/74F539 contains two independent decoders. Each accepts two Address (A_0 – A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH ($P = L$) or active LOW ($P = H$). An active LOW input Enable (E) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH Signal on the active LOW Output Enable (OE) input forces the 3-state outputs to the high impedance state.

- Demultiplexing Capability
- 3-State Outputs
- Two Completely Independent 1-of-4 Decoders
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD Protection > 4000 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC DIAGRAM (1/2 SHOWN)

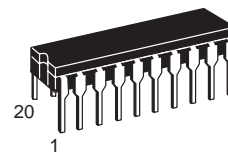


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

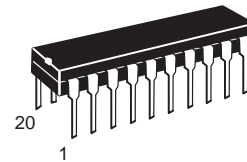
MC54/74F539

DUAL 1-OF-4 DECODER WITH 3-STATE OUTPUTS

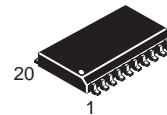
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

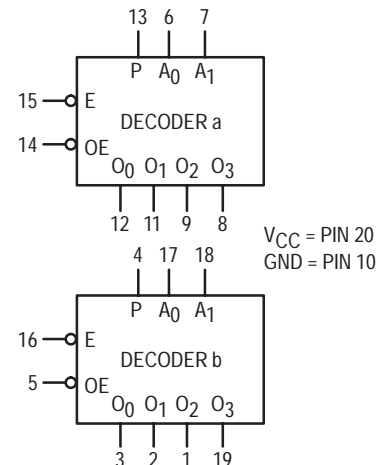


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

LOGIC SYMBOL



MC54/74F539

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4		V	I _{OH} = -3.0 mA, V _{CC} = 4.5 V
		74	2.7		V	I _{OH} = -3.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 24 mA, V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V, V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V, V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CCZ}	Power Supply Current		40	60	mA	V _{CC} = MAX, A ₀ , A ₁ , E = GND OE, P = HIGH

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0 to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to O _n	3.5 3.0		12.5 12.5	3.0 2.5	18.5 16	3.0 2.5	13.5 13	ns
t _{PLH} t _{PHL}	Propagation Delay E to O _n	3.0 3.0		11 11	2.5 3.0	14 13.5	3.0 3.0	12 11.5	ns
t _{PLH} t _{PHL}	Propagation Delay P to O _n	4.0 3.5		9.5 9.5	3.5 3.0	12.5 11.5	3.5 3.0	10.5 10	ns
t _{PLH} t _{PHL}	Propagation Delay P to O _n	5.0 3.0		14.5 9.0	4.0 3.0	19.5 11.5	4.0 3.0	15.5 9.5	ns
t _{PZH} t _{PZL}	Output Enable Time OE to O _n	2.5 4.0		7.5 10	2.0 3.5	10.5 13.5	2.0 3.5	8.5 11.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to O _n	1.5 2.0		6.0 8.0	1.0 1.5	7.5 9.5	1.0 1.5	6.5 8.5	

MC54/74F539

TRUTH TABLE (each half)

Function	Inputs				Outputs			
	OE	E	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	O _n = P			
Active HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

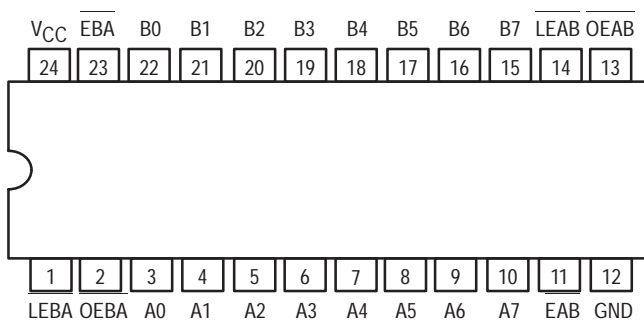


OCTAL REGISTERED TRANSCEIVER, NON-INVERTING, 3-STATE

The MC74F543 Octal Registered Transceivers contain two sets of data flowing in either direction. Separate Latch Enable (LEAB, LEBA) and Enable (OEAB, OEBA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F543 has a noninverting data path. The A outputs are guaranteed to sink 20 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Non-Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F544 for Inverting Version
- ESD Protection > 4000 Volts

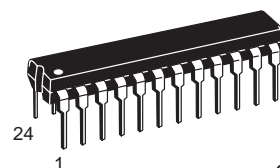
PIN ASSIGNMENT



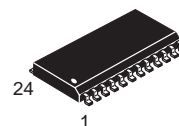
MC74F543

OCTAL REGISTERED
TRANSCEIVER,
NON-INVERTING, 3-STATE

FAST™ SCHOTTKY TTL



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current — High	74		-3.0/-15	mA
I _{OL}	Output Current — Low	74		24/64	mA

MC74F543

FUNCTION TABLE

Inputs				Outputs	Status
OEXX	EXX	LEXX	Data		
H	X	X	X	Z	Outputs disabled
L	H	L	l	Z	Outputs disabled
L	H	L	h	Z	Data latched
L	L	H	l	L	Data latched
L	L	H	h	H	Data latched
L	L	L	L	L	Transparent
L	L	L	H	H	Transparent

H = HIGH voltage level; h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); L = LOW Voltage Level; l = LOW state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); X = Don't care; Z = HIGH impedance state.

FUNCTIONAL DESCRIPTION

The MC74F543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable (EAB) Input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH

transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflects the data present at the output of the A latches. Control of data flow from B to A is similar, but using the EBA, LEBA, and OEBA inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	A0–A7	74	2.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		B0–B7	74	2.7	3.4			V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	A0–A7	74	2.0		V	I _{OL} = -15 mA	V _{CC} = 4.5 V
		B0–B7	74		0.35			0.5
I _{IH}	Input HIGH Current		I/O Pins			1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V
			Control Pins			100		μA
I _{IL}	Input LOW Current		EAB, EBA			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
			Other Inputs			-0.6		
I _{OZH}	Off-State Output Current, High-Level Voltage Applied					70	μA	V _{OUT} = 2.7 V
						1.0		mA
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied					-600	μA	V _{CC} = MAX, V _{OUT} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)		A _n Outputs	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
			B _n Outputs	-100		-225		
I _{CC}	Total Supply Current		I _{CC} H		70	100	mA	V _{CC} = MAX
			I _{CC} L		95	125		
			I _{CC} Z		95	125		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F543

AC ELECTRICAL CHARACTERISTICS

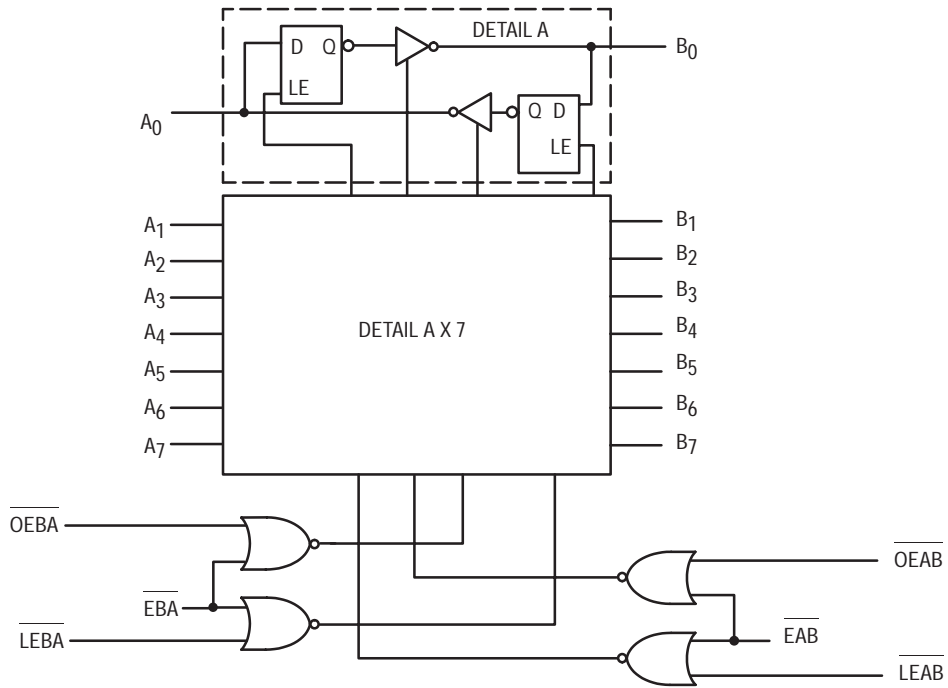
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	70	100		70		MHz
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	3.0 3.0	5.5 5.0	7.5 6.5	3.0 3.0	8.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEAB to B _n	4.5 4.5	8.5 8.5	11 11	4.5 4.5	12.5 12.5	ns
t _{PZH} t _{PZL}	Output Enable Time to OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	3.0 4.0	7.0 7.5	9.0 10.5	3.0 4.0	10 12	ns
t _{PHZ} t _{PLZ}	Output Disable Time to OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	2.5 2.0	6.0 5.5	8.0 7.5	2.5 2.0	9.0 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Setup Time, <u>HIGH</u> or <u>LOW</u> A _n or B _n to LEBA or LEAB	3.0 3.0			3.5 3.5			ns
t _{h(H)} t _{h(L)}	Hold Time, <u>HIGH</u> or <u>LOW</u> A _n to B _n to LEBA or LEAB	3.0 3.0			3.5 3.5			ns
t _{w(L)}	Latch Enable, B to A Pulse Width, LOW	8.0			9.0			ns

MC74F543

LOGIC DIAGRAM



NOTE:

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

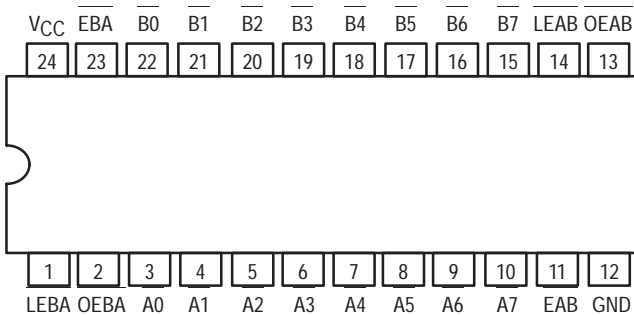


OCTAL REGISTERED TRANSCEIVER, INVERTING, 3-STATE

The MC74F544 Octal Registered Transceivers contain two sets of D-Type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LEAB, LEBA) and Enable (OEAB, OEBA) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The MC74F544 has an inverting data path. The A outputs are guaranteed to sink 24 mA while the B outputs are rated for 64 mA.

- Combines 74F245 and 74F373 Type Functions in One Chip
- 8-Bit Octal Transceiver
- Inverting
- Back-to-Back Registers for Storage
- Separate Controls for Data Flow in Each Direction
- Glitchless Outputs During 3-State Power Up or Power Down Operation
- High Impedance Outputs in Power Off State
- A Outputs Sink 24 mA and Source 3.0 mA
- B Outputs Sink 64 mA and Source 15 mA
- See F543 for Noninverting Version
- ESD Protection > 4000 Volts

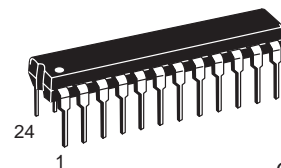
PIN ASSIGNMENT



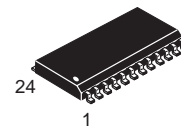
MC74F544

OCTAL REGISTERED
TRANSCEIVER, INVERTING,
3-STATE

FAST™ SCHOTTKY TTL



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	DC Supply Voltage	74	4.5	5.5	V
T _A	Operating Ambient Temperature Range	74	0	70	°C
I _{OH}	Output Current — High	74	—	—	-3.0/-15 mA
I _{OL}	Output Current — Low	74	—	—	24/64 mA

MC74F544

FUNCTION TABLE

Inputs				Outputs	Status
OEXX	EXX	LEXX	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L	↑	L	l	Z	Outputs disabled
L	↑	L	h	Z	Data latched
L	L	↑	l	H	Data latched
L	L	↑	h	L	Data latched
L	L	L	L	H	Transparent
L	L	L	H	L	Transparent
L	L	H	X	NC	Hold

H = HIGH voltage level; h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); L = LOW voltage level; l = LOW state must be present one set-up time before the LOW-to-HIGH transition of LEXX or EXX (XX = AB or BA); X = Don't care; Z = HIGH impedance state; NC = No Change.

FUNCTIONAL DESCRIPTION

The MC74F544 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable (EAB) input must be LOW in order to enter data from A0–A7 or take data from B0–B7, as indicated in the Function Table. With EAB LOW, a LOW signal on the A-to-B latch enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH

transition of the LEAB signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With EAB and OEAB both LOW, the 3-State B output buffers are active and reflect the inverted data present at the output of the A latches. Control of data flow from B to A is similar, but using the EBA, LEBA, and OEBA inputs.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions (Note 1)		
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0	—	—	V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage		—	—	0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage		—	-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	A0–A7	74	2.4	—	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		B0–B7	74	2.0	—	—			V
V _{OL}	Output LOW Voltage	A0–A7	74	—	0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
		B0–B7	74	—	0.4	0.55			
I _{IH}	Input HIGH Current	I/O Pins	—	—	1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V		
		Control Pins	—	—	100			μA	V _{CC} = MAX, V _{IN} = 7.0 V
		Control Pins	—	—	20			μA	V _{CC} = MAX, V _{IN} = 2.7 V
		I/O Pins	—	—	70			μA	
I _{IL}	Input LOW Current	EAB, EBA	—	—	-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V		
		Other Inputs	—	—	-0.6				
I _{OZH}	Off-State Output Current		—	—	70	μA	V _{CC} = MAX, V _{OUT} = 2.7 V		
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied		—	—	-600	μA	V _{CC} = MAX, V _{OUT} = 0.5 V		
I _{OS}	Output Short Circuit Current (Note 2)	A _n Outputs	-60	—	-150	mA	V _{CC} = MAX, V _{OUT} = 0 V		
		B _n Outputs	-100	—	-225				
I _{CC}	Total Supply Current	I _{CC} H	—	70	105	mA	V _{CC} = MAX		
		I _{CC} L	—	95	130				
		I _{CC} Z	—	95	125				

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F544

AC ELECTRICAL CHARACTERISTICS

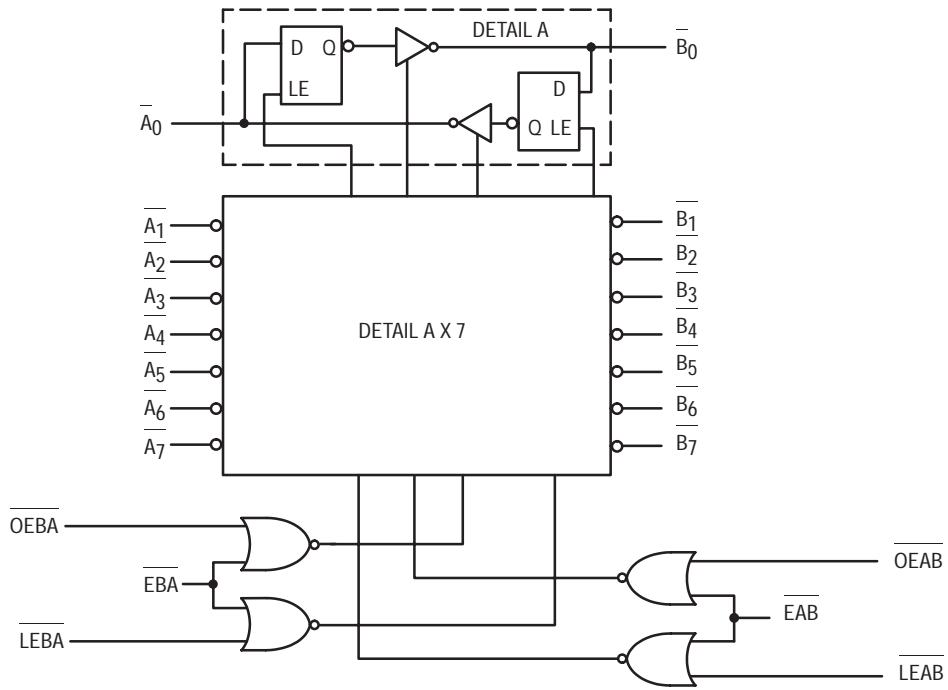
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Transparent Mode A _n to B _n or B _n to A _n	2.0 2.0	— —	9.5 6.5	2.0 2.0	10.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to A _n	6.0 4.0	— —	13 9.5	6.0 4.0	14.5 10.5	ns
t _{PLH} t _{PHL}	Propagation Delay LEAB to B _n	6.0 4.0	— —	13 9.5	6.0 4.0	14.5 10.5	ns
t _{PZH} t _{PZL}	Output Enable Time OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	3.0 4.0	— —	9.0 10.5	3.0 4.0	10 12	ns
t _{PHZ} t _{PLZ}	Output Disable Time OEBA or OEAB to A _n or B _n EBA or EAB to A _n or B _n	1.5 1.5	— —	8.0 7.5	1.5 1.5	9.0 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Setup Time, HIGH or LOW A _n or B _n to LEBA or LEAB	3.0 3.0	— —	— —	3.0 3.0	— —	— —	ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW A _n to B _n to LEBA or LEAB	3.0 3.0	— —	— —	3.0 3.0	— —	— —	ns
t _{w(L)}	Latch Enable, B to A Pulse Width, LOW	6.0	—	—	7.5	—	—	ns

MC74F544

LOGIC DIAGRAM



NOTE:

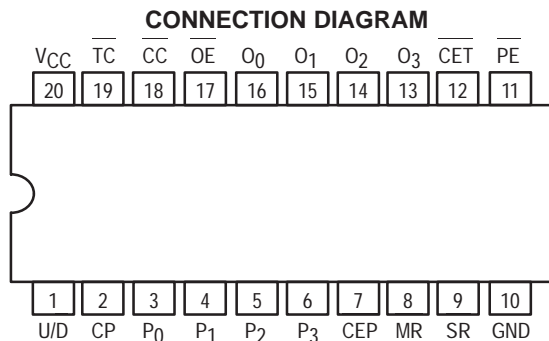
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



4-BIT BIDIRECTIONAL COUNTERS (WITH 3-STATE OUTPUTS)

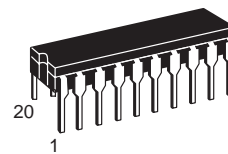
The MC54/74F568 and MC54/74F569 are fully synchronous, reversible counters with 3-state outputs. The F568 is a BCD decade counter; the F569 is a binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/D input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry (CC) and Terminal Count (TC) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable (OE) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

- 4-Bit Bidirectional Counting
 - F568 Decade Counter
 - F569 Binary Counter
- Synchronous Counting and Loading
- Lookahead Carry Capability for Easy Cascading
- Preset Capability for Programmable Operation
- 3-State Outputs for Bus Organized Systems
- Master Reset (MR) Overrides All Other Inputs
- Synchronous Reset (SR) Overrides Counting and Parallel Loading

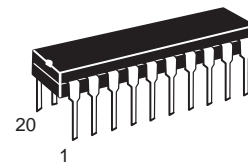


**MC54/74F568
MC54/74F569**

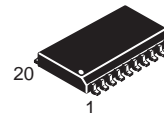
**4-BIT
BIDIRECTIONAL
COUNTERS
(WITH 3-STATE OUTPUTS)**
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 732-03**



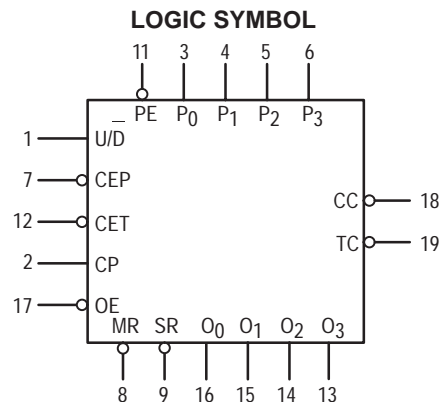
**N SUFFIX
PLASTIC
CASE 738-03**



**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC



MC54/74F568 • MC54/74F569

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

FUNCTIONAL DESCRIPTION

The F568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The F569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset (MR), Synchronous Reset (SR), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — plus the Up/Down (U/D) input, determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on SR overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With MR, SR and PE HIGH, CEP and CET permit counting when both are LOW. Conversely, a HIGH signal on either CEP or CET inhibits counting.

The F568 and F569 use edge-triggered flip-flops and changing the SR, PE, CEP, CET or U/D inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally HIGH and goes LOW providing CET is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the F568, 15 for the F569) in the Up mode. TC will then remain LOW until a state change occurs, whether by counting or pre-setting, or until U/D or CET is changed. To implement synchronous multistage counters, the connections between the TC output and the CEP and CET inputs can provide either slow or fast carry propagation. Figure A shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure B are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 (F568) or 16 (F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock peri-

od is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry (CC) output is provided. The CC output is normally HIGH. When CEP, CET, and TC are LOW, the CC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the CC Truth Table. When the Output Enable (OE) is LOW, the parallel data outputs O₀–O₃ are active and follow the flip-flop Q outputs. A HIGH signal on OE forces O₀–O₃ to the High Z state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:



Count Enable = CEP · CET · PE

Up (F568): TC = Q₀ · Q₁ · Q₂ · Q₃ · (Up) · CET

(F569): TC = Q₀ · Q₁ · Q₂ · Q₃ · (Up) · CET

Down (Both): TC = Q₀ · Q₁ · Q₂ · Q₃ · (Down) · CET


CC TRUTH TABLE

Inputs						Output
SR	PE	CEP	CET	TC*	CP	CC
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L		

* = TC is generated internally

X = Don't Care

L = LOW Voltage Level

 = Low Pulse

H = HIGH Voltage Level

FUNCTION TABLE

Inputs							Operating Mode
MR	SR	PE	CEP	CET	U/D	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	l	X	X	X	X	↑	Synchronous reset
h	h	l	X	X	X	↑	Parallel load
h	h	h	l	l	h	↑	Count up (increment)
h	h	h	l	l	l	↑	Count down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = HIGH voltage level

h = HIGH voltage level one setup prior to the Low-to-High Clock transition

L = LOW voltage level

l = LOW voltage level one setup prior to the Low-to-High clock transition

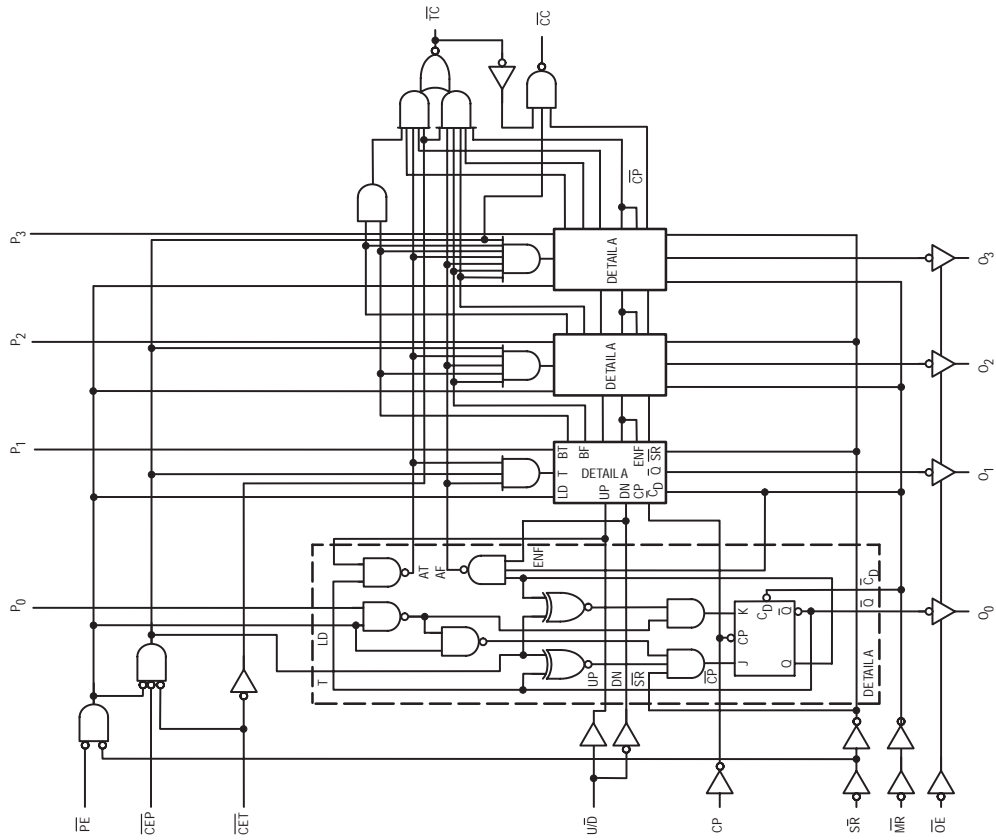
X = Don't care

↑ = Low-to-High clock transition

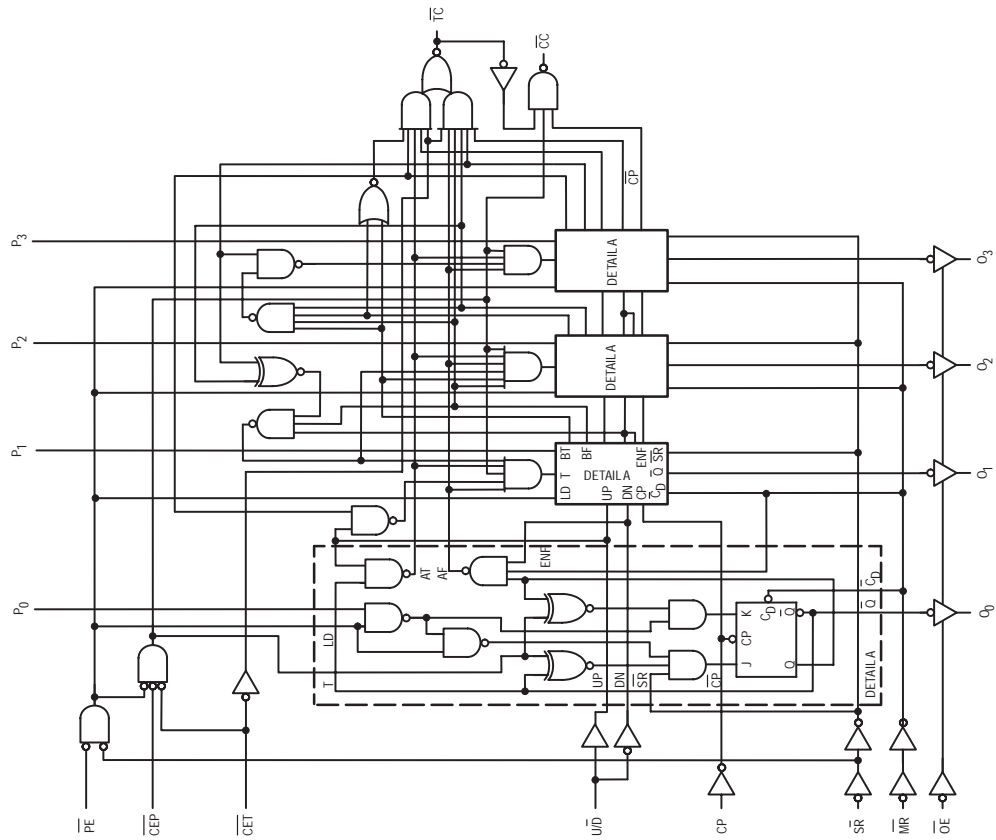
MC54/74F568 • MC54/74F569

LOGIC DIAGRAMS

MC54/74F569



MC54/74F568



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F568 • MC54/74F569

Figure A. Multistage Counter with Ripple Carry

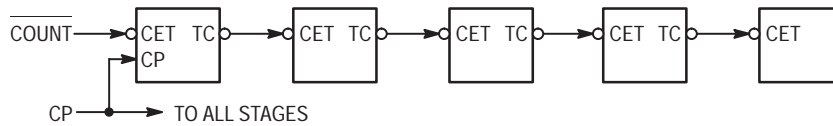
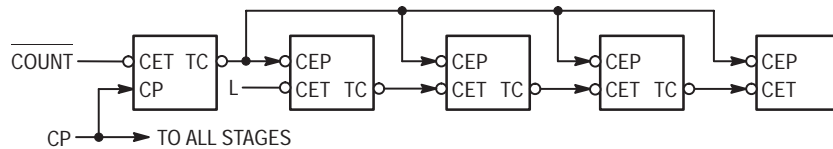


Figure B. Multistage Counter with Lookahead Carry



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.3	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH			50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW			-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current PE, CET Others			-1.2 -0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current (ALL Outputs OFF)			67	mA	V _{CC} = MAX	

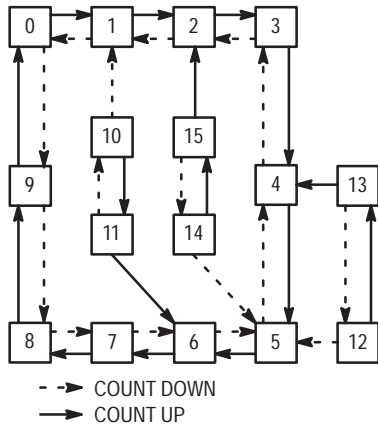
NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

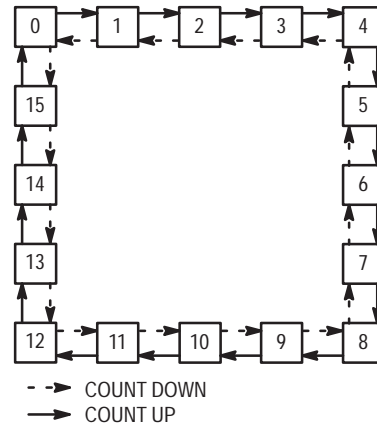
MC54/74F568 • MC54/74F569

STATE DIAGRAMS

MC54/74F568



MC54/74F569



AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100		60		85		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to O _n (PE HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t _{PLH} t _{PHL}	Propagation Delay CP to TC	5.5 4.0	15.5 11	5.5 4.0	18.5 13.5	5.5 4.0	17.5 12.5	ns
t _{PLH} t _{PHL}	Propagation Delay CET to TC	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t _{PLH} t _{PHL}	Propagation Delay U/D to TC ('F568)	3.5 4.0	11 16	3.5 4.0	13.5 19	3.5 4.0	12.5 18	ns
t _{PLH} t _{PHL}	Propagation Delay U/D to TC ('F569)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns
t _{PLH} t _{PHL}	Propagation Delay CP to CC	2.5 2.0	7.0 6.0	2.5 2.0	9.0 8.0	2.5 2.0	8.0 7.0	ns
t _{PLH} t _{PHL}	Propagation Delay CEP, CET to CC	2.5 4.0	6.5 11	2.5 4.0	8.5 13.5	2.5 4.0	7.5 12.5	ns
t _{PHL}	Propagation Delay MR to O _n	5.0	13	5.0	15.5	5.0	14.5	ns
t _{PZH} t _{PZL}	Output Enable Time OE to O _n	2.5 3.0	7.0 8.0	2.5 3.0	9.0 10	2.5 3.0	8.0 9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time OE to O _n	1.5 2.0	6.5 6.0	1.5 2.0	8.5 8.0	1.5 2.0	7.5 7.0	ns

MC54/74F568 • MC54/74F569

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$		
		Min	Max	Min	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		5.5 5.5		4.5 4.5		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW CEP or CET to CP	5.0 5.0		7.0 7.0		6.0 6.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0		0 0		0 0		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW PE to CP	8.0 8.0		10 10		9.0 9.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW PE to CP	0 0		0 0		0 0		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW U/D to CP (F568)	11 16.5		13.5 18.5		12.5 17.5		ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW U/D to CP (F569)	11 7.0		13.5 10		12.5 8.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW U/D to CP	0 0		0 0		0 0		ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW SR to CP	10 8.0		12 10.5		11 9.5		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW SR to CP	0 0		0 0		0 0		
$t_W(H)$ $t_W(L)$	CP Pulse Width HIGH or LOW	4.0 6.0		6.0 8.0		4.5 6.5		ns
$t_W(L)$	MR Pulse Width, LOW	4.5		6.0		5.0		ns
t_{rec}	MR Recovery Time	6.0		8.0		7.0		ns



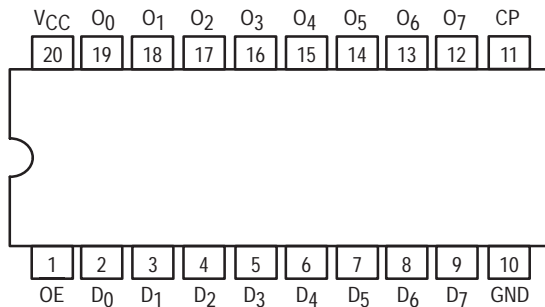
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC74F574 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered clock (CP) and Output Enable (OE) are common to all flip-flops.

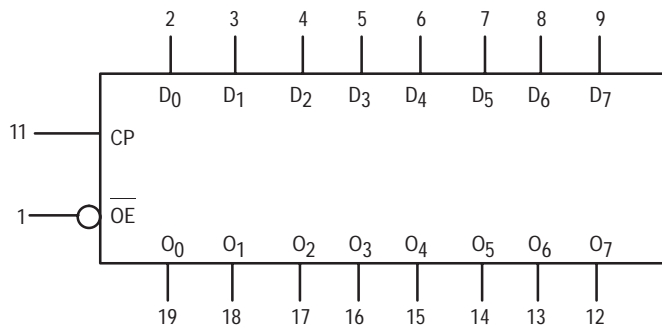
This device is functionally identical to the F374 except for the pinouts.

- Broadside Pinout Version of F374
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications
- ESD Protection > 4000 Volts

PIN ASSIGNMENT



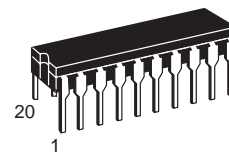
LOGIC SYMBOL



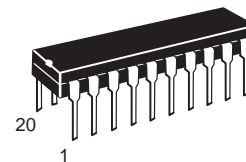
MC74F574

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

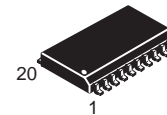
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	74	Min	Typ	Max	Unit
V _{CC}	DC Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74	—	—	3.0	mA
I _{OL}	Output Current — Low	74	—	—	24	mA

MC74F574

FUNCTION TABLE

Inputs			Internal Register	Outputs	Operating Mode
OE	CP	D _n		Q ₀ –Q ₇	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	‡	X	NC	NC	Hold
H	↑	D _n	D _n	Z	Disable outputs
H	X	X	X	Z	

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the Low-to-High clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

FUNCTIONAL DESCRIPTION

The MC74F574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements

on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

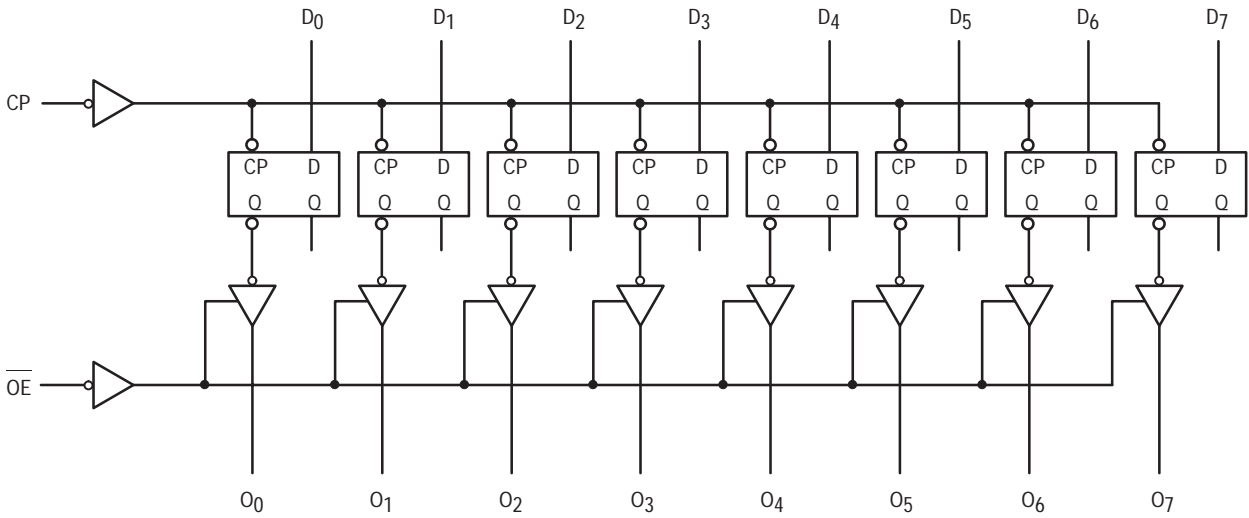
Symbol	Parameter	Limits			Unit	Test Conditions (Note 1)	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage	—	—	–1.2	V	V _{CC} = MIN, I _{IN} = –18 mA	
V _{OH}	Output HIGH Voltage	2.4	—	—	V	I _{OH} = –3.0 mA	V _{CC} = MIN
		2.7	—	—	V		V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	—	—	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current	—	—	20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		—	—	100		V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	—	—	–0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OZH}	Output Off Current — HIGH	—	—	50	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current — LOW	—	—	–50	μA	V _{CC} = MAX, V _{OUT} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)	–60	—	–150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CCZ}	Power Supply Current (All Outputs OFF)	—	55	86	mA	V _{CC} = MAX	D _n – GND; OE = 4.5 V

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F574

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	—	—	70	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CP to O _n	2.5	—	8.5	2.5	8.5	ns
t _{PZH} t _{PZL}	Output Enable Time	3.0	—	9.0	2.5	10.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	—	5.5	1.5	6.5	ns

AC OPERATING CHARACTERISTICS

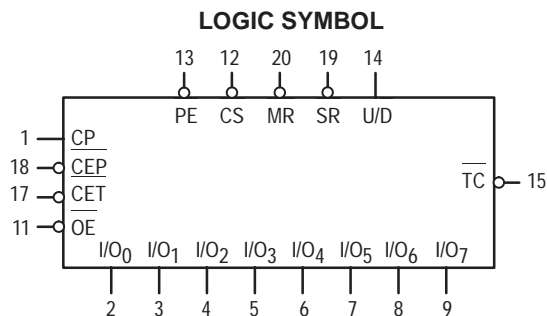
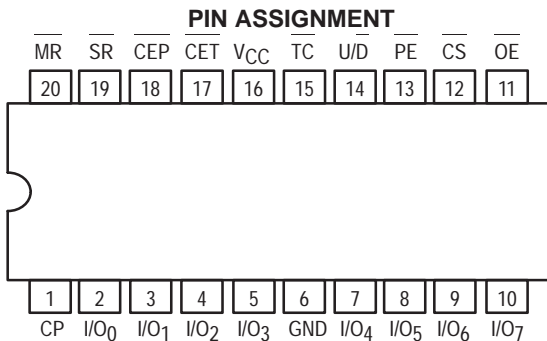
Symbol	Parameter	54/74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Setup Time, HIGH or LOW D _n to CP	2.5	—	—	2.5	—	—	ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH to LOW D _n to CP	2.0	—	—	2.0	—	—	ns
t _{w(H)} t _{w(L)}	CP Pulse Width HIGH or LOW	5.0	—	—	5.0	—	—	ns



8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

The MC74F579 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/D input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. TC output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

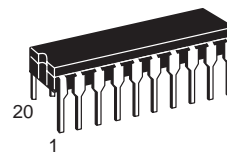
- Multiplexed 3-State I/O Ports For Bus-oriented Applications
- Built-In Cascading Carry Capability
- Count Frequency 115 MHz Typ
- Supply Current 100 mA Typ
- Fully Synchronous Operation
- U/D Pin to Control Direction of Counting
- Separate Pins for Master Reset and Synchronous Reset
- Center Power Pins to Reduce Effects of Package Inductance
- See F269 for 24-Pin Separate I/O Port Version
- See F779 for 16-Pin Version
- ESD Protection > 4000 Volts



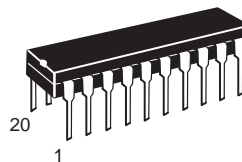
MC74F579

8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

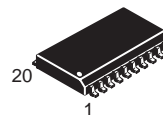
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current — High	TC		-1.0	mA
		I/O _n		-3.0	
I _{OL}	Output Current — Low	TC		20	mA
		I/O _n		24	

MC74F579

FUNCTION TABLE

MR	SR	CS	PE	CEP	CET	U/D	OE	CP	Function
X	X	H	X	X	X	X	X	X	I/O ₀ to I/O ₇ in Hi-Z (PE disabled)
X	X	L	H	X	X	X	H	X	I/O ₀ to I/O ₇ in Hi-Z
X	X	L	H	X	X	X	L	X	Flip-Flop outputs appear on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold (TC held high)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
 X = Don't care
 (not LL) = CS and PE should never both be low voltage at the same time

L = Low voltage level
 ↑ = Low-to-High clock transition

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	74F			Unit	Test Conditions (Note 1)		
		Min	Typ (2)	Max				
V _{OH}	Output HIGH Voltage	TC	2.5			V	I _{OH} = -1.0 mA V _{IL} = MAX V _{IH} = MIN	V _{CC} = 4.5 V
			2.7	3.4			V _{CC} = 4.75 V	
		I/O _n	2.4	3.3		V	I _{OH} = -3.0 mA V _{IL} = MAX V _{IH} = MIN	V _{CC} = 4.5 V
			2.7	3.3			V _{CC} = 4.75 V	
V _{OL}	Output LOW Voltage	TC		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = 4.5 V V _{IL} = MAX V _{IH} = MIN
		I/O _n					I _{OL} = 24 mA	
V _{IK}	Input Clamp Diode Voltage		-0.73	-1.2	V	V _{CC} = 4.5 V, I _{IN} = -18 mA		
I _{IH}	Input HIGH Current	I/O _n			1.0	mA	V _{CC} = 5.5 V	V _{IN} = 5.5 V
		others			100			μA
		I/O _n			70	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V	
		others			20			
I _{IL}	Input LOW Current	Except I/O _n			-0.6	mA		V _{CC} = 5.5 V, V _{IN} = 0.5 V
I _{OZH}	OFF-State Current High-Level Voltage Applied	I/O _n			70	μA	V _{CC} = 5.5 V	V _{OUT} = 2.7 V
I _{OZL}	OFF-State Current Low-Level Voltage Applied				-600			V _{OUT} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 3)		-60	-80	-150	mA		V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Total Supply Current (total)	I _{CCH}		95	135	mA	V _{CC} = MAX	
		I _{CCCL}		105	145			
		I _{CCZ}		105	150			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
- All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
- Not more than one output should be shorted at a time. For I_{OS} testing, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

MC74F579

AC ELECTRICAL CHARACTERISTICS

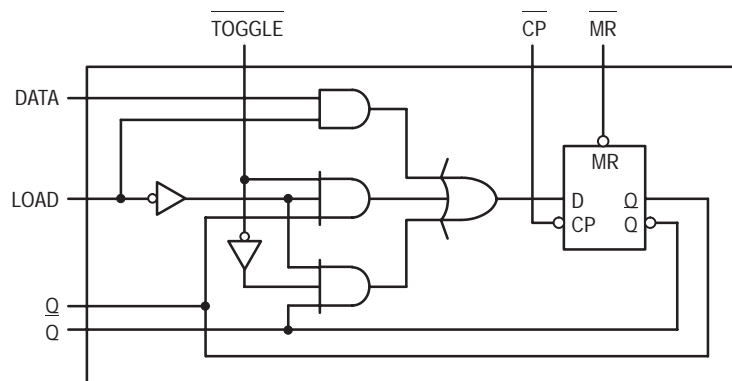
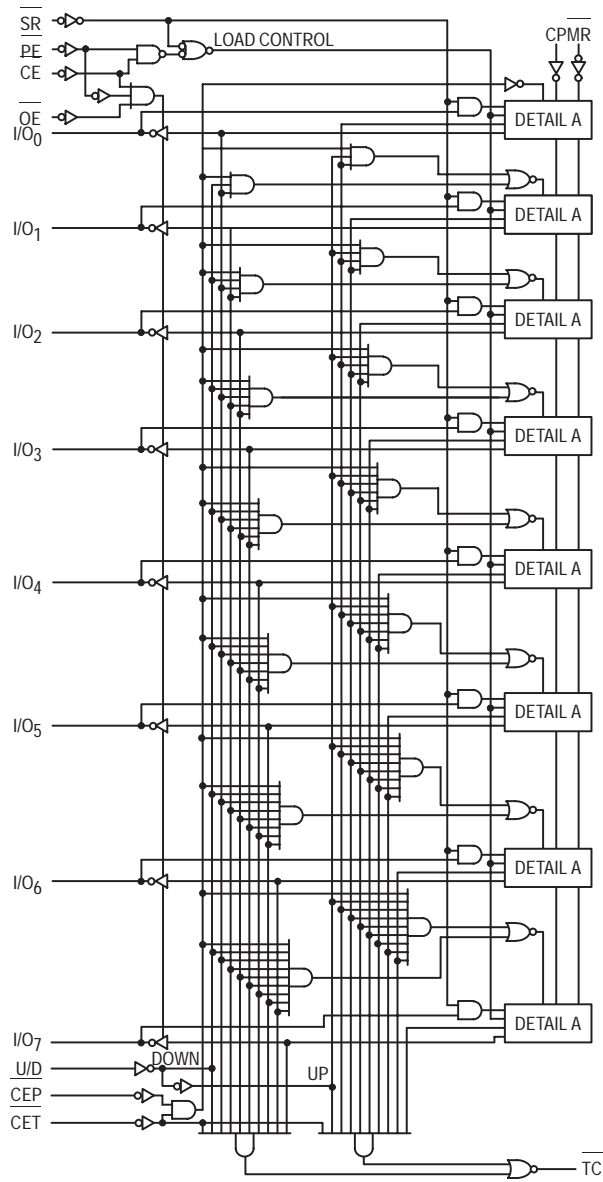
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100			80		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	5.0 5.0		10.5 10.5	5.0 5.0	11.5 11.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to TC	4.5 5.5		10 10	4.5 5.0	11 11	ns
t _{PLH} t _{PHL}	Propagation Delay U/D to TC	3.5 4.5		8.0 8.0	3.5 4.5	9.0 9.0	ns
t _{PLH} t _{PHL}	Propagation Delay CET to TC	3.5 3.5		7.0 8.0	3.5 3.5	8.5 8.5	ns
t _{PHL}	Propagation Delay MR to I/O _n	5.0		10	5.0	11	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level CS, PE to I/O _n	4.5 6.5		10.5 10.5	4.5 6.0	11.5 11.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time to HIGH or LOW Level CS, PE to I/O _n	3.0 4.0		7.5 9.5	3.0 4.0	9.0 11	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level OE to I/O _n	4.0 6.0		8.5 9.5	4.0 5.0	9.5 10.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time to HIGH or LOW Level OE to I/O _n	1.0 2.5		6.0 7.0	1.0 2.5	6.5 8.0	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Setup Time, HIGH or LOW I/O _n to CP	3.0 3.0			4.0 4.0			ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW I/O _n to CP	1.0 1.0			1.0 1.0			ns
t _{s(H)} t _{s(L)}	Setup Time, HIGH or LOW PE, SR or CS to CP	9.5 9.5			10 10			ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW PE, SR or CS to CP	0 0			0 0			ns
t _{s(H)} t _{s(L)}	Setup Time, HIGH or LOW CET, CEP to CP	5.0 9.0			5.5 10.5			ns
t _{h(H)} t _{h(L)}	Hold Time, HIGH or LOW CET, CEP to CP	0 0			0 0			ns
t _w	CP Pulse Width	4.5			6.0			ns
t _{w(L)}	MR Pulse Width	3.5			4.5			ns
t _{rec}	MR Recovery Time	4.0			4.5			ns

MC74F579

LOGIC DIAGRAM



Detail A



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS (INVERTING AND NONINVERTING)

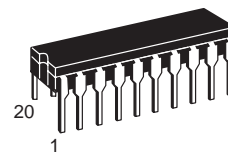
The MC74F620 is an octal bus transceiver featuring inverting 3-state bus-compatible outputs in both send and receive directions. The B_N outputs are capable of sinking 64 mA and sourcing up to 15 mA, providing very good capacitive drive characteristics. The MC74F623 is a non-inverting version of the MC74F620. These octal bus transceivers are designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibility in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs (OEBA and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the MC74F620 and MC74F623 the capability to store data by the simultaneous enabling of OEBA and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

- High Impedance NPN base inputs for reduced loading (70 μ A in High and Low states)
- Ideal for Applications which Require High Output drive and minimal bus loading
- Octal Bidirectional Bus Interface
- 3-State Buffer Outputs Sink 64 mA and Source 15 mA
- – F620 Inverting
- – F623 Noninverting
- ESD Protection > 4000 Volts

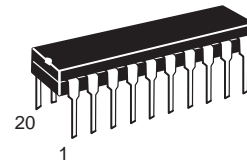
**MC74F620
MC74F623**

**OCTAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS
(INVERTING AND NONINVERTING)**

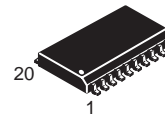
FAST™ SCHOTTKY TTL



**J SUFFIX
CERAMIC
CASE 732-03**



**N SUFFIX
PLASTIC
CASE 738-03**

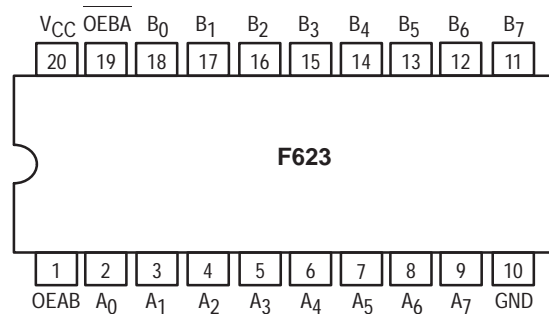
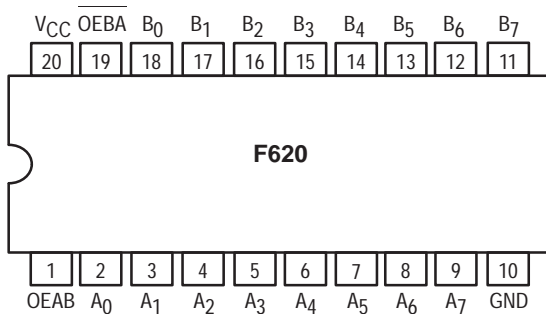


**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

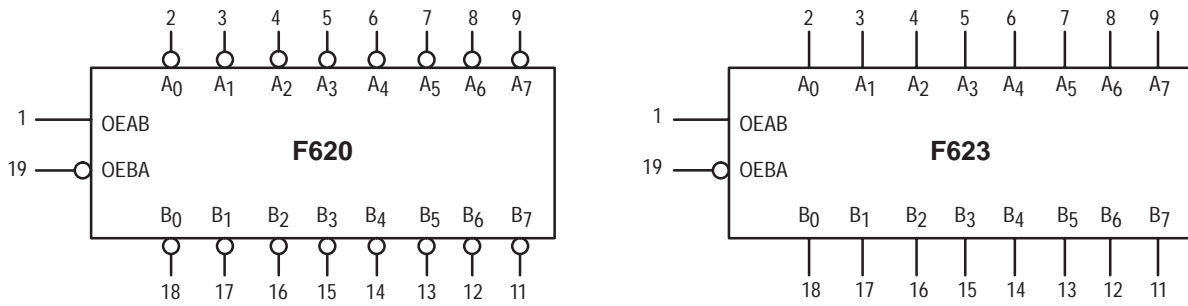
MC74FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

PIN ASSIGNMENTS



MC74F620 • MC74F623

LOGIC SYMBOLS



FUNCTION TABLE

Inputs		Operating Modes	
OEBA	OEAB	F620	F623
L	L	B data to A bus	B data to A bus
H	H	A data to B bus	A data to B bus
H	L	Z	Z
L	H	B data to A bus A data to B bus	B data to A bus A data to B bus

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = High impedance "off" state

GUARANTEED OPERATING RANGES

Symbol	Parameter		Limits			Unit	
			Min	Typ	Max		
V _{CC}	DC Supply Voltage	74	4.5	5.0	5.5	V	
T _A	Operating Ambient Temperature Range	74	0	25	70	°C	
I _{OH}	Output Current — High	A _n Outputs	74	—	—	-3.0	mA
I _{OH}	Output Current — High	B _n Outputs	74	—	—	-15	mA
I _{OL}	Output Current — Low	A _n Outputs	74	—	—	24	mA
I _{OL}	Output Current — Low	B _n Outputs	74	—	—	64	mA

MC74F620 • MC74F623

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

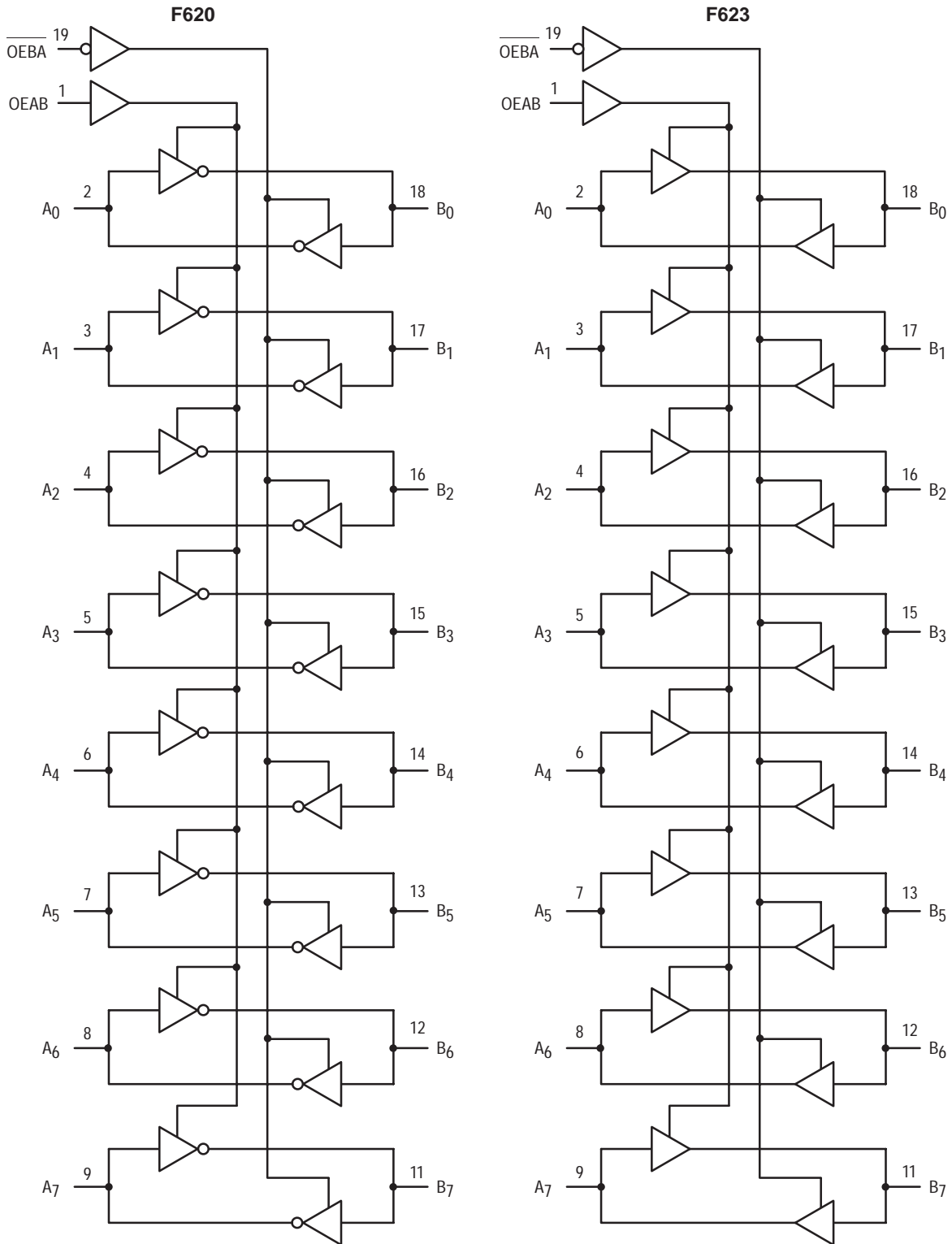
Symbol	Parameter		Limits			Unit	Test Conditions (Note 1)			
			Min	Typ	Max					
V _{IH}	Input HIGH Voltage		2.0	—	—	V	Guaranteed as a HIGH Signal			
V _{IL}	Input LOW Voltage		—	—	0.8	V	Guaranteed as a LOW Signal			
V _{IK}	Input Clamp Diode Voltage		—	—	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA			
V _{OH}	Output HIGH Voltage	A _n	74	2.4	3.3	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V	
			74	2.7	3.3	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V	
		B _n	74	2.4	3.4	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V	
			74	2.7	3.4	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V	
			74	2.0	—	—	V	I _{OH} = -15.0 mA	V _{CC} = 4.5 V	
V _{OL}	Output LOW Voltage	A _n	74	—	0.35	0.50	V	I _{OL} = 24 mA	V _{CC} = MIN	
V _{OL}	Output LOW Voltage	B _n	74	—	—	0.55	V	I _{OL} = 64 mA	V _{CC} = MIN	
I _{OZH} + I _{IH}	Output Off Current HIGH		—	—	70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V		
I _{OZL} + I _{IL}	Output Off Current LOW		—	—	-70	μA	V _{CC} = MAX	V _{OUT} = 0.5 V		
I _{IH}	Input HIGH Current		OEBA, OEAB	—	—	20	μA	V _{CC} = MAX, V _{IN} = 2.7 V		
			OEBA, OEAB	—	—	100	μA	V _{CC} = 0 V, V _{IN} = 7.0 V		
			Others	—	—	1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V		
I _{IL}	Input LOW Current		Non I/O Pins	—	—	-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V		
I _{OS}	Output Short Circuit Current (Note 2)		A ₀ -A ₇	-60	—	-150	mA	V _{CC} = MAX, V _{OUT} = GND		
			B ₀ -B ₇	-100	—	-225				
I _{CC}	Power Supply Current		F620	I _{CC} H	—	—	92	mA	V _{out} = HIGH	V _{CC} = MAX
				I _{CC} L	—	—	110		V _{out} = LOW	
				I _{CC} Z	—	—	92		V _{out} = HIGH Z	
I _{CC}	Power Supply Current		F623	—	—	120	mA	V _{CC} = MAX		

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F620 • MC74F623

LOGIC DIAGRAMS



MC74F620 • MC74F623

AC ELECTRICAL CHARACTERISTICS For F620

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n and B _n to A _n	2.5 1.0	— —	6.5 4.5	2.0 1.0	— —	7.5 5.0	ns
t _{PZH} t _{PZL}	Output Enable Time _____ to High or Low level, OEBA to A _n	3.0 4.0	— —	10.5 10.5	2.5 3.5	— —	11.5 11.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time _____ to High or Low level, OEBA to A _n	2.5 1.5	— —	7.5 7.0	2.0 1.0	— —	8.0 7.5	ns
t _{PZH} t _{PZL}	Output Enable Time _____ to High or Low level, OEAB to B _n	3.5 4.5	— —	10.5 10.0	3.5 4.0	— —	11.5 11.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time _____ to High or Low level, OEAB to B _n	3.0 3.0	— —	9.5 9.5	2.5 1.5	— —	10.5 10.5	ns

AC ELECTRICAL CHARACTERISTICS For F623

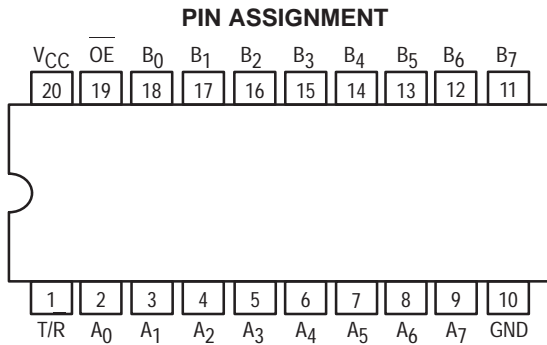
Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n	2.0 3.0	— —	5.5 7.0	2.0 2.5	— —	6.5 7.5	ns
t _{PLH} t _{PHL}	Propagation Delay B _n to A _n	2.0 3.0	— —	6.0 7.0	2.0 2.5	— —	6.5 7.5	ns
t _{PZH} t _{PZL}	Output Enable Time _____ to High or Low level, OEBA to A _n	3.5 5.0	— —	10.5 9.5	3.5 5.0	— —	12.0 10.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time _____ to High or Low level, OEBA to A _n	1.5 1.5	— —	6.5 6.5	1.5 1.5	— —	7.5 7.0	ns
t _{PZH} t _{PZL}	Output Enable Time _____ to High or Low level, OEAB to B _n	3.5 4.5	— —	10.0 9.0	3.5 4.5	— —	11.5 9.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time _____ to High or Low level, OEAB to B _n	3.0 4.0	— —	8.5 9.0	3.0 2.0	— —	10.0 10.0	ns



OCTAL BUS TRANSCEIVER, INVERTING WITH 3-STATE OUTPUTS

The MC74F640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64 mA and sourcing 15 mA, providing very good capacitive drive characteristics. The device features an Output Enable (OE) input for easy cascading and Transmit/Receive (T/R) input for direction control. The 3-state outputs, B₀–B₇, have been designed to prevent output bus loading if the power is removed from the device.

- High-Impedance NPN Base Inputs for Reduced Loading (70 μA in High and Low States)
- Ideal for Applications which Require High-Output Drive and Minimal Bus Loading
- Inverting Version of F245
- Octal Bidirectional Bus Interface
- 3-State Buffer Outputs Sink 64 mA and Source 15 mA
- ESD Sensitive — 4000 V HBM



FUNCTION TABLE

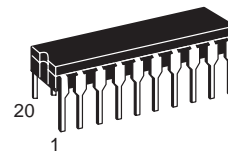
Inputs		Outputs
OE	T/R	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance "Off" State

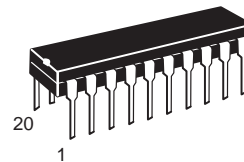
MC74F640

OCTAL BUS TRANSCEIVER, INVERTING WITH 3-STATE OUTPUTS

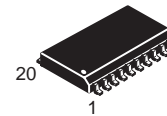
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

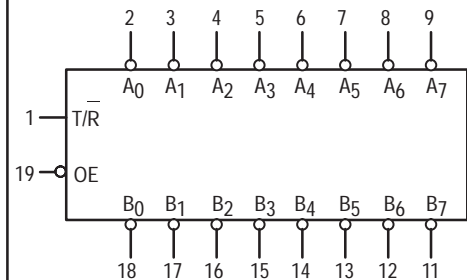


DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

LOGIC SYMBOL



MC74F640

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit	
V _{CC}	DC Supply Voltage		74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range		74	0	25	70	°C
I _{OH}	Output Current — High	A _n Outputs	74			-3.0	mA
I _{OH}	Output Current — High	B _n Outputs	74			-15	mA
I _{OL}	Output Current — Low	A _n Outputs	74			24	mA
I _{OL}	Output Current — Low	B _n Outputs	74			64	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

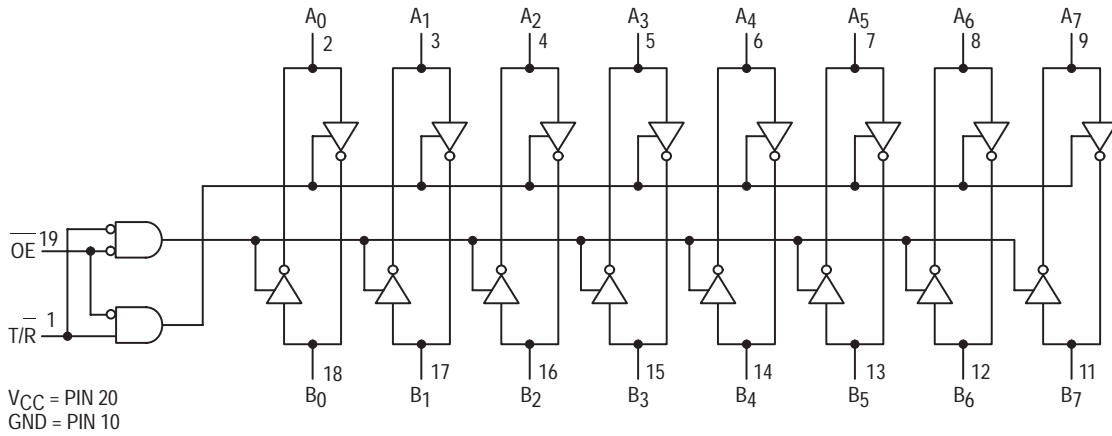
Symbol	Parameter		Limits			Unit	Test Conditions ¹		
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed as a HIGH Signal		
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed as a LOW Signal		
V _{IK}	Input Clamp Diode Voltage				-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	A _n	74	2.4	3.3		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
			74	2.7	3.3		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
		B _n	74	2.4	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
			74	2.7	3.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
			74	2.0			V	I _{OH} = -15 mA	V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	A _n	74		0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
V _{OL}	Output LOW Voltage	B _n	74			0.55	V	I _{OL} = 64 mA	V _{CC} = MIN
I _{OZH} + I _{IH}	Output Off Current HIGH				70	μA	V _{CC} = MAX, V _{OUT} = 2.7 V		
I _{OZL} + I _{IL}	Output Off Current LOW				-70	μA	V _{CC} = MAX, V _{OUT} = 0.5 V		
I _{IH}	Input HIGH Current	OE, T/R				40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		OE, T/R				100	μA	V _{CC} = 0 V, V _{IN} = 7.0 V	
		Others				1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
I _{IL}	Input LOW Current	OE, T/R				-40	μA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Output Short Circuit Current ²	A ₀ -A ₇		-60		-150	mA	V _{CC} = MAX, V _{OUT} = GND	
		B ₀ -B ₇		-100		-225			
I _{CC}	Power Supply Current	I _{CCH}				85	mA	V _{out} = HIGH	V _{CC} = MAX
		I _{CCL}				120		V _{out} = LOW	
		I _{CCZ}				100		OE = 4.5 V V _{out} = HIGH Z	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F640

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F			Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n , B_n to A_n	2.0 1.0		7.0 5.0	2.0 1.0		8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable Time to High or Low Level	3.5 6.0		11 11	3.5 6.0		13 12	ns
t_{PHZ} t_{PLZ}	Output Disable Time to High or Low Level	1.5 1.0		8.0 7.0	1.5 1.0		9.0 7.5	ns



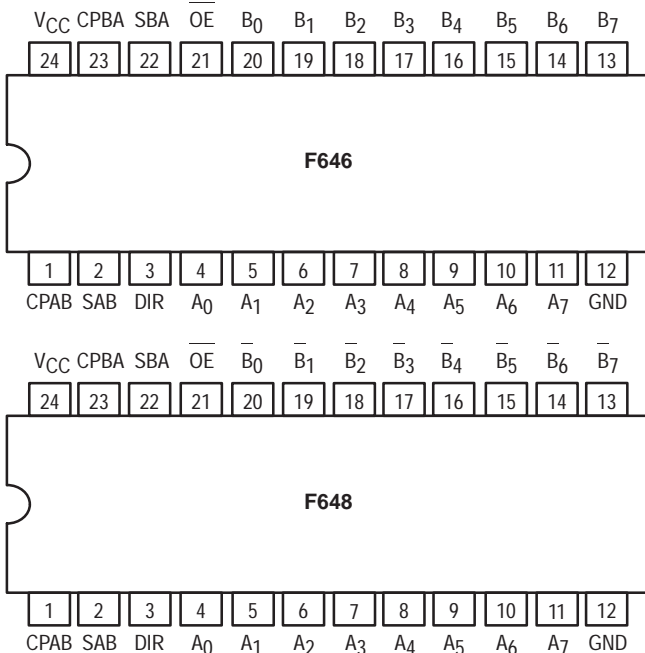
Product Preview

OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS

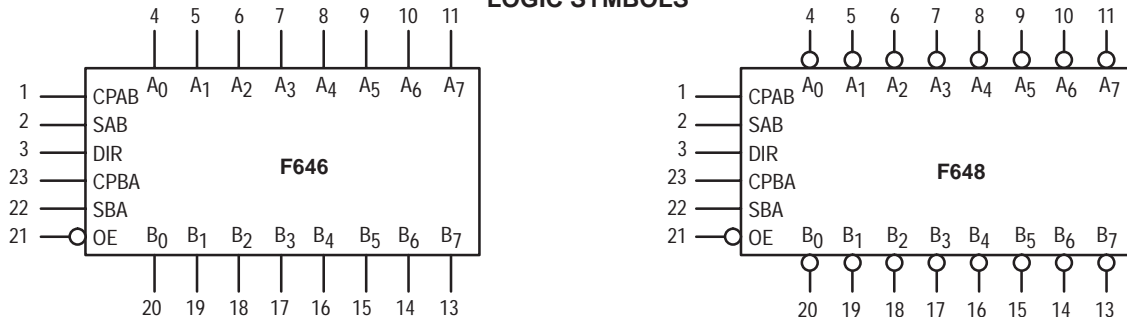
These devices consist of bus transceiver circuits with 3-state D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Output Enable (OE) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable OE is Active LOW. In the isolation mode (OE HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

- Independent Registers for A and B
- Multiplexed Real-Time and Stored Data
- Choice of True (F646) and Inverting (F648) Data Paths
- 3-State Outputs

PIN ASSIGNMENTS

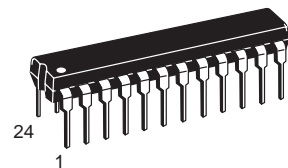


LOGIC SYMBOLS

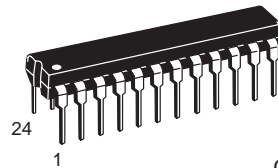


MC54/74F646
MC54/74F648

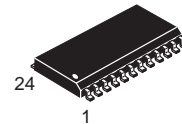
OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC54/74F646 • MC54/74F648

FUNCTION TABLE

Inputs						Data I/O*		Operation/Function
OE bar	DIR	CPAB	CPBA	SAB	SBA	A ₀ –A ₇	B ₀ –B ₇	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X	Input	Input	Store A _n Data in A Register
H	X	X	↑	X	X	Input	Input	Store B _n Data in B Register
H	X	↑	↑	X	X	Input	Input	Store A _n /B _n Data in A/B Register
L	H	X	X	L	X	Input	Output	A _n to B _n — Real Time (Transparent Mode)
L	H	↑	X	L	X	Input	Output	Store A _n Data in A Register
L	H	H or L	X	H	X	Input	Output	A Register to B _n (Stored Mode)
L	H	↑	X	H	X	Input	Output	Clock A _n Data to B _n and into A Register
L	L	X	X	X	L	Output	Input	B _n to A _n — Real Time (Transparent Mode)
L	L	X	↑	X	L	Output	Input	Store B _n Data in B Register
L	L	X	H or L	X	H	Output	Input	B Register to A _n (Stored Mode)
L	L	X	↑	X	H	Output	Input	Clock A _n Data to B _n and into B Register

*The data output function may be enabled or disabled by various signals at the OE bar and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the appropriate clock inputs.

H = HIGH voltage level

L = LOW voltage level

X = Don't Care

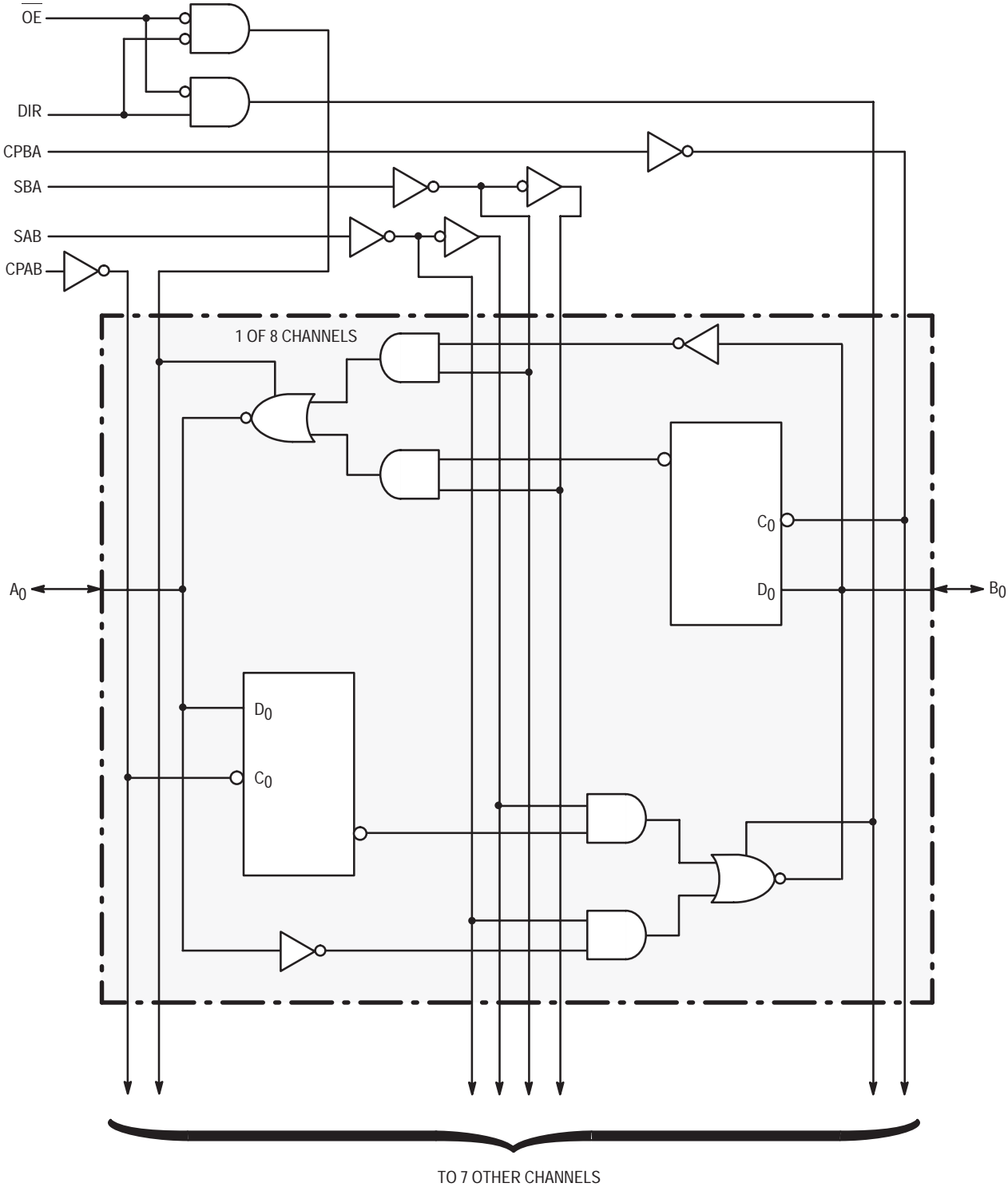
↑ = Low-to-High transition

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	DC Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74	— —	— —	-12 -15	mA
I _{OL}	Output Current — Low	54 74	— —	— —	48 64	mA

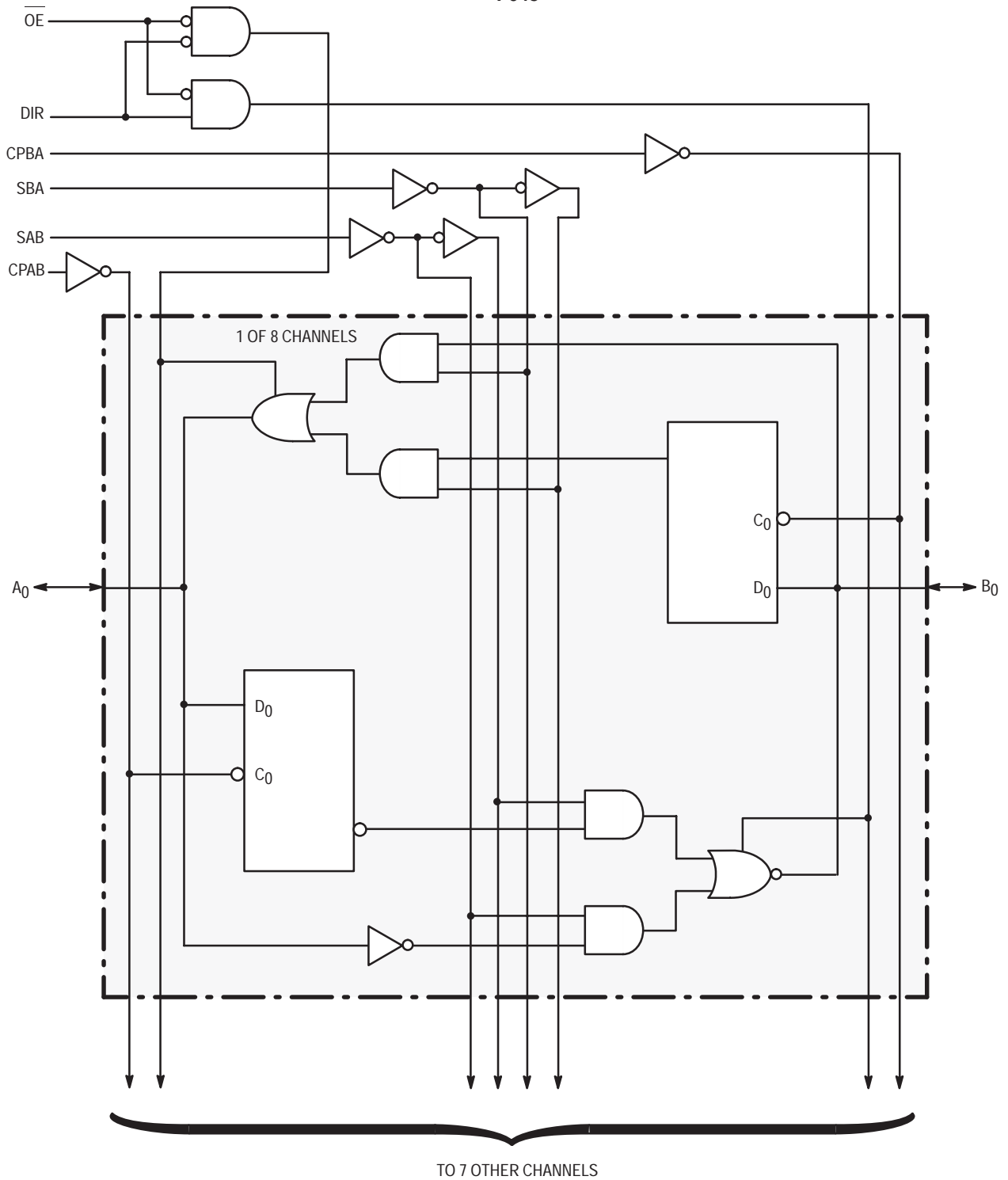
MC54/74F646 • MC54/74F648

LOGIC DIAGRAM
F646



MC54/74F646 • MC54/74F648

LOGIC DIAGRAM
F648



MC54/74F646 • MC54/74F648

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions (Note 1)		
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0	—	—	V	Guaranteed as a HIGH Signal		
V _{IL}	Input LOW Voltage		—	—	0.8	V	Guaranteed as a LOW Signal		
V _{IK}	Input Clamp Diode Voltage		—	—	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage	A _n , B _n	54/74	2.4	—	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
			74	2.7	—	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
			54	2.0	—	—	V	I _{OH} = -12.0 mA	V _{CC} = 4.5 V
			74	2.0	—	—	V	I _{OH} = -15.0 mA	V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	A _n , B _n	54	—	—	0.55	V	I _{OL} = 48 mA	V _{CC} = MIN
			74	—	—	0.55	V	I _{OL} = 64 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current		Non I/O Pins	—	—	20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
			Non I/O Pins	—	—	100	μA	V _{CC} = MAX, V _{IN} = 7.0 V	
			I/O (A _n , B _n)	—	—	1.0	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
I _{IL}	Input LOW Current		Non I/O Pins	—	—	-600	μA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{IH} + I _{OZH}	Output Leakage Current		I/O (A _n , B _n)	—	—	70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V
I _{IL} + I _{OZL}	Output Leakage Current		I/O (A _n , B _n)	—	—	-650	μA	V _{CC} = MAX, V _{OUT} = 0.5 V	
I _{OS}	Output Short Circuit Current (Note 2)			-100	—	-225	mA	V _{CC} = MAX, V _{OUT} = GND	
I _{CC}	Power Supply Current		I _{CC} H	—	—	135	mA	V _{out} = HIGH	V _{CC} = MAX
			I _{CC} L	—	—	150		V _{out} = LOW	
			I _{CC} Z	—	—	150		V _{out} = HIGH Z	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F646 • MC54/74F648

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100	—	75	—	90	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0 2.0	7.0 8.0	2.0 2.0	8.5 9.5	2.0 2.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (F646)	1.0 1.0	7.0 6.5	1.0 1.0	8.0 8.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus (F648)	1.0 1.0	7.0 6.5	1.0 1.0	10.0 9.0	1.0 1.0	7.5 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n	2.0 2.0	7.5 7.5	2.0 2.0	10.0 10.0	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable Time OE to A_n or B_n	2.0 2.0	7.0 7.0	2.0 2.0	9.5 9.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time OE to A_n or B_n	1.0 2.0	7.0 7.0	1.0 2.0	9.5 9.5	1.0 2.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A_n or B_n	2.0 2.0	7.0 7.0	2.0 2.0	9.5 9.5	2.0 2.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A_n or B_n	1.0 2.0	7.0 7.0	1.0 2.0	9.5 9.5	1.0 2.0	8.5 8.5	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		
		Min	Max	Min	Max	Min	Max	
$t_{s(H)}$ $t_{s(L)}$	Setup Time, HIGH or LOW Bus to Clock	4.0 4.0	— —	5.0 5.0	— —	5.0 5.0	— —	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW Bus to Clock	0.0 0.0	— —	0.0 0.0	— —	0.0 0.0	— —	ns
$t_{w(H)}$ $t_{w(L)}$	Clock Pulse Width HIGH or LOW	4.0 5.0	— —	4.0 5.0	— —	4.0 5.0	— —	ns



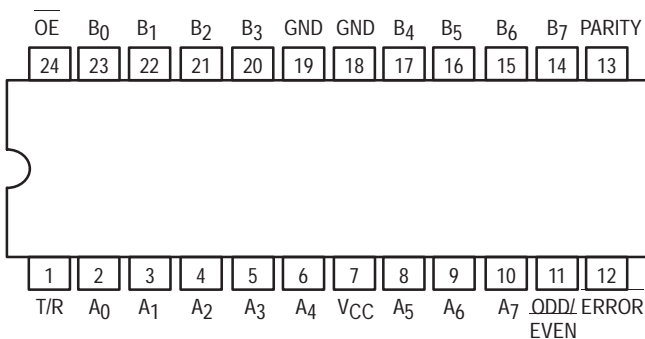
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY GENERATOR CHECKER (3-STATE OUTPUTS)

The MC74F657A and MC74F657B are Octal Bidirectional Transceivers with an 8-bit parity Generator/Checker and 3-state outputs.

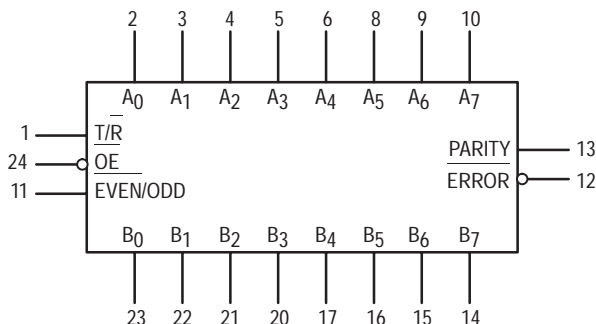
The A and B options are faster versions of the F657 and contain eight non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker. These devices are intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receiver (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

- High-Impedance NPN Base Input for Reduced Loading (20 μ A in HIGH and LOW States)
- Ideal in Applications Where High Output Drive and Light Bus Loading are Required (I_{OL} is 20 μ A versus Fast std of 600 μ A)
- Combines F245 and F280A Functions in One Package
- 3-State Outputs
- B Outputs, PARITY, ERROR, Sink 64 mA and Source 15 mA
- 15 mA Source Current
- Input Diodes for Termination Effects
- Glitchless Outputs During Power Up and Power Down
- High Impedance Outputs During Power Off
- ESD Protection > 4000 Volts

PIN ASSIGNMENT



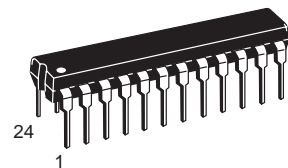
LOGIC SYMBOL



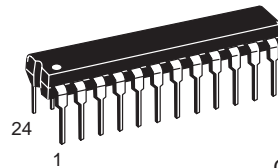
MC74F657A,B

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 8-BIT PARITY GENERATOR CHECKER (3-STATE OUTPUTS)

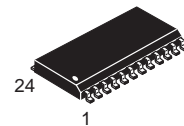
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03



DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC74FXXXAJ/BJ	Ceramic
MC74FXXXAN/BN	Plastic
MC74FXXXADW/BDW	SOIC

MC74F657A, B

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.5	V
T _A	Operating Ambient Temperature Range	74	0	70	°C
I _{OH}	Output Current — High	74		-3.0/-15	mA
I _{OL}	Output Current — Low	74		24/64	mA

FUNCTION TABLE

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/R	Even/Odd	Parity	Error	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	L	Receive

Number of Inputs That are High	Inputs			Input/Output	Outputs	
	OE	T/R	Even/Odd	Parity	Error	Outputs Mode
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't Care	H	X	X	Z	Z	Z

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care; Z = HIGH impedance state.

MC74F657A, B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	All Outputs	74	2.4		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
				2.7	3.4			V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	A0-A7	74		0.35	0.5	V	I _{OL} = 24 mA
		B0-B7 PARITY, ERROR	74		0.4	0.55	V	I _{OL} = 64 mA
I _{IH}	Input HIGH Current	T/R, OE, EVEN/ODD				100	μA	V _{CC} = 0 V, V _{IN} = 7.0 V
		A0-A7				2.0	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V
		B0-B7, PARITY				1.0		V _{CC} = 5.5 V, V _{IN} = 5.5 V
		EVEN/ODD				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		T/R, OE				40		
I _{IL}	Input LOW Current	EVEN/ODD				-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V
		T/R, OE				-40		
I _{IH} + I _{OZH}	Off-State Current HIGH Level Voltage Applied	A0-A7 B0-B7 PARITY				70	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{IL} + I _{OZL}	Off-State Current LOW Level Voltage Applied					-70		V _{CC} = MAX, V _{OUT} = 0.5 V
I _{OZH}	Off-State Output Current, High-Level Voltage Applied	ERROR				50	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied					-50		V _{CC} = MAX, V _{OUT} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	A _n Outputs		-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
		PARITY, B _n Outputs, ERROR		-100		-225		
I _{CC}	Total Supply Current	I _{CC} H		90	135	mA	V _{CC} = MAX	
		I _{CC} L		106	150			
		I _{CC} Z		98	145			

NOTES:

1. For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at one time, nor for more than 1 second.

MC74F657A, B

F657A

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	2.0		7.0	2.0	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _n to PARITY	6.0		13	5.5	14	ns
t _{PLH} t _{PHL}	Propagation Delay EVEN/ODD to PARITY, ERROR	4.5		10.5	4.5	11	ns
t _{PLH} t _{PHL}	Propagation Delay B _n to ERROR	7.0		18	6.5	19	ns
t _{PLH} t _{PHL}	Propagation Delay PARITY to ERROR	8.0		14	7.0	15	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	3.0		8.0	3.0	9.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH or LOW Level	2.0		7.5	2.0	8.0	ns

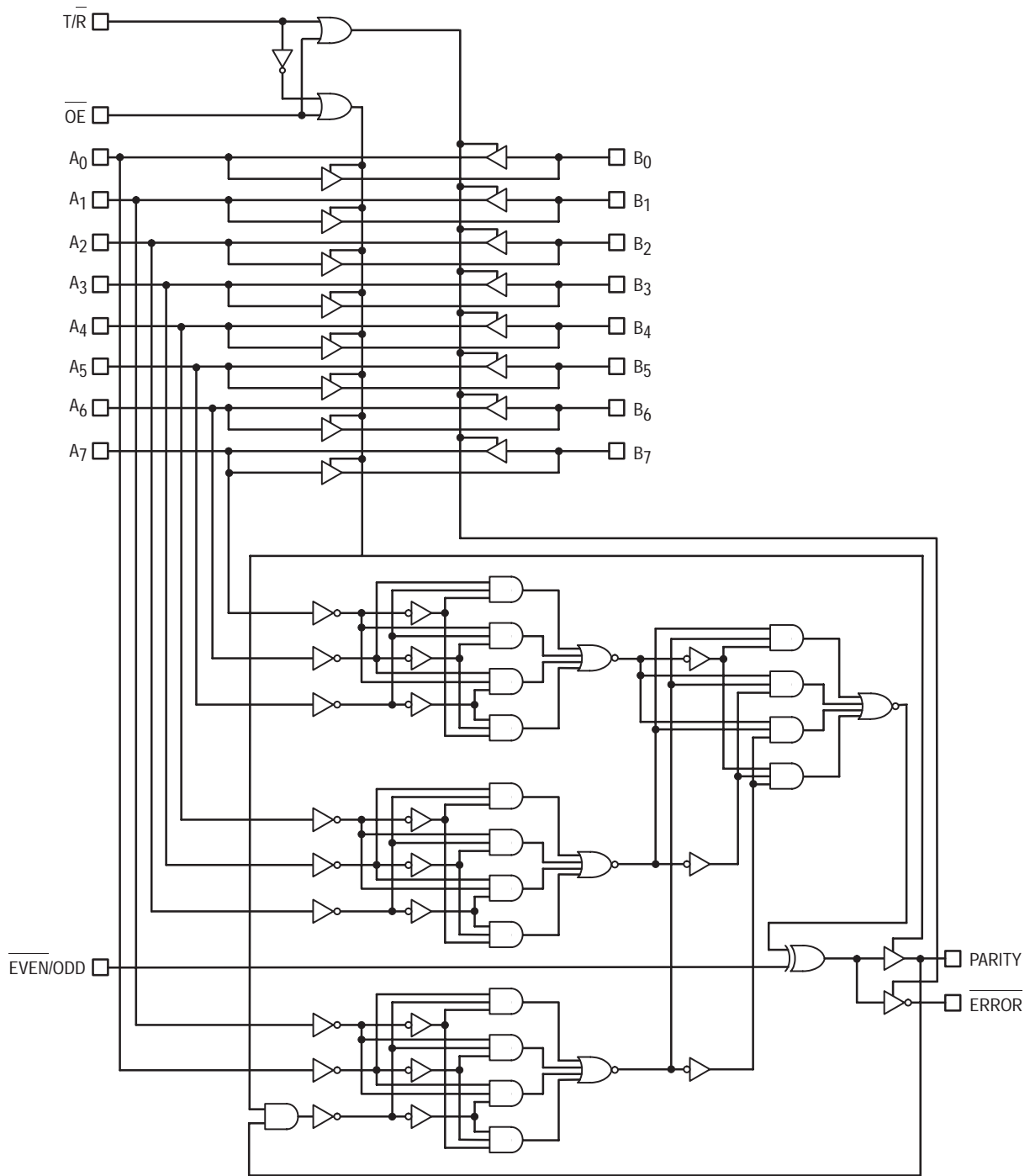
F657B

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay A _n to B _n or B _n to A _n	2.0		6.0	2.0	6.5	ns
t _{PLH} t _{PHL}	Propagation Delay A _n to PARITY	4.5		11.5	4.5	13	ns
t _{PLH} t _{PHL}	Propagation Delay EVEN/ODD to PARITY, ERROR	2.0		7.5	2.0	8.5	ns
t _{PLH} t _{PHL}	Propagation Delay B _n to ERROR	4.0		15	3.5	16	ns
t _{PLH} t _{PHL}	Propagation Delay PARITY to ERROR	5.0		11	4.0	12	ns
t _{PZH} t _{PZL}	Output Enable Time to HIGH or LOW Level	2.0		7.0	2.0	8.0	ns
t _{PHZ} t _{PLZ}	Output Disable Time from HIGH or LOW Level	2.0		6.0	2.0	6.5	ns

MC74F657A, B

LOGIC DIAGRAM



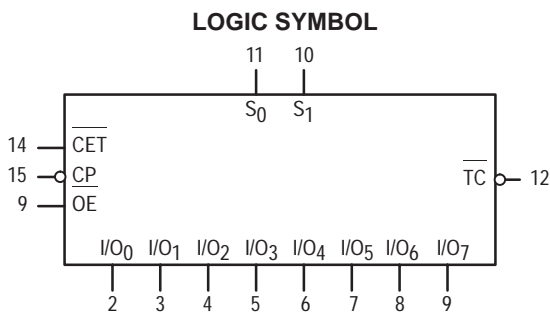
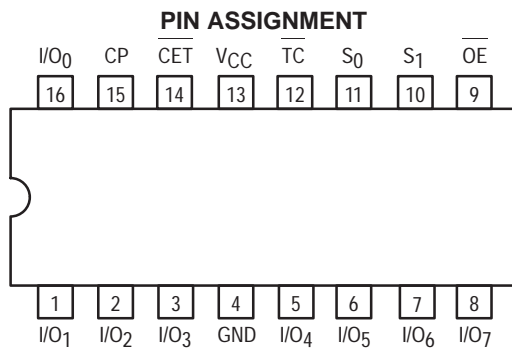


8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)

The MC74F779 is a fully synchronous 8-stage up/down counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0 , S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock.

When \overline{CET} is High the data outputs are held in their current state and \overline{TC} is held high. The \overline{TC} output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

- Multiplexed 3-State I/O Ports For Bus-oriented Applications
- Built-In Look-Ahead Carry Capability
- Count Frequency 145 MHz Typ
- Supply Current 90 mA Typ
- Fully Synchronous Operation
- Separate Pins for Master Reset and Synchronous Reset
- Center Power Pins to Reduce Effects of Package Inductance
- See F269 for 24-Pin Separate I/O Port Version
- See F579 for 20-Pin Version
- ESD Protection > 4000 Volts

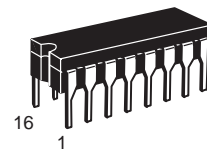


GUARANTEED OPERATING RANGES

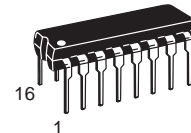
Symbol	Parameter	74	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	74	0	25	70	°C
I_{OH}	Output Current — High	$I/O_0-I/O_7$			-3.0	mA
		\overline{TC}			-1.0	
I_{OL}	Output Current — Low	$I/O_0-I/O_7$	74		24	mA
		\overline{TC}			20	

MC74F779

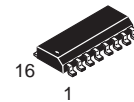
8-BIT BIDIRECTIONAL BINARY COUNTER (3-STATE)



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

MC74F779

FUNCTION TABLE

S1	S0	CET	OE	CP	Operating Mode
X	X	X	H	X	I/Oa to I/Oh in Hi-Z
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold (TC held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count Down

H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

(not LL) = S₁ and S₂ should never be Low voltage level at the same time in the hold mode only.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	74F			Unit	Test Conditions (Note 1)		
		Min	Typ (Note 2)	Max				
V _{OH}	Output HIGH Voltage	TC	2.5			V	I _{OH} = -1.0 mA V _{IL} = MAX V _{IH} = MIN	V _{CC} = 4.5 V
			2.7	3.4			V _{CC} = 4.75 V	
		I/O _n	2.4	3.3		V	I _{OH} = -3.0 mA V _{IL} = MAX V _{IH} = MIN	V _{CC} = 4.5 V
			2.7	3.3				V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	TC		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = 4.5 V
		I/O _n						I _{OL} = 24 mA
V _{IK}	Input Clamp Diode Voltage		-0.73	-1.2		V	V _{CC} = 4.5 V, I _{IN} = -18 mA	
I _{IH}	Input HIGH Current	I/O _n			1.0	mA	V _{CC} = 5.5 V	V _{IN} = 5.5 V
		others			100			μA
		I/O _n			70	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V	
		others			20			
I _{IL}	Input LOW Current	Except I/O _n			-0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V	
I _{OZH}	OFF-State Current High-Level Voltage Applied	I/O _n			70	μA	V _{CC} = 5.5 V	V _{OUT} = 2.7 V
I _{OZL}	OFF-State Current Low-Level Voltage Applied				-600			V _{OUT} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 3)		-60	-80	-150	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Total Supply Current (total)	I _{CC} H		82	116	mA	V _{CC} = MAX	
		I _{CC} L		91	128			
		I _{CC} Z		97	136			

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating conditions for the applicable device type.
2. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

MC74F779

AC ELECTRICAL CHARACTERISTICS

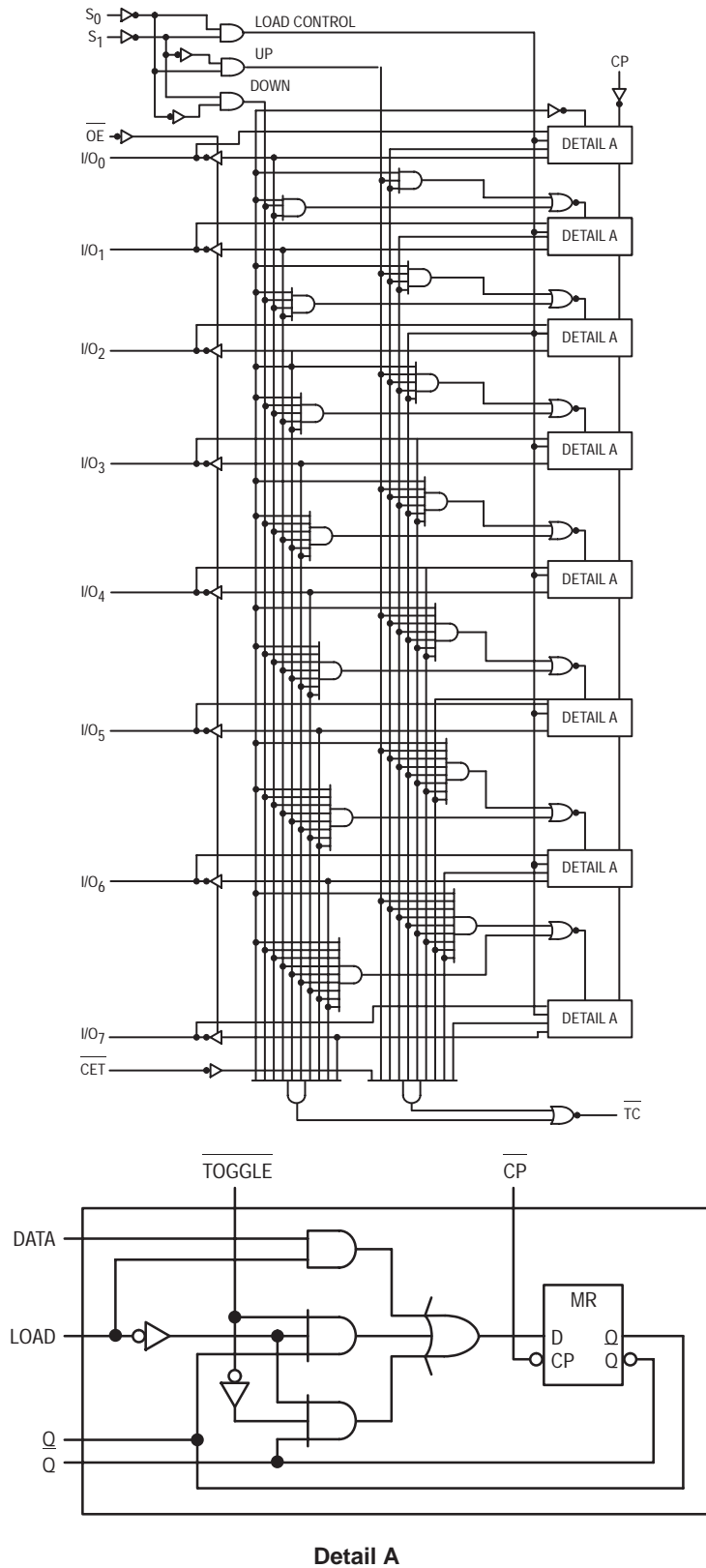
Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	125			80		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	4.5 5.5		10.5 10.5	4.5 5.5	11 11	ns
t _{PLH} t _{PHL}	Propagation Delay CP to TC	4.5 4.5		9.0 9.0	4.5 4.5	10 10	ns
t _{PLH} t _{PHL}	Propagation Delay CET to TC	3.0 3.0		6.5 7.5	2.5 2.5	7.5 8.0	ns
t _{PZH} t _{PZL}	Enable Time from High or Low Level	2.5 4.5		7.0 9.0	2.5 4.5	8.0 9.5	ns
t _{PHZ} t _{PLZ}	Disable Time from High or Low Level	1.0 1.0		6.5 7.0	1.0 1.0	8.0 8.0	ns

AC SETUP REQUIREMENTS

Symbol	Parameter	74F			74F			Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t _{s(H)} t _{s(L)}	Set-up time, HIGH or LOW I/O _n to CP	5.0 5.0			5.0 5.0			ns
t _{h(H)} t _{h(L)}	Hold time, HIGH or LOW I/O _n to CP	1.0 1.0			2.0 2.0			ns
t _{s(H)} t _{s(L)}	Set-up time, HIGH or LOW CET to CP	5.0 5.5			5.0 6.0			ns
t _{h(H)} t _{h(L)}	Hold time, HIGH or LOW CET to CP	0 0			0 0			ns
t _{s(H)} t _{s(L)}	Set-up time, HIGH or LOW S _n to CP	8.0 8.0			8.5 8.5			ns
t _{h(H)} t _{h(L)}	Hold time, HIGH or LOW S _n to CP	0 0			0 0			ns
t _{w(H)} t _{w(L)}	Clock Pulse Width	4.0 4.0			4.0 4.0			ns

MC74F779

LOGIC DIAGRAM

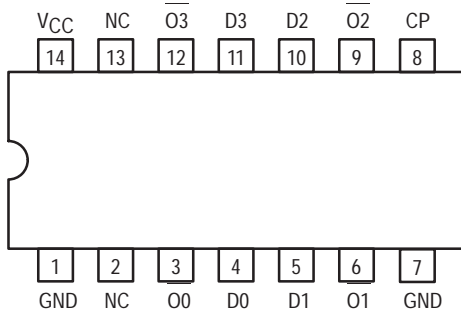


Clock Driver Quad D-Type Flip-Flop With Matched Propagation Delays

The MC74F803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs, and inverting outputs with closely matched propagation delays. With a buffered clock (CP) input that is common to all flip-flops, the F803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 1.0 to 1.5 nanoseconds.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching

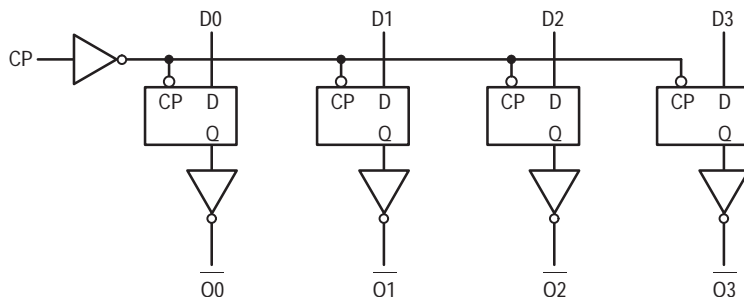
Pinout: 14-Lead Plastic (Top View)



GUARANTEED OPERATION RANGES

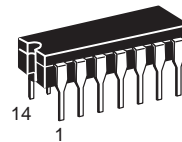
Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current — High	—	—	-20	mA
I _{OL}	Output Current — Low	—	—	24	mA

LOGIC DIAGRAM

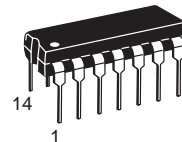


MC74F803

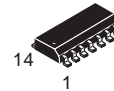
CLOCK DRIVER QUAD D-TYPE FLIP-FLOP WITH MATCHED PROPAGATION DELAYS



J SUFFIX
CERAMIC
CASE 632-08

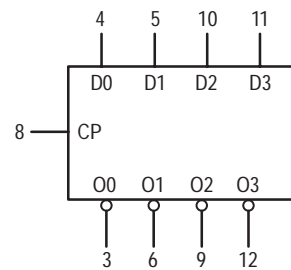


N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-03

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13



FUNCTIONAL DESCRIPTION

The F803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz, and the LOW-to-HIGH and HIGH-to-LOW propagation delays of the O₁ output vary by, at most, 1 nanosecond. Therefore, the device is ideal for use as a divide-

by-two driver for high-frequency clock signals that require symmetrical duty cycles. The difference between the LOW-to-HIGH and HIGH-to-LOW propagation delays for the O₀, O₂, and O₃ outputs vary by at most 1.5 nanoseconds. These outputs are very useful as clock drivers for circuits with less stringent requirements. In addition, the output-to-output skew is a maximum of 1.5 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least –20 milliamps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions*	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage	—	—	–1.2	V	I _{IN} = –18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	2.5	—	—	V	I _{OH} = –20 mA	V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage	—	0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
		—	—	20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
I _{IH}	Input HIGH Current	—	—	100		V _{IN} = 7.0 V	V _{CC} = MAX
I _{IL}	Input LOW Current	—	—	–0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)	–60	—	–150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current	—	—	70	mA	V _{CC} = MAX	

* Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the 74F803 can be tied together and the I_{OH} doubles.

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%, see Note 1)

Symbol	Parameter	C _L = 50 pF		C _L = 100 pF		Unit
		Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	70	—	50	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CP to On	3.0	7.5	3.0	10	ns
t _{PV}	Propagation Delay CP to On Variation (see Note 3)	—	3.0	—	4.0	ns
t _{ps} O ₁	Propagation Delay Skew t _{PLH} Actual – t _{PHL} Actual for O ₁ Only	—	1.0	—	2.0	ns
t _{ps} O ₀ , O ₂ , O ₃	Propagation Delay Skew t _{PLH} Actual – t _{PHL} Actual for O ₀ , O ₂ , O ₃	—	1.5	—	2.0	ns
t _{os}	Output to Output Skew (see Note 2) t _p On – t _p Om	—	1.5	—	2.5	ns
t _{rise} , t _{fall} O ₁	Rise/Fall Time for O ₁ (0.8 to 2.0 V)	—	3.0	—	4.0	ns
t _{rise} , t _{fall} O ₀ , O ₂ , O ₃	Rise/Fall Time for O ₀ , O ₂ , O ₃ (0.8 to 2.0 V)	—	3.5	—	4.5	ns

1. The test conditions used are all four outputs switching simultaneously. The AC characteristics described above (except for O₁) are also guaranteed when two outputs are tied together.
2. Where t_p On and t_p Om are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
3. For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

AC OPERATING REQUIREMENTS ($T_A = 0$ to 70°C , $V_{CC} = 5.0\text{ V} \pm 10\%$)

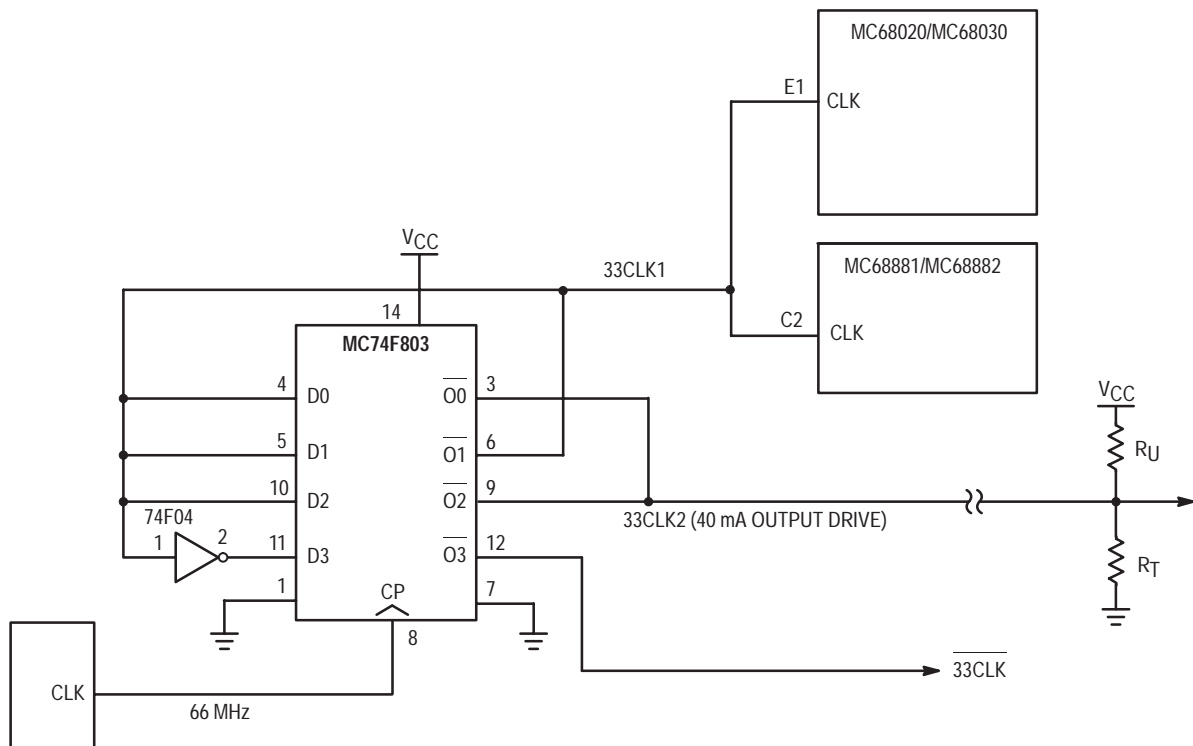
Symbol	Parameter	$C_L = 50\text{ pF}$		$C_L = 100\text{ pF}$		Unit
		Min	Max	Min	Max	
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW D_n to CP	3.0	—	4.0	—	ns
t_f	$t_p + t_s$ (see Note)	—	9.0	—	12	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW D_n to CP	2.0	—	2.0	—	ns
$t_{w(H)}$ $t_{w(L)}$	CP Pulse Width HIGH or LOW	7.0	—	8.0	—	ns

The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

APPLICATION NOTE

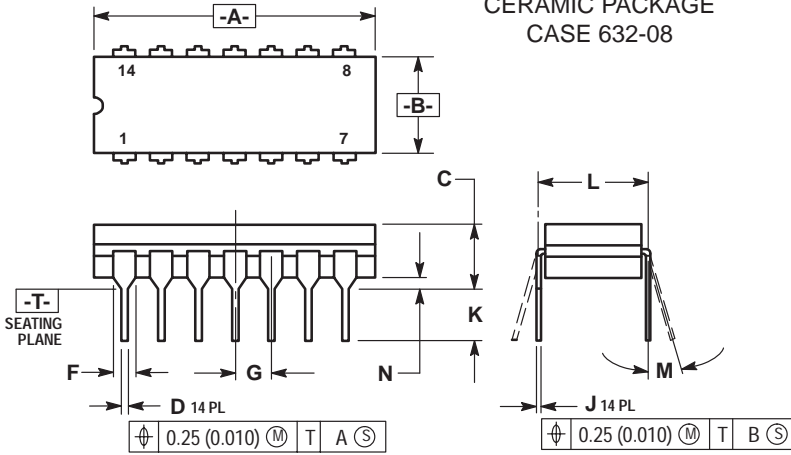
The closely matched outputs of the MC74F803 provide an ideal interface for the clock input of Motorola's high-frequency microprocessors.

74F803 INTERFACE AS CLOCK TO MC68020 SYSTEM



OUTLINE DIMENSIONS

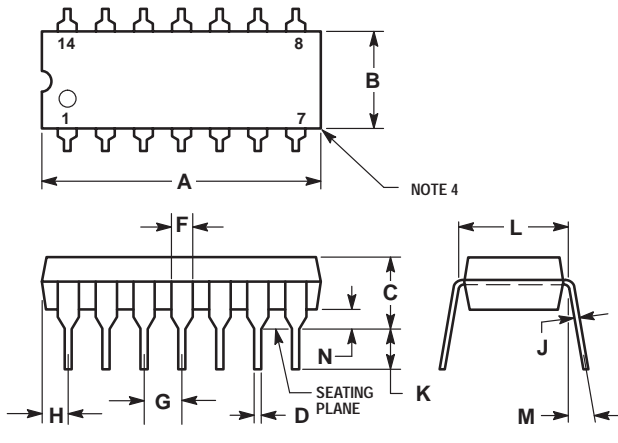
J SUFFIX
CERAMIC PACKAGE
CASE 632-08



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC ϕ		0.300 BSC ϕ	
M	0	15	0	15
N	0.51	1.01	0.020	0.040

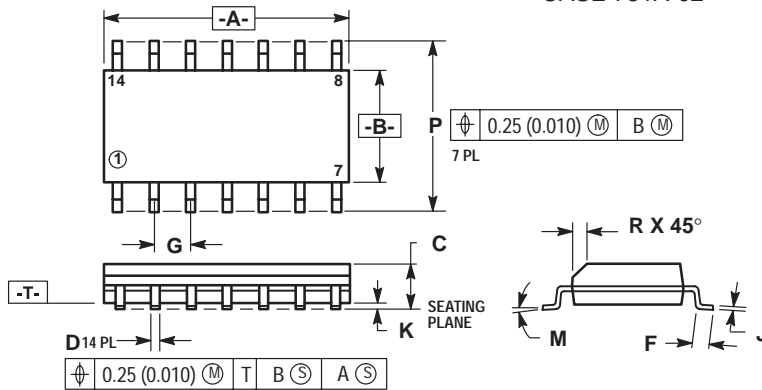
N SUFFIX
PLASTIC PACKAGE
CASE 646-06



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 4. ROUNDED CORNERS OPTIONAL.
 5. 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC ϕ		0.300 BSC ϕ	
M	0.39	1.01	0.015	0.039
N	0.39	1.01	0.015	0.039


D SUFFIX
SOIC PACKAGE
CASE 751A-02



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0	7	0	7
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



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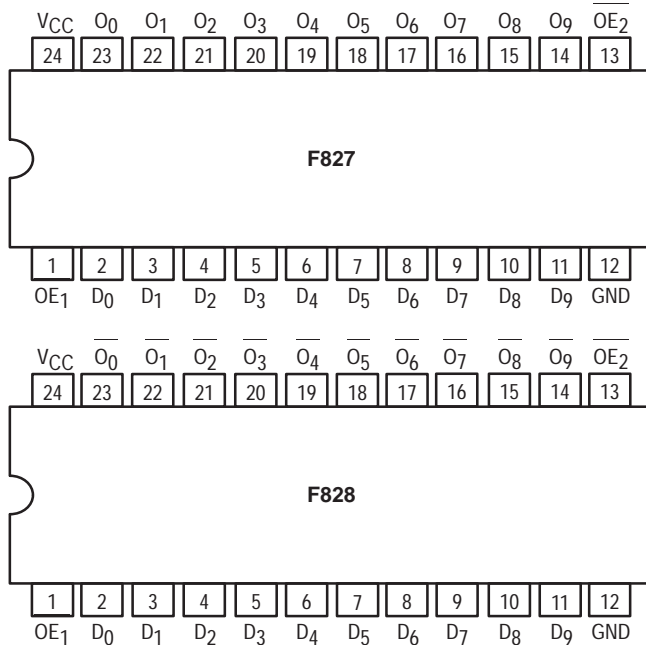
10-BIT BUFFERS/LINE DRIVERS (WITH 3-STATE OUTPUTS)

The MC54/74F827 and MC54/74F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

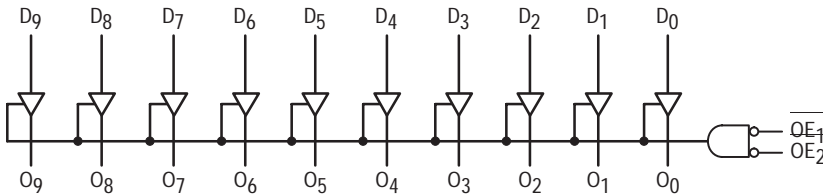
The F827 and F828 are functionally and pin compatible to AMD's 29827 and 29828. The F828 is an inverting version of the F827.

- 3-State Outputs Drive Memory Address, Bus and Clock Lines
- Outputs Sink 64 mA
- 15 mA Source Current
- Flow Through Pinout Architecture for Microprocessor Oriented Applications

CONNECTION DIAGRAMS (TOP VIEW)



LOGIC DIAGRAM

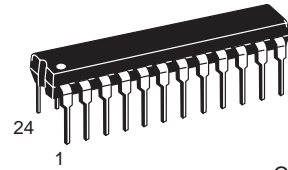


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

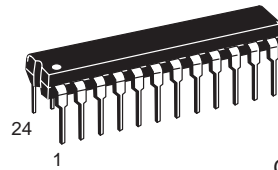
MC54/74F827 MC54/74F828

10-BIT BUFFERS/LINE DRIVERS (WITH 3-STATE OUTPUTS)

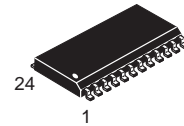
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 758-01



N SUFFIX
PLASTIC
CASE 724-03

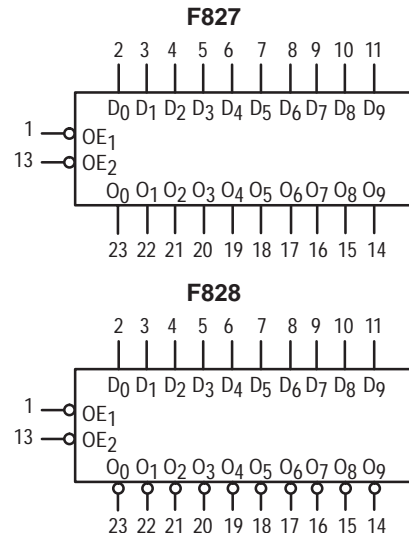


DW SUFFIX
SOIC
CASE 751E-03

ORDERING INFORMATION

MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

LOGIC SYMBOL



MC54/74F827 • MC54/74F828

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage*	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54	—	—	-12	mA
		74	—	—	-15	
I _{OL}	Output Current — Low	54	—	—	48	mA
		74	—	—	64	

FUNCTION TABLE

Inputs		Outputs		Function
$\overline{\text{OE}}$	D _n	O _n		
		F827	F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

MC54/74F827 • MC54/74F828

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage	—	—	-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN	
V _{OH}	Output HIGH Voltage	54	2.0	—	—	V	I _{OH} = -12 mA	V _{CC} = MIN
		74	2.0	—	—	V	I _{OH} = -15 mA	
		54, 74	2.4	—	—	V	I _{OH} = -3.0 mA	
		74	2.7	—	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage	54	—	—	0.55	V	I _{OL} = 48 mA	V _{CC} = MIN
		74	—	—	0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH	—	—	50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX	
I _{OZL}	Output Off Current LOW	—	—	-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX	
I _{IH}	Input HIGH Current	—	—	20	μA	V _{IN} = 2.7 V	V _{CC} = 0 V	
		—	—	100	μA	V _{IN} = 7.0 V		
I _{IL}	Input LOW Current	—	—	-20	μA	V _{IN} = 0.5 V	V _{CC} = MAX	
I _{OS}	Output Short Circuit Current (Note 2)	-100	—	-225	mA	V _{OUT} = 0 V	V _{CC} = MAX	
I _{CCH}	Power Supply Current HIGH	F827	—	—	70	mA	Outputs HIGH	V _{CC} = MAX
		F828	—	—	45	mA		
I _{CCL}	Power Supply Current LOW	F827	—	—	100	mA	Outputs LOW	V _{CC} = MAX
		F828	—	—	85	mA		
I _{CCZ}	Power Supply Current OFF	F827	—	—	90	mA	Outputs OFF	V _{CC} = MAX
		F828	—	—	70	mA		

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

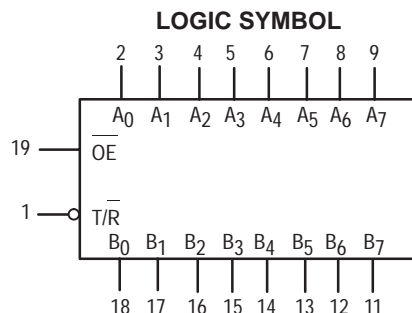
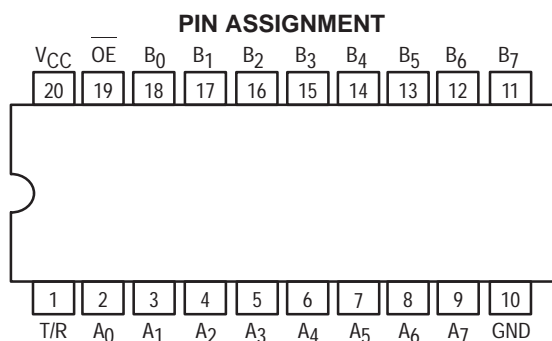
Symbol	Parameter	54/74F		54F		74F		Unit	
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to 70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF			
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Output	F827	2.0	8.5	2.0	10	2.0	9.0	ns
			2.0	8.5	2.0	10	2.0	9.0	
t _{PZH} t _{PZL}	Output Enable Time		3.5	9.5	3.5	11	3.5	10	ns
			4.0	9.0	4.0	10.5	4.0	9.5	
t _{PHZ} t _{PLZ}	Output Disable Time		2.0	8.0	2.0	9.5	2.0	8.5	ns
			1.5	8.0	1.5	9.5	1.5	8.5	
t _{PLH} t _{PHL}	Propagation Delay, Data to Output	F828	2.0	9.0	2.0	11	2.0	10	ns
			1.0	8.0	1.0	10	1.0	9.0	
t _{PZH} t _{PZL}	Output Enable Time		3.5	9.5	3.5	11	3.5	10	ns
			4.0	9.0	4.0	10.5	4.0	9.5	
t _{PHZ} t _{PLZ}	Output Disable Time		2.0	8.5	2.0	10	2.0	9.0	ns
			1.5	7.0	1.5	9.0	1.5	8.0	



OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

The MC74F1245 contains eight noninverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at the A ports and 64 mA at the B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-Z condition.

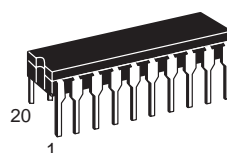
- Noninverting Buffers
- Bidirectional Data Path
- B Outputs Sink 64 mA
- High Impedance Inputs for Reduced Loading
- Same Function and Pinout as the F245
- ESD Protection > 4000 Volts



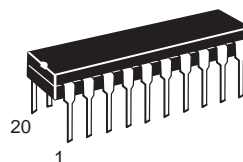
MC74F1245

OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

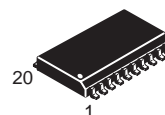
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

MC74FXXXXJ Ceramic
MC74FXXXXN Plastic
MC74FXXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit	
V _{CC}	DC Supply Voltage	74	4.5	5.0	5.5	V	
T _A	Operating Ambient Temperature Range	74	0	25	70	°C	
I _{OH}	Output Current — High	A _n Outputs	74	—	—	—3.0	mA
I _{OL}	Output Current — Low	A _n Outputs	74	—	—	24	mA
I _{OH}	Output Current — High	B _n Outputs	74	—	—	—15	mA
I _{OL}	Output Current — Low	B _n Outputs	74	—	—	64	mA

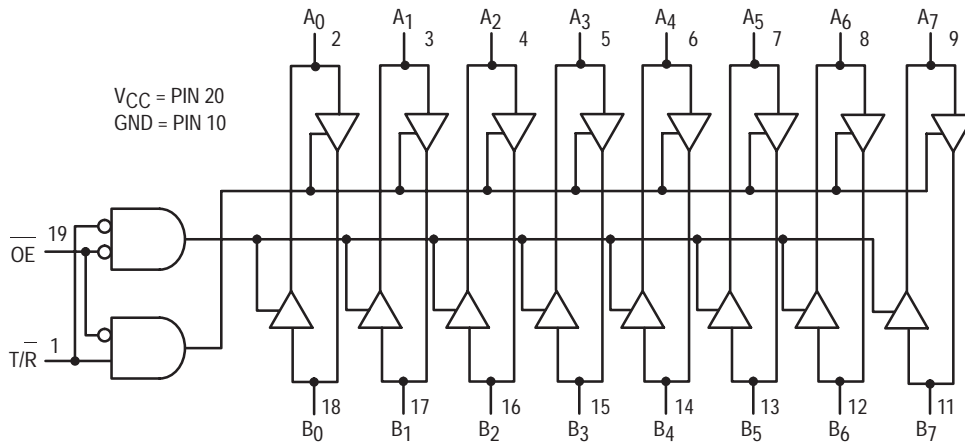
MC74F1245

FUNCTION TABLE

Inputs		Inputs/Outputs	
OE	T/R	A _n	B _n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = HIGH impedance "off" state.

LOGIC DIAGRAM



MC74F1245

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions (Note 1)		
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0	—	—	V	Guaranteed Input HIGH Voltage		
V _{IL}	Input LOW Voltage	—	—	0.8	V	Guaranteed Input LOW Voltage		
V _{IK}	Input Clamp Diode Voltage	—	-0.73	-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA		
V _{OH}	Output HIGH Voltage A _n Outputs	74	2.4	3.3	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3	—	V		V _{CC} = 4.75 V
V _{OH}	Output HIGH Voltage B _n Outputs	74	2.4	3.4	—	V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	—	V		V _{CC} = 4.75 V
		74	2.0	—	—	V	I _{OH} = -15 mA	V _{CC} = 4.5 V
V _{OL}	Output LOW Voltage A _n Outputs	74	—	0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
V _{OL}	Output LOW Voltage B _n Outputs	74	—	—	0.55	V	I _{OL} = 64 mA	
I _{OZH}	Output Off Current HIGH	—	—	70	μA	V _{CC} = MAX	V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW	—	—	-70	μA	V _{CC} = MAX, V _{OUT} = 0.5 V		
I _{IH}	Input HIGH Current	OE, T/R Inputs	—	—	40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		A _n , B _n Inputs	—	—	70	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		OE, T/R Inputs	—	—	100	μA	V _{CC} = 0 V, V _{IN} = 7.0 V	
		B _n Inputs	—	—	1.0	mA	V _{CC} = 0 V, V _{IN} = 5.5 V	
I _{IHH}	Input HIGH Current	A _n Inputs	—	—	2.0	mA	V _{CC} = 0 V, V _{IN} = 5.5 V	
I _{IL}	Input LOW Current	OE, T/R Inputs	—	—	-40	μA	V _{CC} = MAX, V _{IN} = 0.5 V	
		A _n , B _n Inputs	—	—	-70	μA		
I _{OS}	Output Short Circuit Current (Note 2)	A _n Outputs	-60	—	-150	mA	V _{CC} = MAX, V _{OUT} = GND	
		B _n Outputs	-100	—	-225	mA		
I _{CC}	Power Supply Current	I _{CC} H	—	—	120	mA	V _{CC} = MAX	
		I _{CC} L	—	—	120			
		I _{CC} Z	—	—	130			

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0 V ±10% C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay	2.0	6.5	1.5	7.0	ns
t _{PHL}	Transparent Mode A _n to B _n or B _n to A _n	2.5	7.5	2.0	8.0	
t _{PZH}	Output Enable Time	3.0	8.0	2.5	9.0	ns
t _{PZL}		4.0	10.0	3.5	11.0	
t _{PHZ}	Output Disable Time	2.0	8.0	1.5	9.0	ns
t _{PLZ}		1.0	10.0	1.0	11.0	

Advance Information

Clock Driver

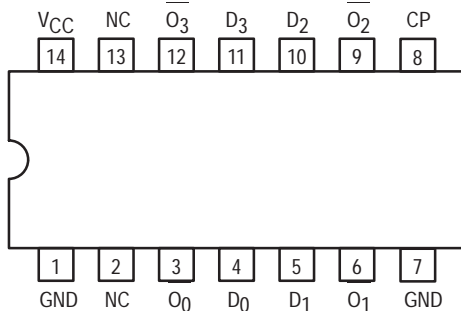
Quad D-Type Flip-Flop

With Matched Propagation Delays

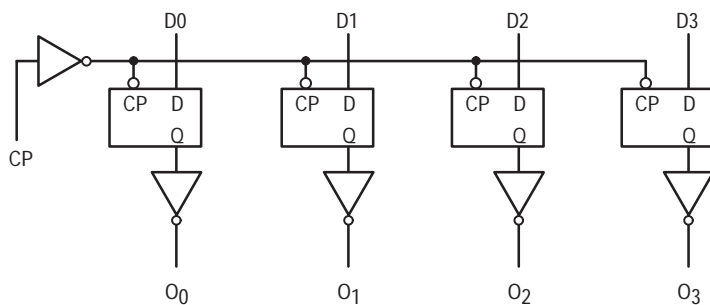
The MC74F1803 is a high-speed, low-power, quad D-type flip-flop featuring separate D-type inputs and inverting outputs with closely matched propagation delays. With a buffered positive edge-triggered clock (CP) input that is common to all flip-flops, the MC74F1803 is useful in high-frequency systems as a clock driver, providing multiple outputs that are synchronous. Because of the matched propagation delays, the duty cycles of the output waveforms in a clock driver application are symmetrical within 2.0 nanoseconds.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Clock Driver Applications
- Outputs Guaranteed for Simultaneous Switching

Pinout: 14-Lead Plastic (Top View)



LOGIC DIAGRAM

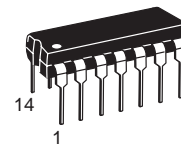


V_{CC} = Pin 14; GND = Pins 1,7; NC = Pins 2, 13

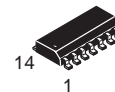
NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays

MC74F1803

CLOCK DRIVER QUAD D-TYPE FLIP-FLOP WITH MATCHED PROPAGATION DELAYS

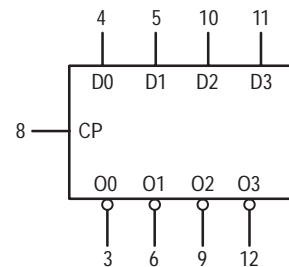


N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-03

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PINS 1 AND 7
NC = PINS 2 AND 13

This document contains information on a new product. Specifications and information herein are subject to change without notice.



FUNCTIONAL DESCRIPTION

The MC74F1803 consists of four positive edge-triggered flip-flops with individual D-type inputs and inverting outputs. The buffered clock is common to all flip-flops and the following specifications allow for outputs switching simultaneously. The four flip-flops store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. The maximum frequency of the clock input is 70 megahertz and the LOW-to-HIGH and HIGH-to-LOW

propagation delays of the $\overline{\text{On}}$ output vary by at most, 2.0 nanoseconds. Therefore, the device is ideal for use as a divide-by-two driver for high-frequency clock signals that require symmetrical duty cycles. In addition, the output-to-output skew is a maximum of 2.0 nanoseconds. Finally, the I_{OH} specification at 2.5 volts is guaranteed to be at least -20 milli-amps. If their inputs are identical, multiple outputs can be tied together and the I_{OH} is commensurately increased.

GUARANTEED OPERATION RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High	—	—	-20	mA
I_{OL}	Output Current — Low	—	—	24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions 1,2
			Min	Typ	Max		
V_{IH}	Input HIGH Voltage		2.0	—	—	V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage		—	—	0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage		—	—	-1.2	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage A_n Outputs	74	2.5	—	—	V	$I_{OH} = -20$ mA, $V_{CC} = 4.5$ V
V_{OL}	Output LOW Voltage A_n Outputs	74	—	0.35	0.5	V	$I_{OL} = 24$ mA, $V_{CC} = \text{MIN}$
I_{IH}	Input HIGH Current		—	—	20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7$ V
			—	—	100	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0$ V
I_{IL}	Input LOW Current		—	—	-0.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.5$ V
I_{OS}	Output Short Circuit Current ³		-60	—	-150	mA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0$ V
I_{CC}	Power Supply Current		—	—	70	mA	$V_{CC} = \text{MAX}$

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

² Normal test conditions for this device are all four outputs switching simultaneously. Two outputs of the MC74F1803 can be tied together and the I_{OH} doubles.

³ Not more than one output should be shorted at a time, nor for more than 1 second.

AC OPERATING REQUIREMENTS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = +5.0$ V $\pm 10\%$; $R_L = 500$ Ω)

Symbol	Parameter	$C_L = 50$ pF		Unit
		Min	Max	
$t_{S(H)}$ $t_{S(L)}$	Setup Time, HIGH or LOW: D_n to CP	3.0 3.0	— —	ns
t_f	$t_p + t_s$ ¹	—	9.0	ns
$t_{h(H)}$ $t_{h(L)}$	Hold Time, HIGH or LOW: D_n to CP	2.0 2.0	— —	ns
$t_{W(H)}$ $t_{W(L)}$	Cp Pulse Width HIGH or LOW	7.0 6.0	— —	ns

MC74F1803

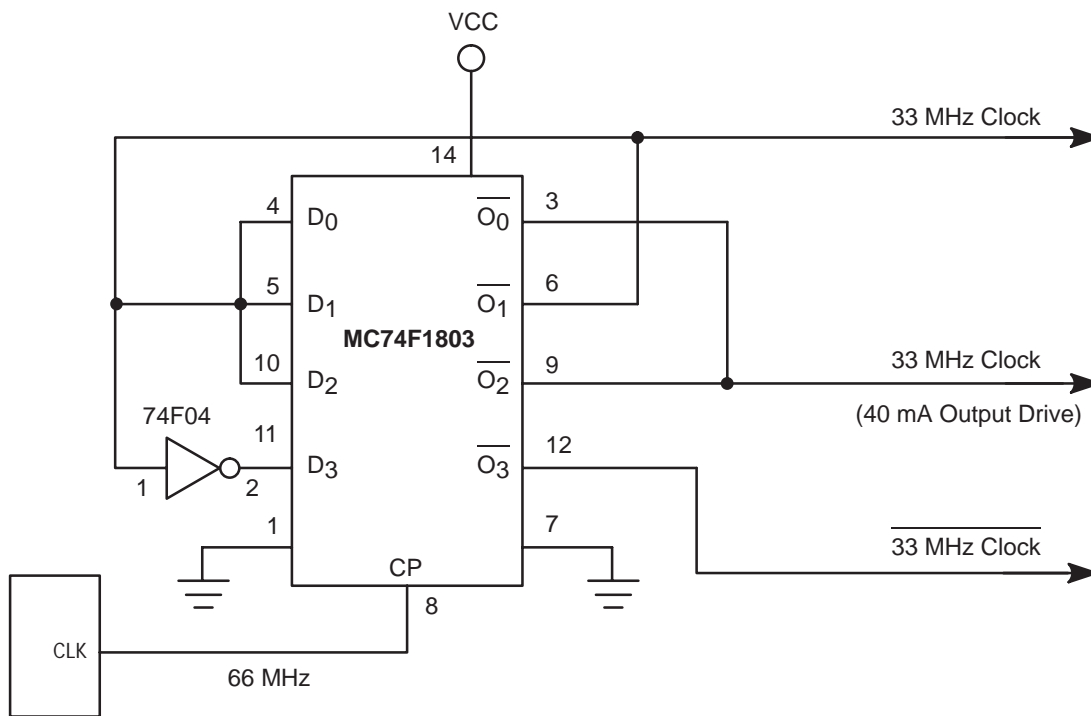
¹ The combination of the setup time (t_s) requirement and maximum propagation delay (t_p) are guaranteed to be within this limit for all conditions.

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C: V_{CC} = +5.0 V ±10%: R_L = 500 Ω)¹

Symbol	Parameter	C _L = 50 pF		Unit
		Min	Max	
f _{max}	Maximum Clock Frequency	70	–	MHz
t _{pLH} t _{pHL}	Propagation Delay CP to O _n	3.0	7.5	ns
t _{pV}	Propagation Delay CP to O _n Variation	–	3.0	ns
t _{ps} O ₀ , O ₁ , O ₂ , O ₃ ,	Propagation Delay Skew t _{pLH} Actual – t _{pHL} Actual for O ₀ , O ₁ , O ₂ , O ₃	–	2.0	ns
t _{os}	Output to Output Skew ² t _p O _n – t _p O _m	–	2.0	ns
t _{rise} , t _{fall} O ₁ ,	Rise/Fall Time for O ₁ (0.8 to 2.0 V)	–	3.0	ns
t _{rise} , t _{fall} O ₀ , O ₂ , O ₃ ,	Rise/Fall Time for O ₁ , O ₂ , O ₃ , (0.8 to 2.0 V)	–	3.5	ns

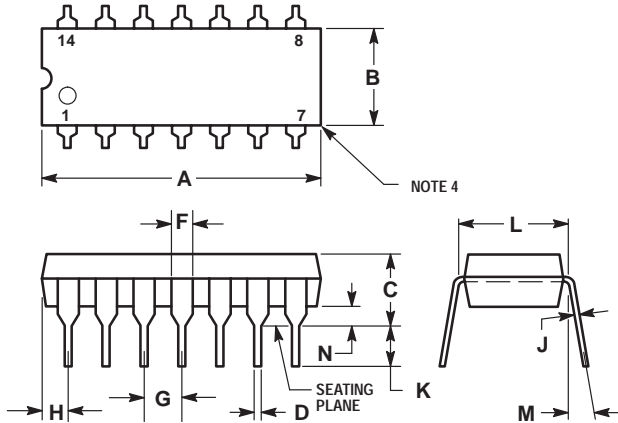
- ¹ The test conditions used are all four outputs switching simultaneously. The AC characteristics described above are also guaranteed when two outputs are tied together.
- ² Where t_p O_n and t_p O_m are the actual propagation delays (any combination of high or low) for two separate outputs from a given high transition of CP.
- ³ For a given set of conditions (i.e., capacitive load, temperature, V_{CC}, and number of outputs switching simultaneously) the variation from device to device is guaranteed to be less than or equal to the maximum.

TYPICAL MC74F1803 APPLICATION



OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 646-06

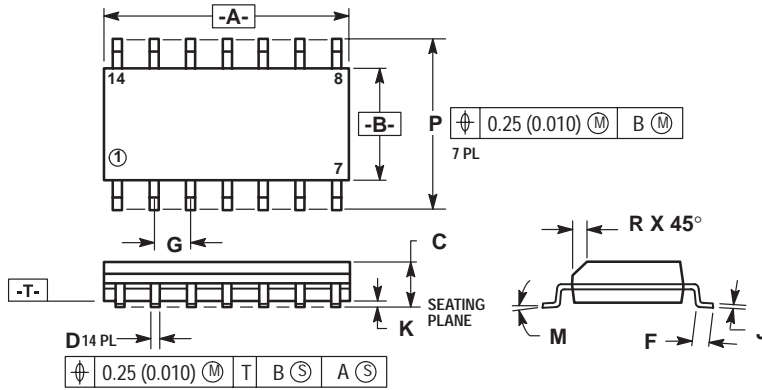


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	0.62 BSC		0.300 BSC	
M	0.39	1.01	0.015	0.039
N				

D SUFFIX
SOIC PACKAGE
CASE 751A-02



NOTES:

- DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0	7	0	7
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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QUAD FUTUREBUS BACKPLANE TRANSCEIVER (3 STATE + OPEN COLLECTOR)

The MC74F3893A is a quad backplane transceiver and is intended to be used in very high speed bus systems.

The MC74F3893A interfaces to "Backplane Transceiver Logic" (BTL). BTL features a reduced (1 V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5 pF).

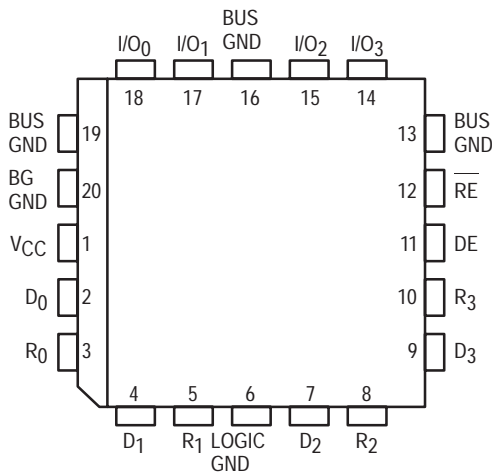
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, reduced EMI and crosstalk, low capacitive loading, superior noise margin and short propagation delays. This results in a high bandwidth, reliable backplane.

The MC74F3893A has four TTL outputs (R_n) on the receiver side with a common Receive Enable input (RE). It has four data inputs (D_n) which are also TTL. These data inputs are NANDed with the Data Enable input (DE). The four I/O pins (Bus side) are futurebus compatible, sink a minimum of 100 mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch-free during power up and power down.

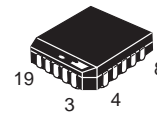
- Quad Backplane Transceiver
- Drives Heavily Loaded Backplanes with Equivalent Load Impedances Down to 10 ohms
- Futurebus Drivers Sink 100 mA
- Reduced Voltage Swing (1 Volt) Produces Less Noise and Reduces Power Consumption
- High Speed Operation Enhances Performance of Backplane Buses and Facilitates Incident Wave Switching
- Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards
- Built-In Precision Band-Gap (BG) Reference Provides Accurate Receiver Threshold and Improved Noise Immunity
- Glitch-Free Power Up/Power Down Operation On All Outputs
- Pin and Function Compatible with NSC DS3893A and Signetics 74F3893
- Separate Bus Ground Returns for Each Driver to Minimize Ground Noise
- MOS and TTL Compatible High Impedance Inputs

PINOUT: 20-LEAD PLCC (TOP VIEW)



MC74F3893A

**QUAD FUTUREBUS
BACKPLANE TRANSCEIVER
(3 STATE + OPEN COLLECTOR)**
FAST™ SCHOTTKY TTL

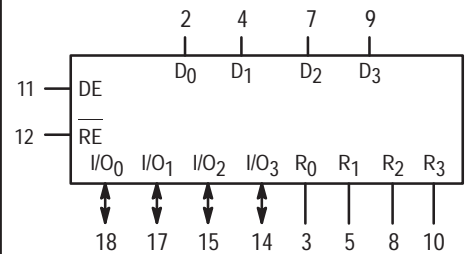


**FN SUFFIX
PLASTIC
CASE 775-02**

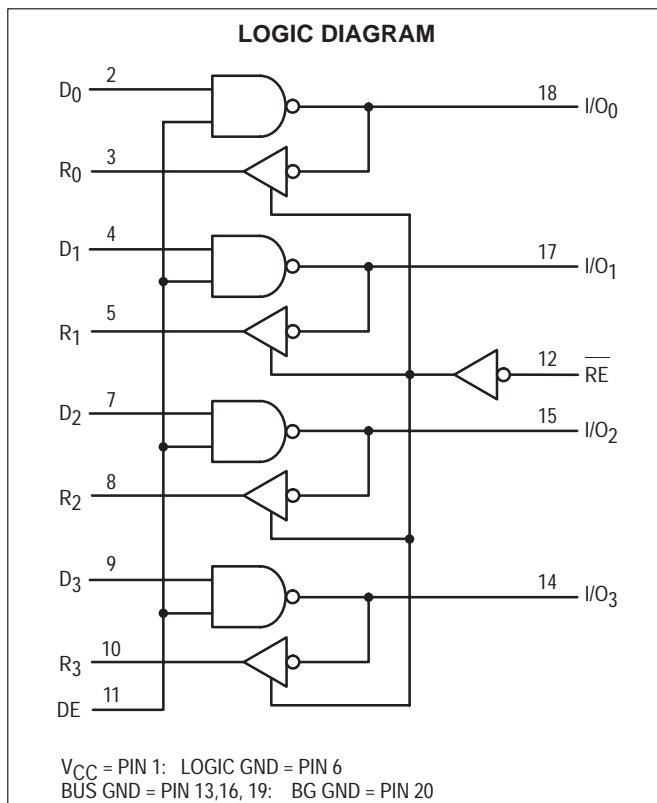
ORDERING INFORMATION

MC74FXXXXAFN Plastic

LOGIC SYMBOL



MC74F3893A



FUNCTION TABLE

Inputs			Input/Output	Outputs	Operating Mode
DE	RE	D_n	I/O_n	R_n	
H	L	L	H	L	Transmit to Bus
H	L	H	L	H	
H	H	L	$\overline{D_n}$	Z	Receiver 3-State, Transmit to Bus
L	H	H	H	Z	
L	L	X	H	L	Receive, I/O_n = Inputs
L	L	X	L	H	

H = HIGH voltage level:
 L = LOW voltage level:
 X = Don't care:
 Z = HIGH impedance "Off" state.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit	
		Min	Typ	Max		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	High-Level Input Voltage	2.0	—	—	V	
V_{IL}	Low-Level Input Voltage					
I_{IK}	Input Clamp Current	—	—	-18	mA	
V_{TH}	Bus Input Threshold	I/O_n Only	1.475	1.550	1.625	V
I_{OH}	Output Current — High	R_n Only	—	—	-3.0	mA
I_{OL}	Output Current — Low		—	—	100	mA
T_A	Operating Ambient Temperature Range	0	—	70	°C	

MC74F3893A

DC CHARACTERISTICS (Over Recommended Operating Free-Air Temperature Range Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions (Note 1)
			Min	Typ (2)	Max		
V _{OH}	High-Level Output Voltage	R _n	2.5	—	—	V	V _{CC} = MIN: V _{IL} = 1.3 V; RE = 0.8 V; I _{OH} = MAX
V _{OHB}	High-Level Output Bus Voltage	I/O _n	1.9	—	—	V	V _{CC} = MAX: DN = DE = 0.8 V; V _T = 2.0 V; R _T = 10Ω; RE = 2.0 V I _{OH} = MAX
V _{OL}	Output LOW Voltage	R _n	—	0.35	0.5	V	V _{CC} = MIN: V _{IN} = 1.8 V; RE = 0.8 V; I _{OL} = 6.0 mA
V _{OLB}	Low Level Output Bus Voltage	I/O _n	0.75	1.0	1.2	V	D _n = DE = V _{IH} ; I _{OL} = 100 mA
			0.75	1.0	1.1		D _n = DE = V _{IH} ; I _{OL} = 80 mA
V _{OCB}	Driver Output Positive Clamp Voltage	I/O _n	—	—	2.9	V	V _{CC} = MAX or 0 V: DN = DE = 0.8 V; RE = 2.0 V
			—	—	3.2		
V _{IK}	Input Clamp Diode Voltage		—	-0.73	-1.2	V	V _{CC} = MIN, I _I = I _{IK}
I _I	Input Current at Maximum Input Voltage		—	—	100	μA	V _{CC} = MAX: V _I = 7.0 V; DE = RE = D _n = V _{CC}
I _{IH}	High Level Input Current	D _n , RE, DE	—	—	20	μA	V _{CC} = MAX: DE = RE = D _n = 2.5 V
I _{IHB}	High-Level I/O Bus Current (Power Off)	I/O _n	—	—	100	μA	V _{CC} = 0 V: DN = DE = 0.8 V; I/O _n = 1.2 V; RE = 0 V:
I _{IL}	Low-Level Input Current	RE	—	—	-100	μA	V _{CC} = MAX: V _I = 0.5V: DE = 4.5 V D _n = 4.5 V
		D _n	—	—	-200		
		DE	—	—	-500		
I _{ILB}	Low-Level I/O Bus Current (Power On)	I/O _n	-250	—	100	μA	V _{CC} = MAX: D _n = DE = 0.8 V; I/O _n = 0.75 V; RE = 0 V:
I _{OZH}	Off-State Output Current, High- Level Voltage Applied	R _n	—	—	20	μA	V _O = 2.5V; RE = 2.0 V V _{CC} = MAX: V _O = 0.5 V; RE = 2.0 V D _n = 1.2 V; V _O = 0 V; RE = 0.8 V
I _{OZL}	Off-State Output Current, Low-Level Voltage Applied		—	—	-20		
I _{OS}	Output Short Circuit Current (Note 3)		-80	—	-200		
I _{CC}	Supply Current (Total)		—	55	80	mA	V _{CC} = MAX: (RE = V _{IH} or V _{IL})

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- All typical values are at V_{CC} = 5.0 V, T_A = + 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

MC74F3893A

AC ELECTRICAL CHARACTERISTICS for Receiver and Receiver Enable

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$, $V_T = +2.0\text{V}$ $C_D = 30\text{ pF}$ $R_T = 10\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$, $V_T = +2.0\text{V}$ $C_D = 30\text{ pF}$ $R_T = 10\ \Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to I/O_n	—	—	—	1.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay DE to I/O_n	—	—	—	1.0	7.0	ns
t_{TLH} t_{THL}	D_n to I/O_n Transition Time 10% to 90%, 90% to 10%	—	—	—	1.0	5.0	ns
t_{Dskew}	Skew Between Receivers in Same Package	—	1.0	—	—	—	ns

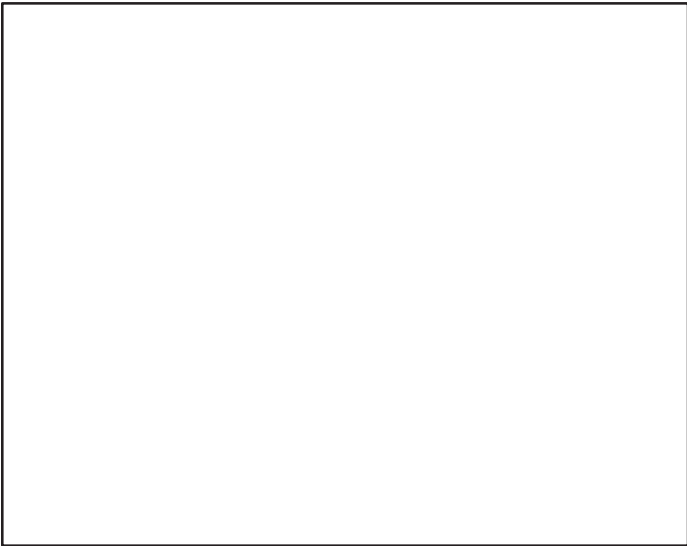
AC ELECTRICAL CHARACTERISTICS for Receiver

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ $R_L = 1.0\text{K}\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 1.0\text{K}\ \Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay I/O_n to R_n	—	—	—	2.0	8.0	ns
t_{Dskew}	Skew Between Receivers in Same Package	—	1.0	—	—	—	ns

AC ELECTRICAL CHARACTERISTICS for Receiver Enable

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		
		Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output Enable to High or Low Level RE to R_n	—	—	—	2.0	12.0	ns
t_{PHZ} t_{PLZ}	Output Disable From High or Low Level RE to R_n	—	—	—	1.0	8.0	ns

FAST AND LS TTL



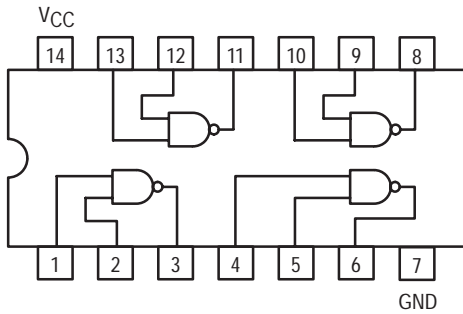
LS Data Sheets

5



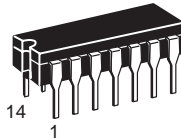
QUAD 2-INPUT NAND GATE

- ESD > 3500 Volts

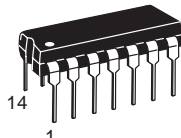


SN54/74LS00

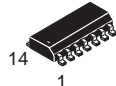
**QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY**



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH			1.6	mA	V _{CC} = MAX	
	Total, Output LOW			4.4			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

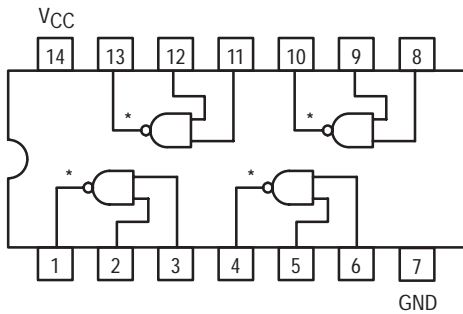
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	15	ns	



QUAD 2-INPUT NAND GATE

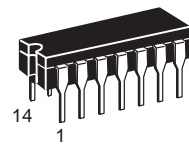
- ESD > 3500 Volts



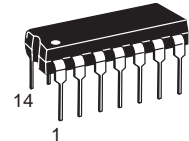
* OPEN COLLECTOR OUTPUTS

SN54/74LS01

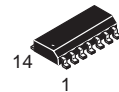
QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS01

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

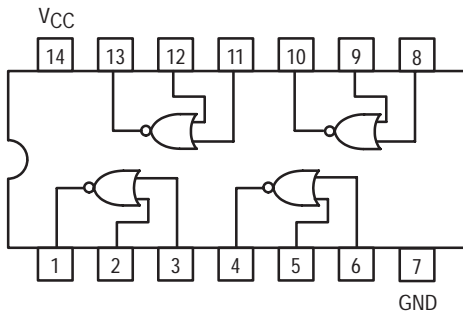
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH				1.6	mA	V _{CC} = MAX	
	Total, Output LOW				4.4			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			17	32	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			15	28			

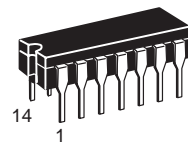


QUAD 2-INPUT NOR GATE

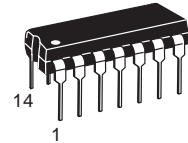


SN54/74LS02

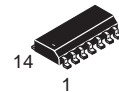
**QUAD 2-INPUT NOR GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
 SN74LSXXN Plastic
 SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS02

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH			3.2	mA	V _{CC} = MAX	
				5.4			
	Total, Output LOW						

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

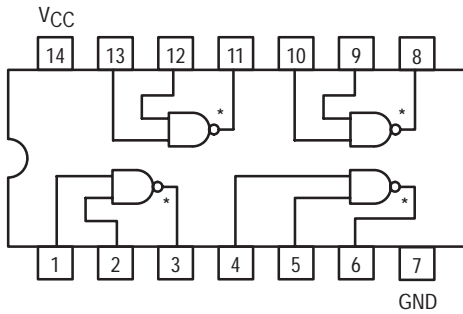
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		10	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	15	ns	



QUAD 2-INPUT NAND GATE

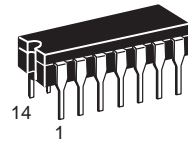
- ESD > 3500 Volts



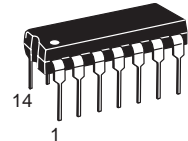
* OPEN COLLECTOR OUTPUTS

SN54/74LS03

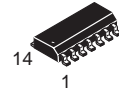
QUAD 2-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS03

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

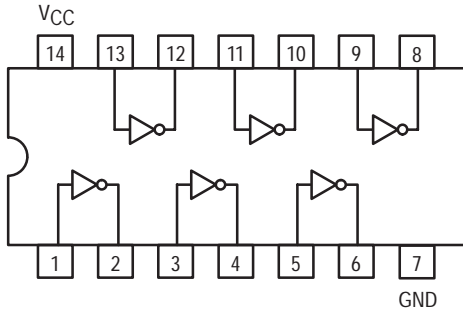
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				1.6	mA	V _{CC} = MAX	
					4.4			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			17	32	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			15	28	ns		



HEX INVERTER



SN54/74LS04

**HEX INVERTER
LOW POWER SCHOTTKY**

**J SUFFIX
CERAMIC
CASE 632-08**

**N SUFFIX
PLASTIC
CASE 646-06**

**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS04

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			2.4	mA	V _{CC} = MAX	
				6.6			

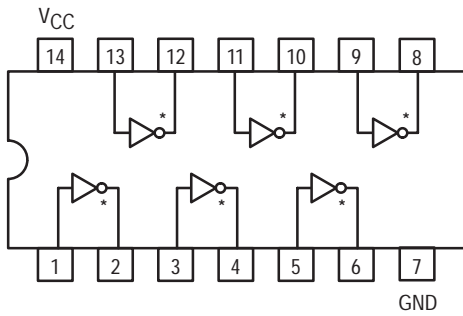
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	15	ns	



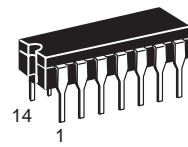
HEX INVERTER



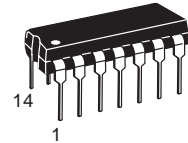
* OPEN COLLECTOR OUTPUTS

SN54/74LS05

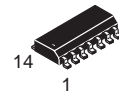
HEX INVERTER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS05

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

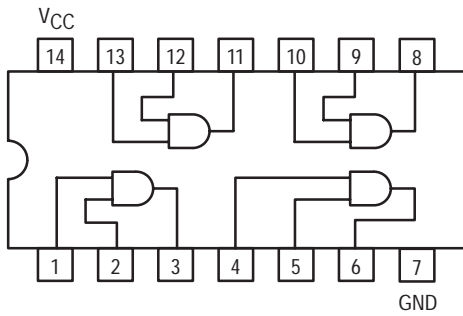
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				2.4	mA	V _{CC} = MAX	
					6.6			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			17	32	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			15	28	ns		

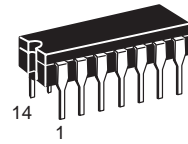


QUAD 2-INPUT AND GATE

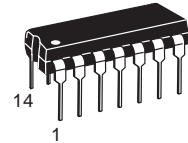


SN54/74LS08

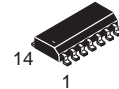
**QUAD 2-INPUT AND GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS08

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH				4.8	mA	V _{CC} = MAX	
	Power Supply Current Total, Output LOW				8.8			

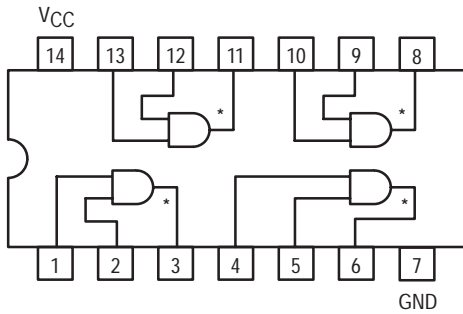
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			8.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF	
t _{PHL}	Turn-On Delay, Input to Output			10	20	ns		



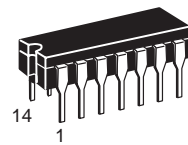
QUAD 2-INPUT AND GATE



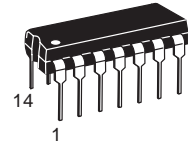
* OPEN COLLECTOR OUTPUTS

SN54/74LS09

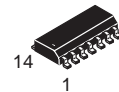
QUAD 2-INPUT AND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS09

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

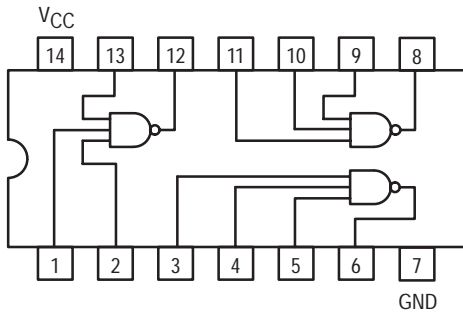
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				4.8	mA	V _{CC} = MAX	
					8.8			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			20	35	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			17	35	ns		

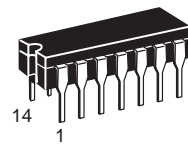


TRIPLE 3-INPUT NAND GATE

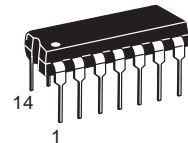


SN54/74LS10

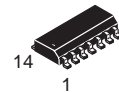
**TRIPLE 3-INPUT NAND GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS10

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			1.2	mA	V _{CC} = MAX	
				3.3			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

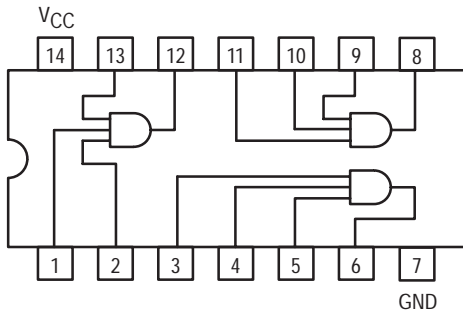
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	15	ns	



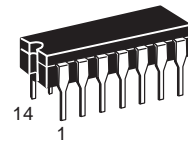
MOTOROLA

TRIPLE 3-INPUT AND GATE

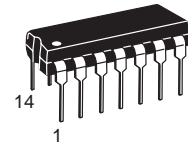


SN54/74LS11

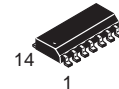
**TRIPLE 3-INPUT AND GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS11

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			3.6	mA	V _{CC} = MAX	
				6.6			

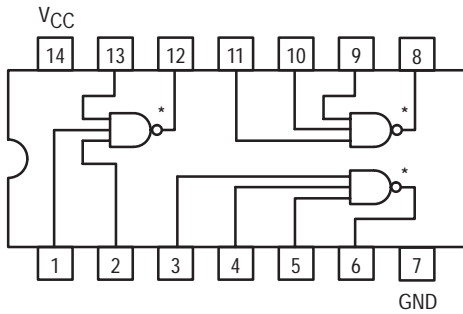
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	20	ns	



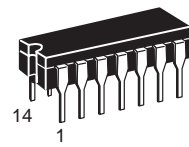
TRIPLE 3-INPUT NAND GATE



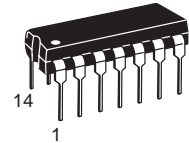
*OPEN COLLECTOR OUTPUTS

SN54/74LS12

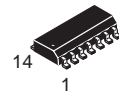
TRIPLE 3-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS12

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				1.4	mA	V _{CC} = MAX	
					3.3			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			17	32	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			15	28	ns		

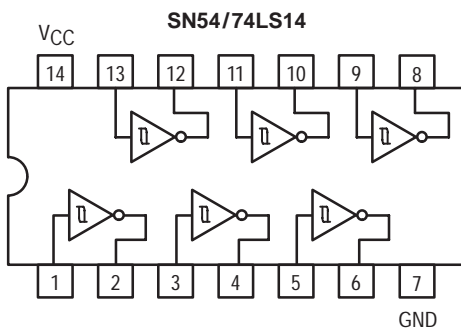
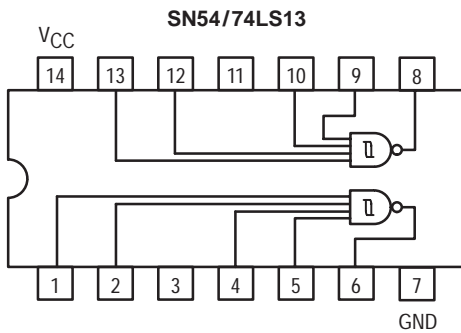


SCHMITT TRIGGERS DUAL GATE/HEX INVERTER

The SN54LS/74LS13 and SN54LS/74LS14 contain logic gates/inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional inverters.

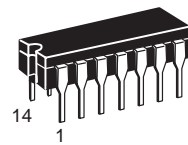
Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

LOGIC AND CONNECTION DIAGRAMS

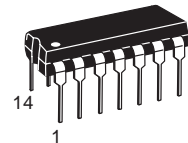


**SN54/74LS13
SN54/74LS14**

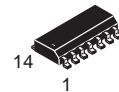
**SCHMITT TRIGGERS
DUAL GATE/HEX INVERTER
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS13 • SN54/74LS14

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{T+}	Positive-Going Threshold Voltage	1.5		2.0	V	$V_{CC} = 5.0\text{ V}$	
V_{T-}	Negative-Going Threshold Voltage	0.6		1.1	V	$V_{CC} = 5.0\text{ V}$	
$V_{T+} - V_{T-}$	Hysteresis	0.4	0.8		V	$V_{CC} = 5.0\text{ V}$	
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}, I_{IN} = -18\text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.4	V	$V_{CC} = \text{MIN}, I_{OH} = -400\text{ }\mu\text{A}, V_{IN} = V_{IL}$	
		74	2.7	3.4	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = \text{MIN}, I_{OL} = 4.0\text{ mA}, V_{IN} = 2.0\text{ V}$
		74		0.35	0.5	V	$V_{CC} = \text{MIN}, I_{OL} = 8.0\text{ mA}, V_{IN} = 2.0\text{ V}$
I_{T+}	Input Current at Positive-Going Threshold		-0.14		mA	$V_{CC} = 5.0\text{ V}, V_{IN} = V_{T+}$	
I_{T-}	Input Current at Negative-Going Threshold		-0.18		mA	$V_{CC} = 5.0\text{ V}, V_{IN} = V_{T-}$	
I_{IH}	Input HIGH Current		1.0	20	μA	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}, V_{OUT} = 0\text{ V}$	
I_{CC}	Power Supply Current					$V_{CC} = \text{MAX}$	
	Total, Output HIGH	LS13	2.9	6.0	mA		
		LS14	8.6	16			
	Total, Output LOW	LS13	4.1	7.0	mA		
	LS14	12	21				

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Max		Unit	Test Conditions
		LS13	LS14		
t_{PLH}	Propagation Delay, Input to Output	22	22	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
t_{PHL}	Propagation Delay, Input to Output	27	22	ns	

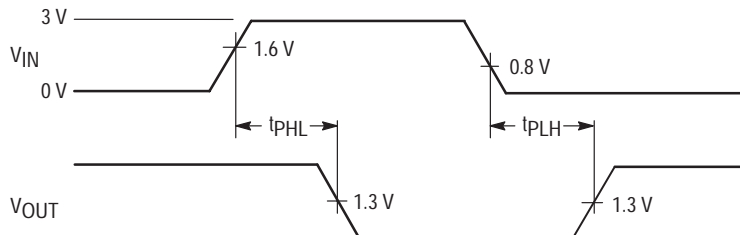


Figure 1. AC Waveforms

SN54/74LS13 • SN54/74LS14

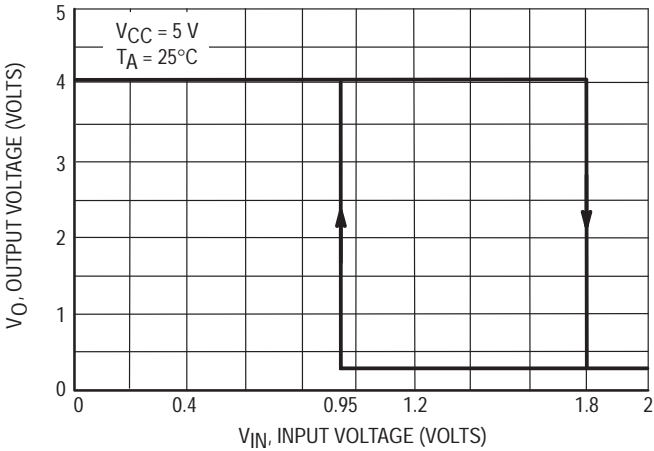


Figure 2. V_{IN} versus V_{OUT} Transfer Function

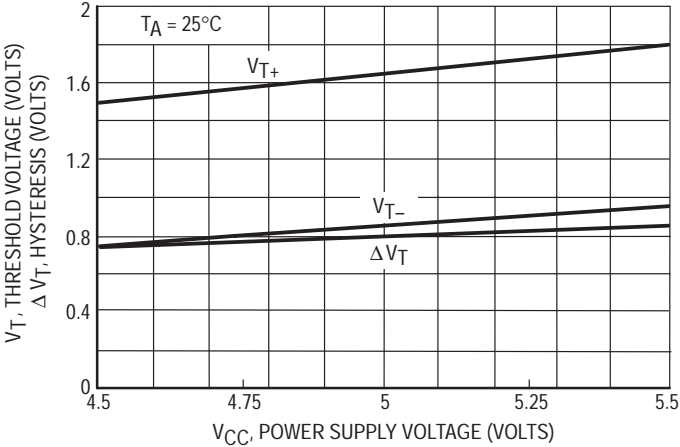


Figure 3. Threshold Voltage and Hysteresis versus Power Supply Voltage

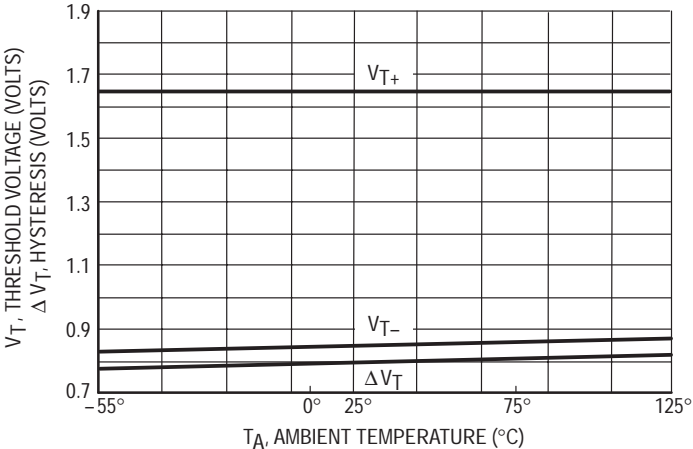
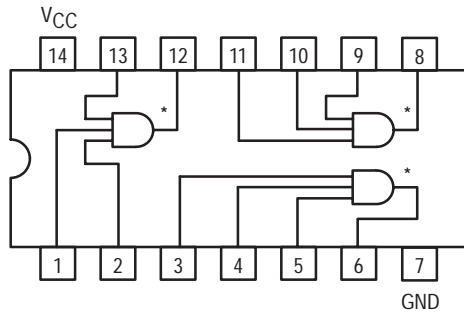


Figure 4. Threshold Voltage Hysteresis versus Temperature



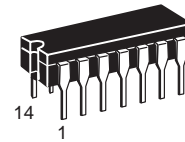
TRIPLE 3-INPUT AND GATE



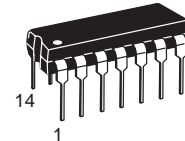
*OPEN COLLECTOR OUTPUTS

SN54/74LS15

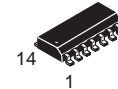
TRIPLE 3-INPUT AND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS15

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

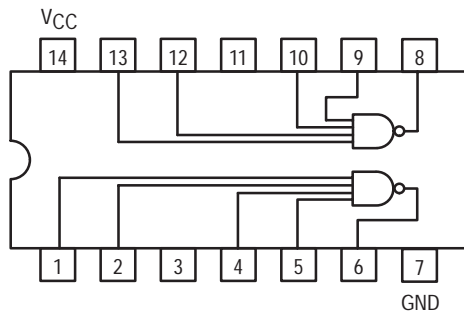
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
I_{OH}	Output HIGH Current	54, 74		100	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table
		74	0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			3.6	mA	$V_{CC} = \text{MAX}$
				6.6		

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		20	35	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t_{PHL}	Turn-On Delay, Input to Output		17	35	ns	

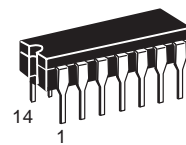


DUAL 4-INPUT NAND GATE

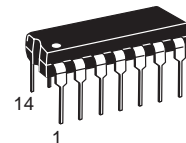


SN54/74LS20

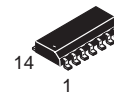
DUAL 4-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS20

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			0.8	mA	$V_{CC} = \text{MAX}$	
				2.2			

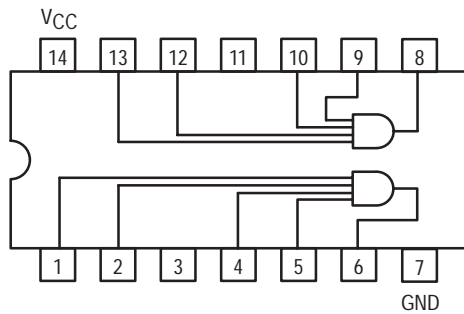
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

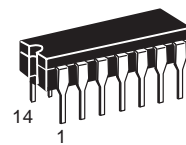


DUAL 4-INPUT AND GATE

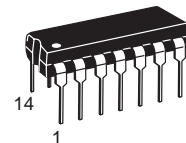


SN54/74LS21

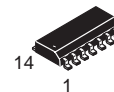
DUAL 4-INPUT AND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS21

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			2.4	mA	V _{CC} = MAX	
				4.4			

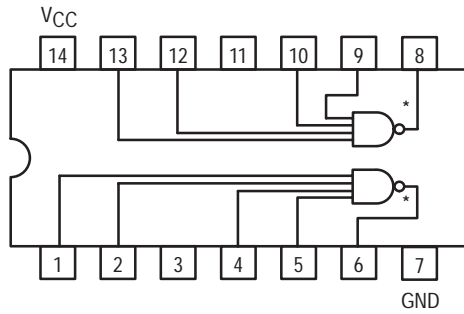
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		10	20	ns	



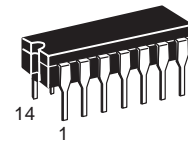
DUAL 4-INPUT NAND GATE



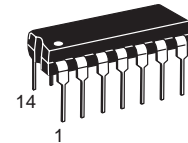
* OPEN COLLECTOR OUTPUTS

SN54/74LS22

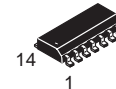
DUAL 4-INPUT NAND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			55	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS22

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				0.8	mA	V _{CC} = MAX	
					2.2			

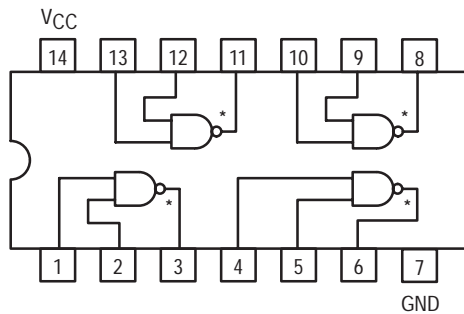
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			17	32	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}	Turn-On Delay, Input to Output			15	28	ns		



QUAD 2-INPUT NAND BUFFER

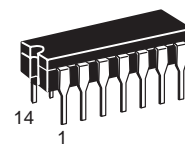
- ESD > 3500 Volts



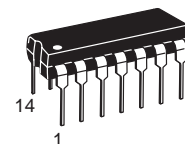
*OPEN COLLECTOR OUTPUTS

SN54/74LS26

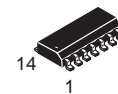
QUAD 2-INPUT NAND BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			15	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS26

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

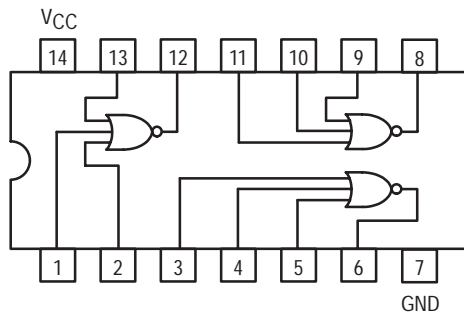
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
I_{OH}	Output HIGH Current	54, 74		1000	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$
		54, 74		50	μA	$V_{CC} = \text{MIN}$, $V_{OH} = 12 \text{ V}$
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
		74	0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{CC}	Power Supply Current Total, Output HIGH			1.6	mA	$V_{CC} = \text{MAX}$
				4.4		
	Total, Output LOW					

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		17	32	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t_{PHL}	Turn-On Delay, Input to Output		15	28	ns	

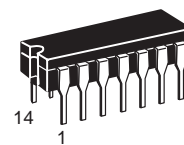


TRIPLE 3-INPUT NOR GATE

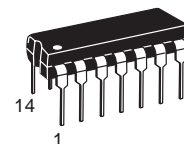


SN54/74LS27

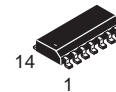
**TRIPLE 3-INPUT NOR GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS27

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH			4.0	mA	$V_{CC} = \text{MAX}$	
	Total, Output LOW			6.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

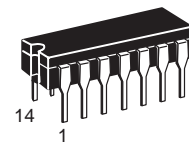
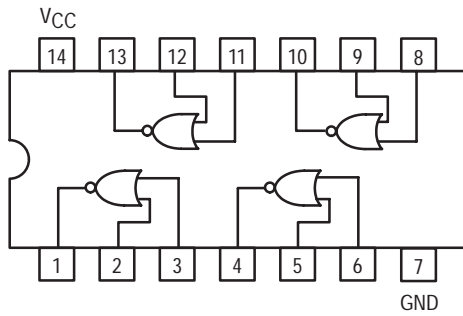
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		10	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	



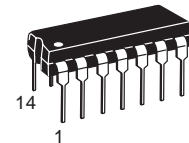
QUAD 2-INPUT NOR BUFFER

SN54/74LS28

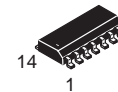
QUAD 2-INPUT NOR BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-1.2	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS28

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH			3.6	mA	$V_{CC} = \text{MAX}$	
	Total, Output LOW			13.8			

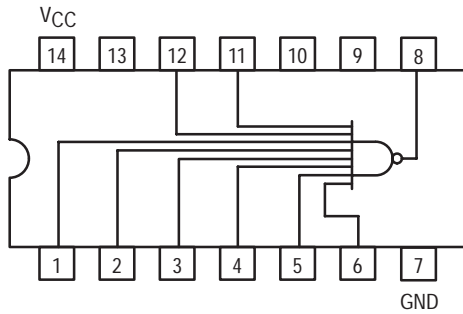
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Propagation Delay		12	24	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$
t_{PHL}	Propagation Delay		12	24	ns	

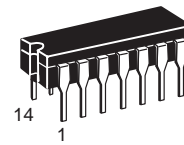


8-INPUT NAND GATE

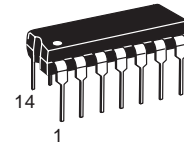


SN54/74LS30

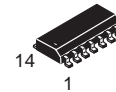
**8-INPUT NAND GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS30

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH				0.5	mA	V _{CC} = MAX	
	Power Supply Current Total, Output LOW				1.1			

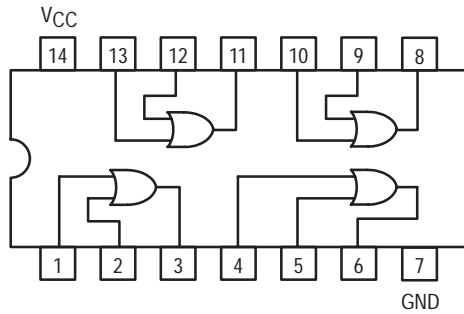
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			8.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF	
t _{PHL}	Turn-On Delay, Input to Output			13	20	ns		

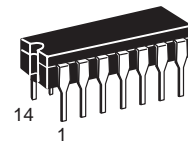


QUAD 2-INPUT OR GATE

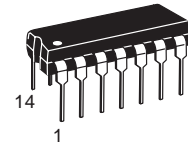


SN54/74LS32

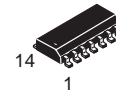
QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS32

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH				6.2	mA	V _{CC} = MAX	
	Power Supply Current Total, Output LOW				9.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

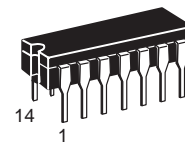
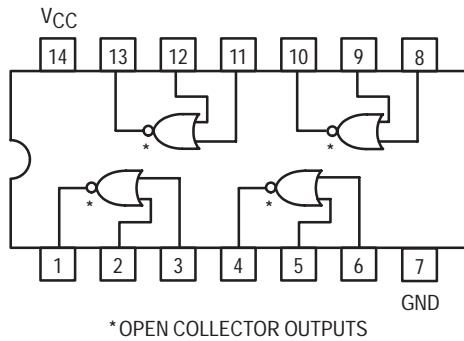
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			14	22	ns	V _{CC} = 5.0 V C _L = 15 pF	
t _{PHL}	Turn-On Delay, Input to Output			14	22	ns		



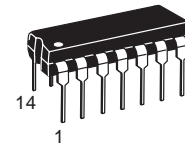
QUAD 2-INPUT NOR BUFFER

SN54/74LS33

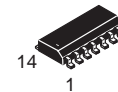
QUAD 2-INPUT NOR BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS33

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

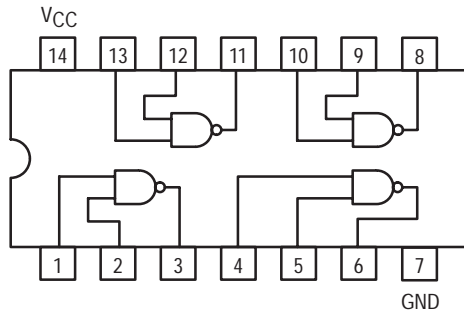
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
I _{OH}	Output HIGH Current	54, 74			250	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current Total, Output HIGH				3.6	mA	V _{CC} = MAX	
	Total, Output LOW				13.8			

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			20	32	ns	V _{CC} = 5.0 V, R _L = 667 Ω C _L = 45 pF	
t _{PHL}	Turn-On Delay, Input to Output			18	28			

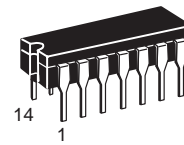


QUAD 2-INPUT NAND BUFFER

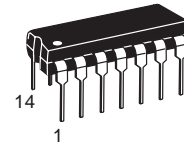


SN54/74LS37

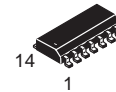
QUAD 2-INPUT NAND BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-1.2	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS37

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V		
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH				2.0	mA	V _{CC} = MAX	
	Power Supply Current Total, Output LOW				12			

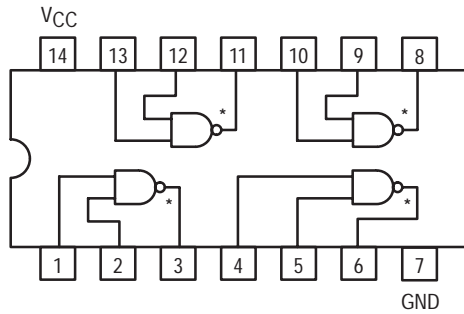
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Turn-Off Delay, Input to Output			12	24	ns	V _{CC} = 5.0 V, R _L = 667 Ω C _L = 45 pF	
t _{PHL}	Turn-On Delay, Input to Output			12	24			



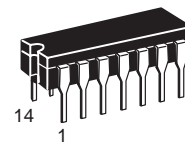
QUAD 2-INPUT NAND BUFFER



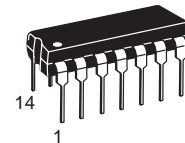
*OPEN COLLECTOR OUTPUTS

SN54/74LS38

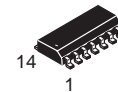
QUAD 2-INPUT NAND BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS38

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

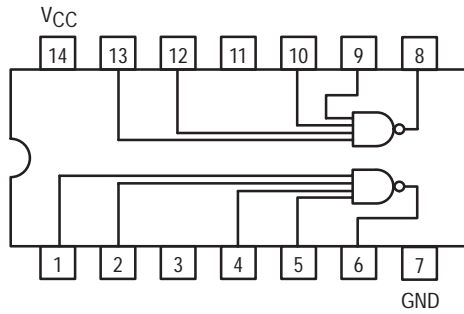
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
I_{OH}	Output HIGH Current	54, 74			250	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table
		74		0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	
I_{IH}	Input HIGH Current				20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.4 \text{ V}$	
					0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current				-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{CC}	Power Supply Current Total, Output HIGH				2.0	mA	$V_{CC} = \text{MAX}$	
	Total, Output LOW				12			

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t_{PLH}	Turn-Off Delay, Input to Output			20	32	ns	$V_{CC} = 5.0 \text{ V}$, $R_L = 667 \Omega$ $C_L = 45 \text{ pF}$	
t_{PHL}	Turn-On Delay, Input to Output			18	28			

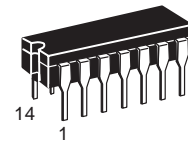


DUAL 4-INPUT NAND BUFFER

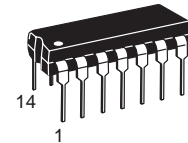


SN54/74LS40

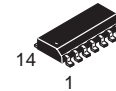
DUAL 4-INPUT NAND BUFFER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-1.2	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS40

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			1.0	mA	$V_{CC} = \text{MAX}$	
				6.0			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		12	24	ns	$V_{CC} = 5.0 \text{ V}$, $R_L = 667 \Omega$ $C_L = 45 \text{ pF}$
t_{PHL}	Turn-On Delay, Input to Output		12	24	ns	

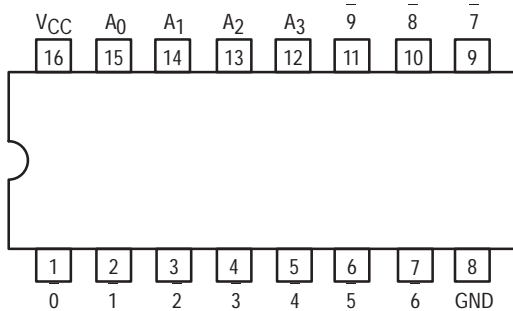


ONE-OF-TEN DECODER

The LSTTL/MSI SN54/74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Mutually Exclusive Outputs
- Demultiplexing Capability
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0 - A_3 Address Inputs
0 to 9 Outputs, Active LOW (Note b)

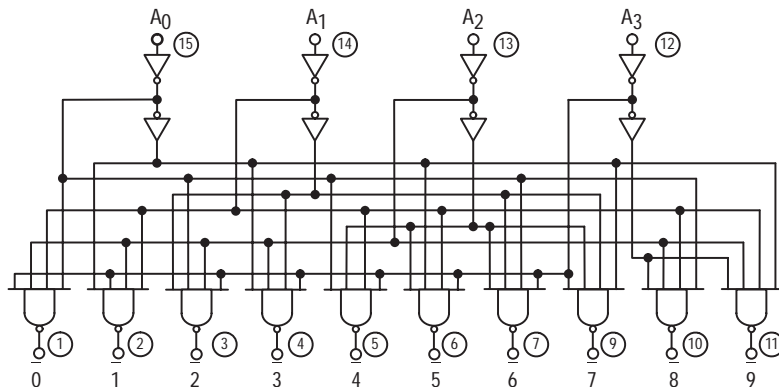
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	5(2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

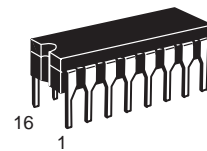
LOGIC DIAGRAM



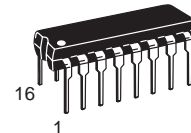
V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS42

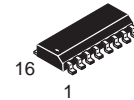
ONE-OF-TEN DECODER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

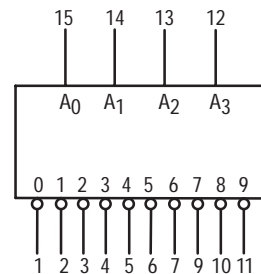


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS42

FUNCTIONAL DESCRIPTION

The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied

to the inputs.

The most significant input A₃ produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A₃ input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A ₀	A ₁	A ₂	A ₃	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS42

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$	
I_{IH}	Input HIGH Current				20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
					0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current				-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)		-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current				13	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)			15 15	25 25	ns	Figure 2	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)			20 20	30 30	ns	Figure 1	

AC WAVEFORMS

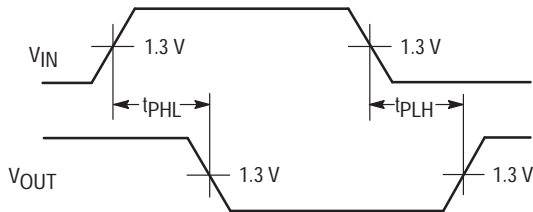


Figure 1

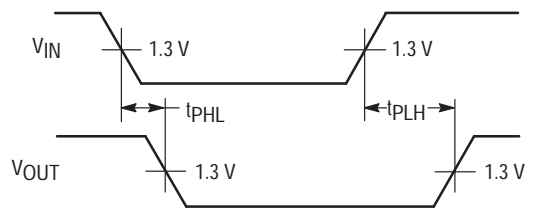


Figure 2



BCD TO 7-SEGMENT DECODER/DRIVER

The SN54/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

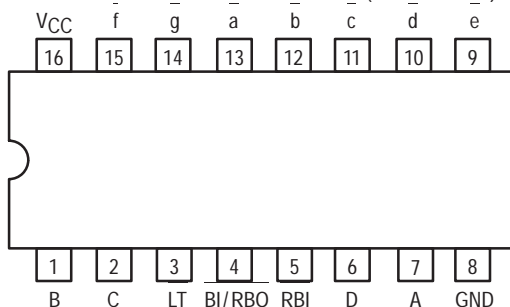
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μ A. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

A, B, C, D	BCD Inputs
RBI	Ripple-Blanking Input
LT	Lamp-Test Input
BI/RBO	Blanking Input or Ripple-Blanking Output
a, to g	Outputs

LOADING (Note a)

	HIGH	LOW
A, B, C, D	0.5 U.L.	0.25 U.L.
RBI	0.5 U.L.	0.25 U.L.
LT	0.5 U.L.	0.25 U.L.
BI/RBO	0.5 U.L.	0.75 U.L.
a, to g	1.2 U.L.	2.0 U.L.
Open-Collector		15 (7.5) U.L.

NOTES:

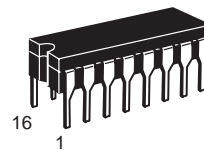
a) 1 Unit Load (U.L.) = 40 μ A HIGH, 1.6 mA LOW.

b) Output current measured at $V_{OUT} = 0.5$ V

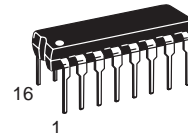
The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS47

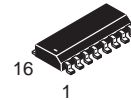
BCD TO 7-SEGMENT DECODER/DRIVER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

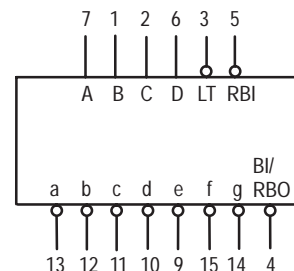


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

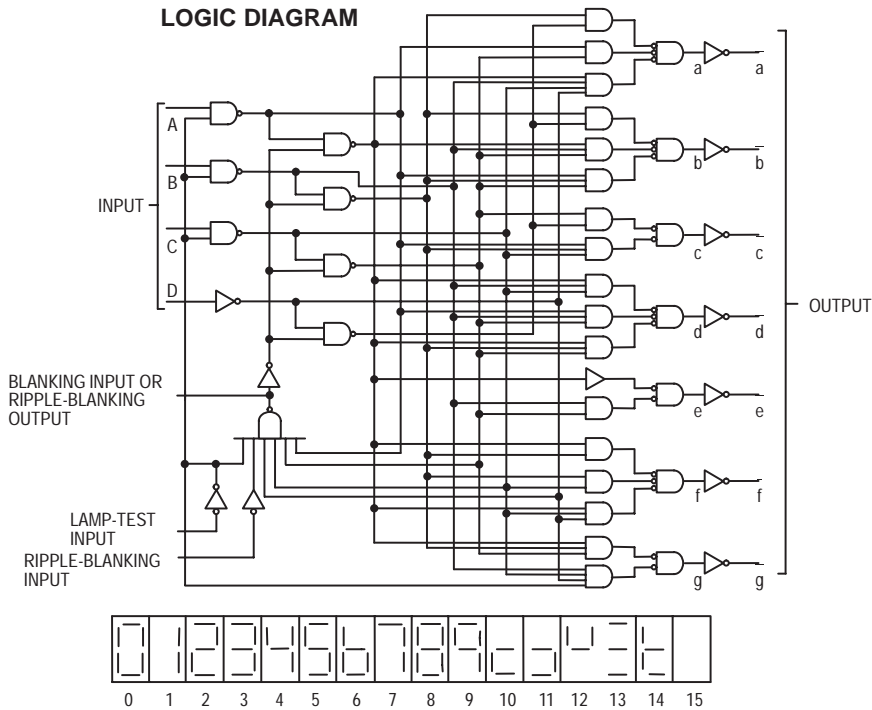
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
 GND = PIN 8

SN54/74LS47



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS						OUTPUTS							NOTE	
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B	A	$\overline{\text{BI/RBO}}$	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$		$\overline{\text{g}}$
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

- (A) BI/RBO is wire-AND logic serving as blanking Input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.
- (B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.
- (C) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (D) When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

SN54/74LS47

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High BI/RBO	54, 74			-50	μA
I _{OL}	Output Current — Low BI/RBO BI/RBO	54			1.6	mA
		74			3.2	
V _{O (off)}	Off-State Output Voltage \bar{a} to \bar{g}	54, 74			15	V
I _{O (on)}	On-State Output Current \bar{a} to \bar{g} \bar{a} to \bar{g}	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Theshold Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage, \bar{BI}/\bar{RBO}	2.4	4.2		V	V _{CC} = MIN, I _{OH} = -50 μA, V _{IN} = V _{IN} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage BI/RBO	54, 74	0.25	0.4	V	I _{OL} = 1.6 mA V _{CC} = MIN, V _{IN} = V _{IN} or V _{IL} per Truth Table
		74	0.35	0.5	V	
I _{O (off)}	Off-State Output Current a thru g			250	μA	V _{CC} = MAX, V _{IN} = V _{IN} or V _{IL} per Truth Table, V _{O (off)} = 15 V
V _{O (on)}	On-State Output Voltage a thru g	54, 74	0.25	0.4	V	I _{O (on)} = 12 mA V _{CC} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current BI/RBO Any Input except BI/RBO			-1.2 -0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS BI/RBO}	Output Short Circuit Current (Note 1)	-0.3		-2.0	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		7.0	13	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PHL}	Propagation Delay, Address			100	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Input to Segment Output			100		
t _{PHL}	Propagation Delay, RBI Input			100	ns	
t _{PLH}	To Segment Output			100		

AC WAVEFORMS

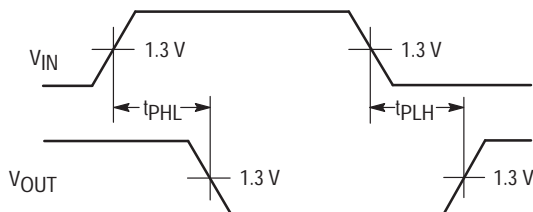


Figure 1

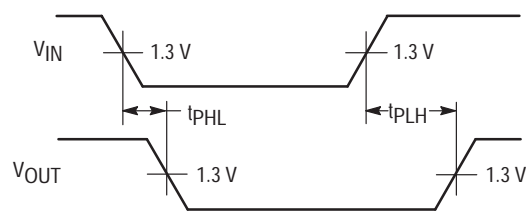


Figure 2



BCD TO 7-SEGMENT DECODER

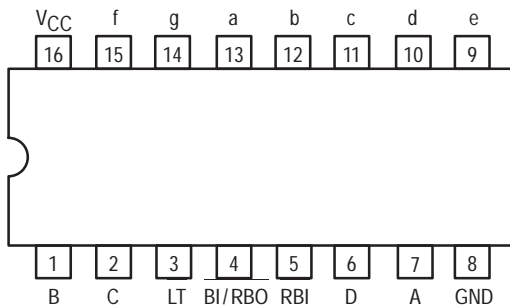
The SN54/74LS48 is a BCD to 7-Segment Decoder consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking input for the LS48.

The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables.

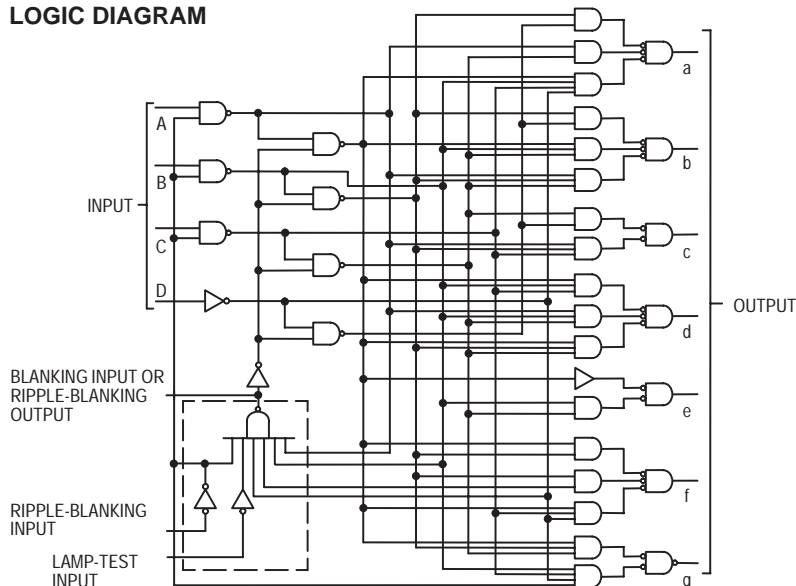
The LS48 circuit incorporates automatic leading and/or trailing edge zero-blanking control (RBI and RBO). Lamp Test (LT) may be activated any time when the BI/RBO node is HIGH. Both devices contain an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

- Lamp Intensity Modulation Capability (BI/RBO)
- Internal Pull-Ups Eliminate Need for External Resistors
- Input Clamp Diodes Eliminate High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

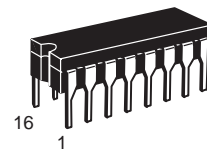


LOGIC DIAGRAM

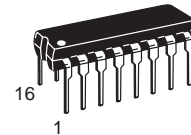


SN54/74LS48

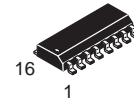
BCD TO 7-SEGMENT DECODER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

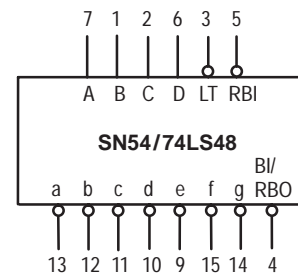


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS48

PIN NAMES

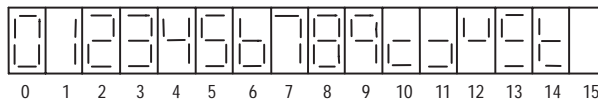
A, B, C, D	BCD Inputs
RBI	Ripple-Blanking (Active Low) Input
LT	Lamp-Test (Active Low) Input
BI/RBO	Blanking Input or Ripple-Blanking Output (Active Low)
—	Blanking Output (Active Low)
BI	Blanking (Active Low) Input

LOADING (Note a)

	HIGH	LOW
	0.5 U.L.	0.25 U.L.
	0.5 U.L.	0.25 U.L.
	0.5 U.L.	0.25 U.L.
	0.5 U.L.	0.75 U.L.
	1.2 U.L.	2(1) U.L.
	0.5 U.L.	0.25 U.L.
Open-Collector		3.75 (1.25) U.L. (48)

NOTES:

- a) Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW
 b) Output current measured at $V_{OUT} = 0.5$ V
 Output LOW drive factor is SN54LS/74LS48: 1.25 U.L. for Military (54), 3.75 U.L. for Commercial (74).



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE SN54/74LS48

DECIMAL OR FUNCTION	INPUTS						OUTPUTS							NOTE	
	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f		g
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	L	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	L	H	L	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

- BI/RBO is wired-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.
- When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
- When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

SN54/74LS48

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage		4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range		-55 0	25 25	125 70	°C
I _{OH}	Output Current — High a to g	54, 74			-100	μA
I _{OH}	Output Current — High BI/RBO	54, 74			-50	μA
I _{OL}	Output Current — Low a to g	54 74			2.0 6.0	mA
I _{OL}	Output Current — Low BI/RBO	54 74			1.6 3.2	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage			-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	4.2		μA	V _{CC} = MIN, I _{OH} = -50 μA, V _{IN} = V _{IH} or U.L. per Truth Table
I _O	Output Current a to g	-1.3	-2.0		mA	V _{CC} = MIN, V _O = 0.85 V Input Conditioner as for V _{OH}
V _{OL}	Output LOW Voltage a to g	54, 74		0.4	V	I _{OL} = 2.0 mA V _{CC} = MIN, V _{IH} = 2.0 V V _{IL} = V _{IL} MAX
		74		0.5	V	
V _{OL}	Output LOW Voltage BI/RBO	54, 74		0.4	V	I _{OL} = 1.6 mA V _{CC} = MAX, V _{IH} = 2.0 V V _{IL} = V _{IL} MAX
		74		0.5	V	
I _{IH}	Input HIGH Current (Except BI/RBO)			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current (Except BI/RBO)			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{IL}	Input LOW Current BI/RBO			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current		25	38	mA	V _{CC} = MAX
I _{OS}	Short Circuit Current BI/RBO (Note 1)	-0.3		-2.0	mA	V _{CC} = MAX

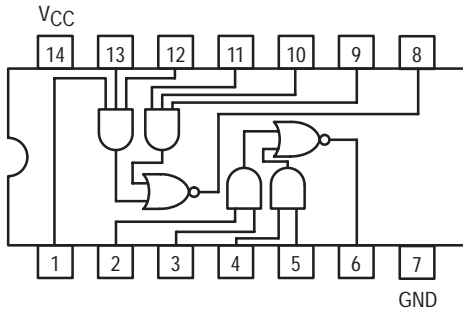
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from A Input			100	ns	C _L = 15 pF, R _L = 4.0 kΩ
t _{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from A Input			100	ns	
t _{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from RBI Input			100	ns	C _L = 15 pF, R _L = 6.0 kΩ
t _{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from RBI Input			100	ns	

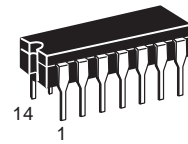


DUAL 2-WIDE 2-INPUT/ 3-INPUT AND-OR-INVERT GATE

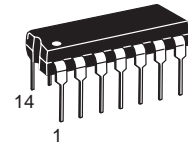


SN54/74LS51

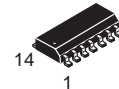
**DUAL 2-WIDE 2-INPUT/
3-INPUT AND-OR-INVERT GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS51

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			1.6	mA	V _{CC} = MAX	
				2.8			

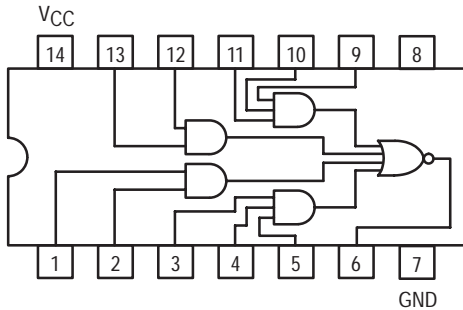
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		12.5	20	ns	

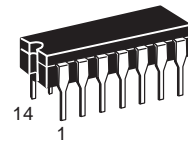


3-2-2-3-INPUT AND-OR-INVERT GATE

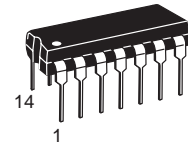


SN54/74LS54

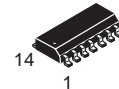
**3-2-2-3-INPUT
AND-OR-INVERT GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
 SN74LSXXN Plastic
 SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS54

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			1.6	mA	V _{CC} = MAX	
				2.0			

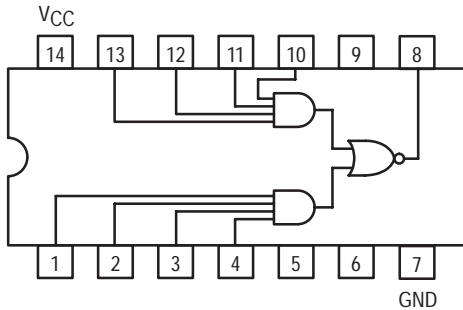
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		12.5	20	ns	

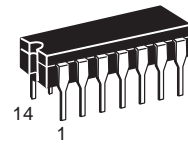


2-WIDE 4-INPUT AND-OR-INVERT GATE

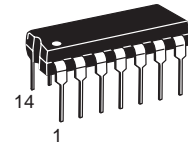


SN54/74LS55

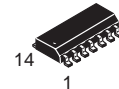
**2-WIDE 4-INPUT
AND-OR-INVERT GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
 SN74LSXXN Plastic
 SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS55

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			0.8	mA	V _{CC} = MAX	
				1.3			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

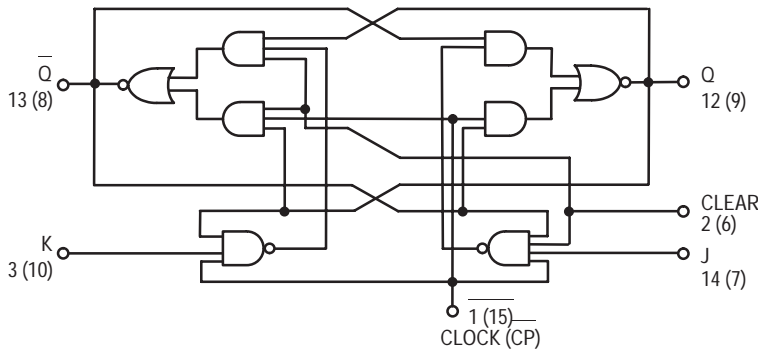
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		12	20	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		12.5	20	ns	



DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	C_D	J	K	Q	\bar{Q}
Reset (Clear)	L	X	X	\underline{L}	H
Toggle	H	h	h	q	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	\underline{L}
Hold	H	l	l	q	q

H, h = HIGH Voltage Level

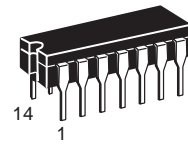
L, l = LOW Voltage Level

X = Don't Care

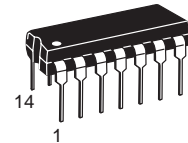
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS73A

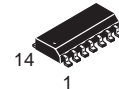
**DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**

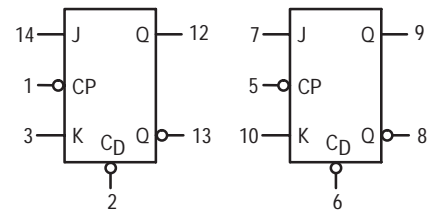


**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
 SN74LSXXN Plastic
 SN74LSXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 4
 GND = PIN 11

SN54/74LS73A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		J, K Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		15 15	20 20	ns ns	Figure 1

V_{CC} = 5.0 V
C_L = 15 pF

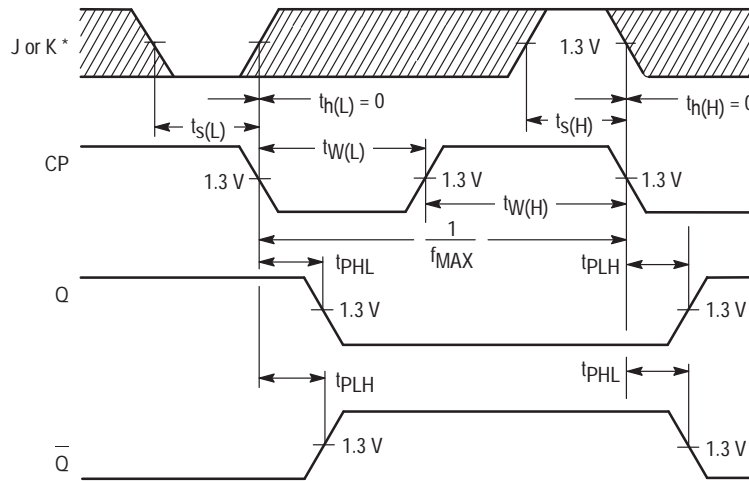
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	Figure 1
t _W	Clear Pulse Width	25			ns	Figure 2
t _S	Setup Time	20			ns	Figure 1
t _H	Hold Time	0			ns	

V_{CC} = 5.0 V

SN54/74LS73A

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width

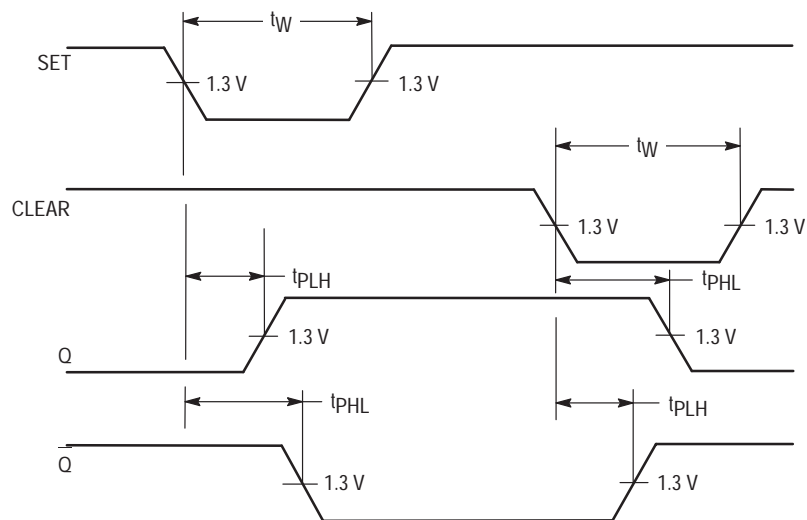


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths

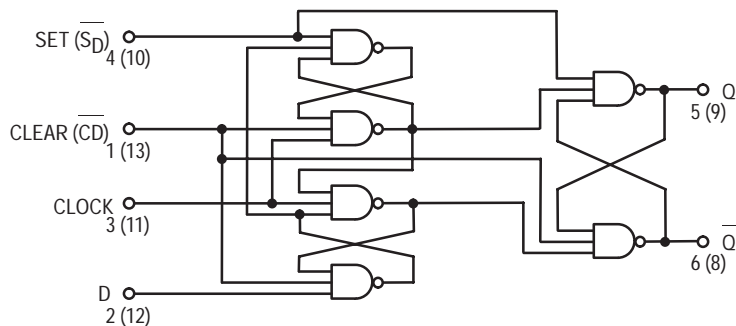


DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and Q outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	S _D	S _D	D	Q	Q
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

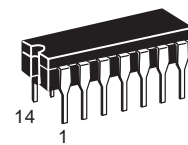
X = Don't Care

i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

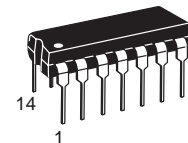
SN54/74LS74A

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

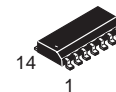
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

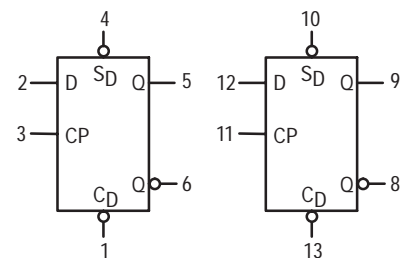


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

SN54/74LS74A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input High Current Data, Clock Set, Clear			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Data, Clock Set, Clear			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Data, Clock Set, Clear			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			8.0	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

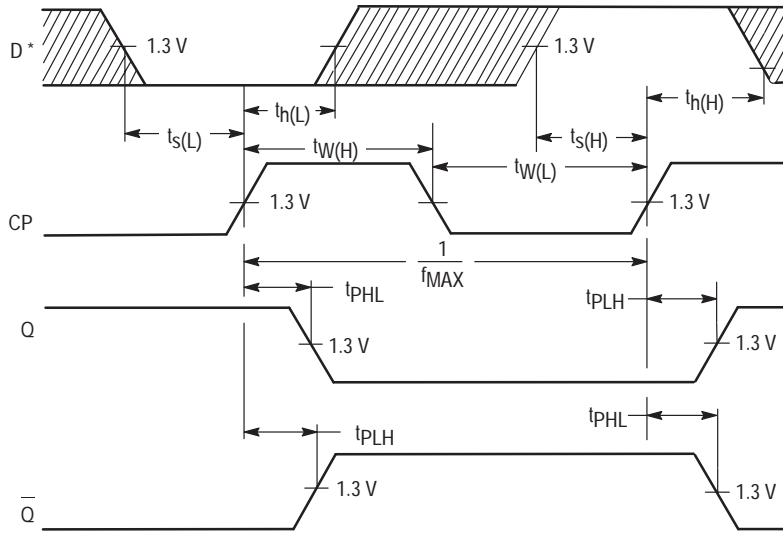
Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f _{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1	
			25	40	ns		

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t _{W(H)}	Clock	25			ns	Figure 1	V _{CC} = 5.0 V
t _{W(L)}	Clear, Set	25			ns	Figure 2	
t _s	Data Setup Time — HIGH LOW	20			ns	Figure 1	
		20			ns		
t _h	Hold Time	5.0			ns	Figure 1	

SN54/74LS74A

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width

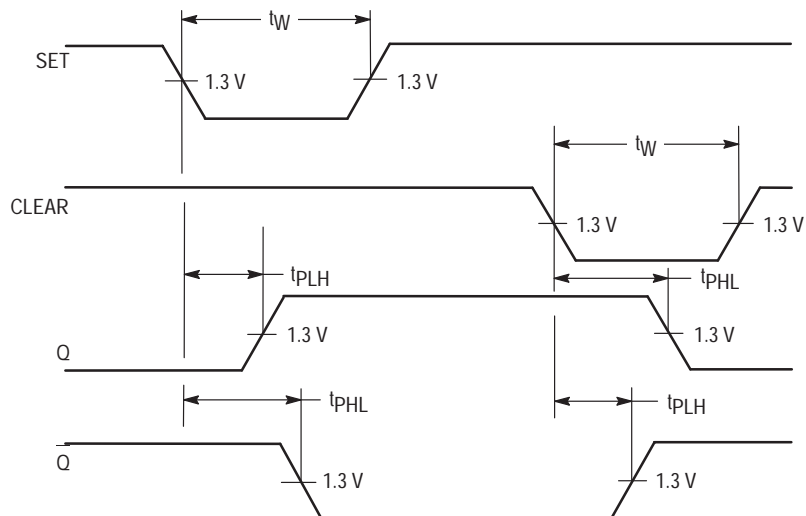


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths

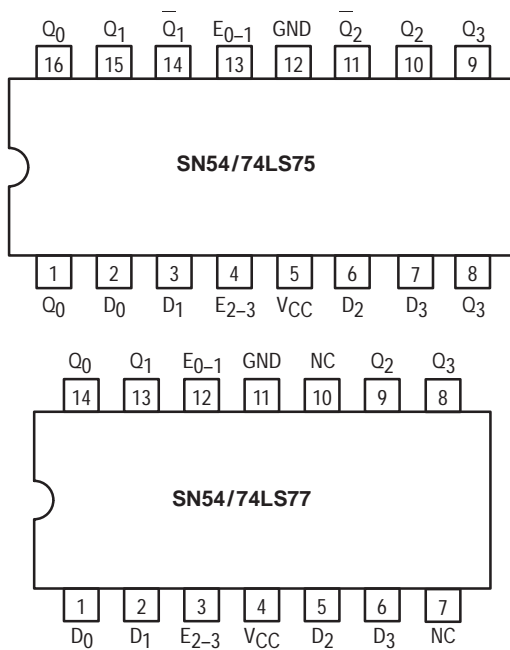


4-BIT D LATCH

The TTL/MSI SN54/74LS75 and SN54/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54/74LS75 features complementary Q and Q output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54/74LS77 4-bit latch is available in the 14-pin package with Q outputs omitted.

CONNECTION DIAGRAMS DIP (TOP VIEW)



PIN NAMES

D ₁ -D ₄	Data Inputs
E ₀₋₁	Enable Input Latches 0, 1
E ₂₋₃	Enable Input Latches 2, 3
Q ₁ -Q ₄	Latch Outputs (Note b)
Q ₁ -Q ₄	Complimentary Latch Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
D ₁ -D ₄	0.5 U.L.	0.25 U.L.
E ₀₋₁	2.0 U.L.	1.0 U.L.
E ₂₋₃	2.0 U.L.	1.0 U.L.
Q ₁ -Q ₄	10 U.L.	5 (2.5) U.L.
Q ₁ -Q ₄	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 Unit Load (U.L.) = 40 μA HIGH.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

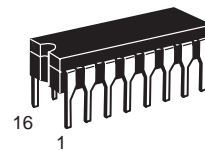
TRUTH TABLE (Each latch)

t _n	t _{n+1}
D	Q
H	H
L	L

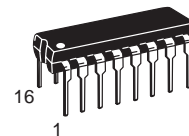
NOTES:
 t_n = bit time before enable negative-going transition
 t_{n+1} = bit time after enable negative-going transition

SN54/74LS75 SN54/74LS77

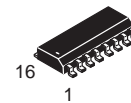
4-BIT D LATCH LOW POWER SCHOTTKY



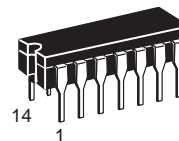
J SUFFIX
CERAMIC
CASE 620-09



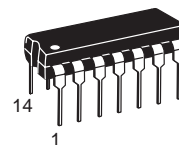
N SUFFIX
PLASTIC
CASE 648-08



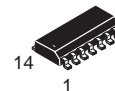
D SUFFIX
SOIC
CASE 751B-03



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



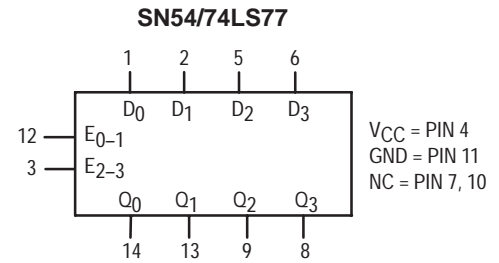
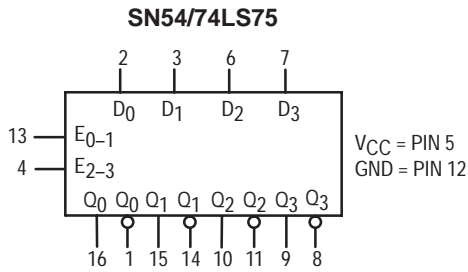
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

SN54/74LS75

LOGIC SYMBOLS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current	D Input		20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
		E Input		80			
I_{IL}	Input LOW Current	D Input		0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
		E Input		0.4			
I_{OL}	Output LOW Current			-0.4 -1.6	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			12	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, Data to \bar{Q}		12 7.0	20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to \bar{Q}		16 7.0	30 15	ns	

SN54/74LS77

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

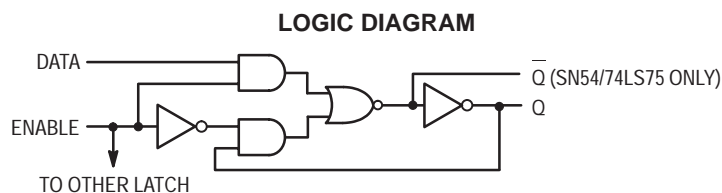
Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	D Input			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		E Input			80		
I _{IL}	Input LOW Current	D Input			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		E Input			0.4		
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				13	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Q			11 9.0	19 17	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Enable to Q			10 10	18 18		

SN54/74LS75 • SN54/74LS77



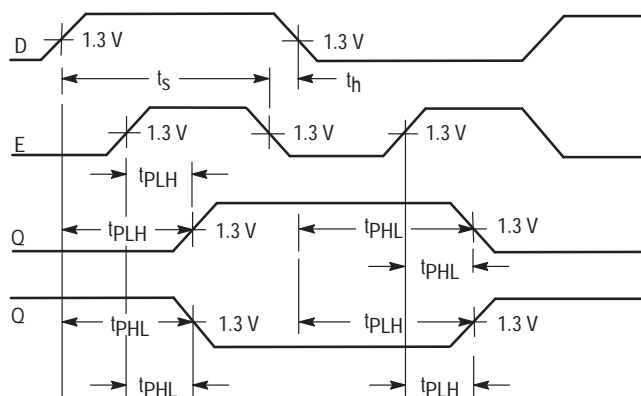
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Enable Pulse Width High	20			ns	$V_{CC} = 5.0\text{ V}$
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

AC WAVEFORMS



DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.



DUAL JK FLIP-FLOP WITH SET AND CLEAR

The SN54/74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	S _D	C _D	J	K	Q	\bar{Q}
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	q	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q

*Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

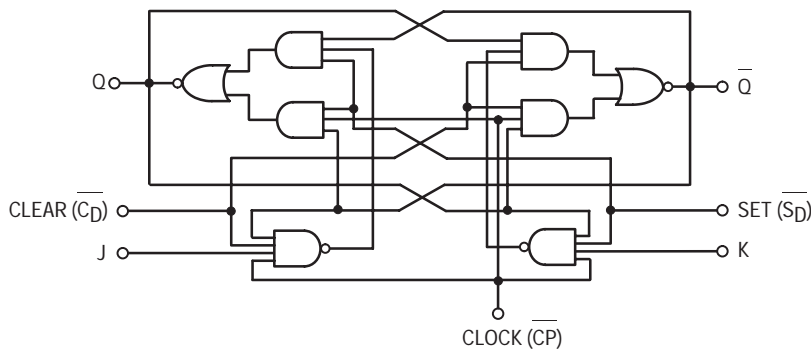
H,h = HIGH Voltage Level

L,l = LOW Voltage Level

X = Immaterial

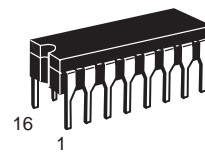
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the HIGH-to-LOW clock transition

LOGIC DIAGRAM

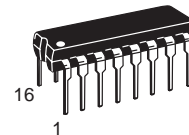


SN54/74LS76A

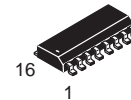
DUAL JK FLIP-FLOP WITH SET AND CLEAR
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

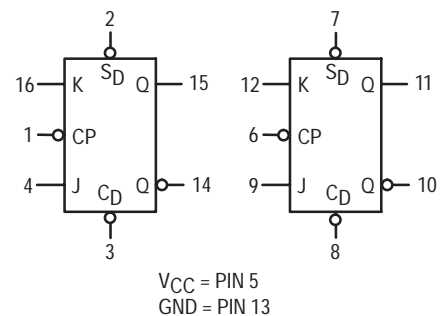


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

LOGIC SYMBOL



SN54/74LS76A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Clear, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Clock, Clear, Set to Output		15	20	ns	
			15	20	ns	

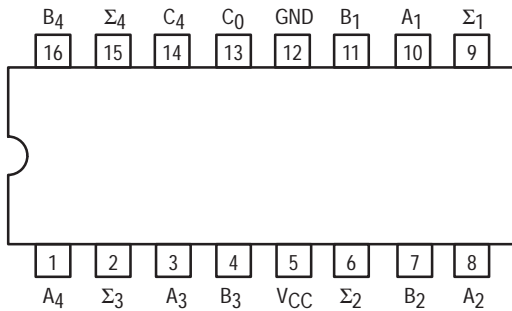
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	V _{CC} = 5.0 V
t _W	Clear Set Pulse Width	25			ns	
t _s	Setup Time	20			ns	
t _h	Hold Time	0			ns	

4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS83A is a high-speed 4-Bit binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4 , B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs $\Sigma_1-\Sigma_4$ and the Carry Output (C_4) from the most significant bit. The LS83A operates with either active HIGH or active LOW operands (positive or negative logic). The SN54/74LS283 is recommended for new designs since it is identical in function with this device and features standard corner power pins.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_1-A_4 Operand A Inputs
 B_1-B_4 Operand B Inputs
 C_0 Carry Input
 $\Sigma_1-\Sigma_4$ Sum Outputs (Note b)
 C_4 Carry Output (Note b)

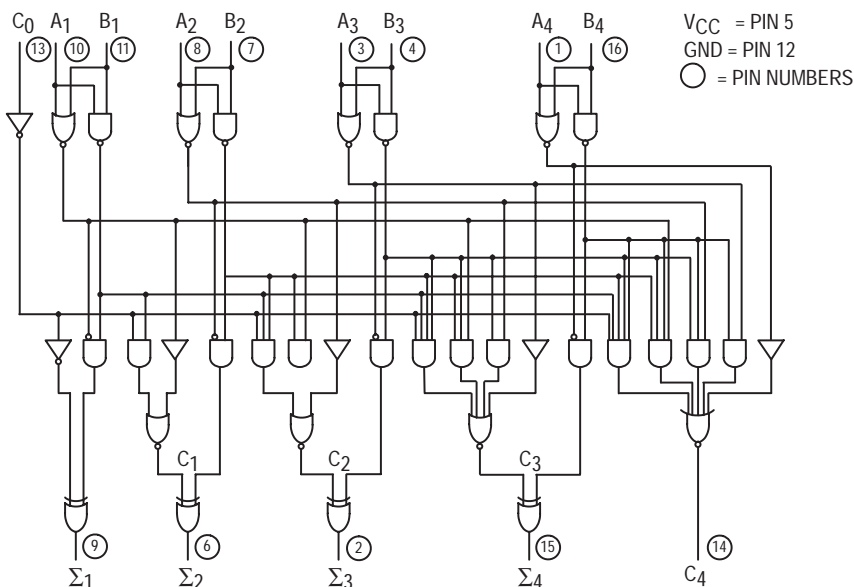
LOADING (Note a)

	HIGH	LOW
A_1-A_4	1.0 U.L.	0.5 U.L.
B_1-B_4	1.0 U.L.	0.5 U.L.
C_0	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	10 U.L.	5 (2.5) U.L.
C_4	10 U.L.	5 (2.5) U.L.

NOTES:

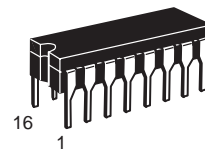
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

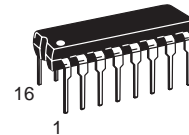


SN54/74LS83A

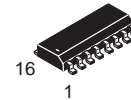
4-BIT BINARY FULL ADDER WITH FAST CARRY LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

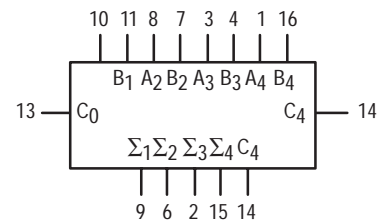


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ Ceramic
 SN74LSXXN Plastic
 SN74LSXXD SOIC

LOGIC SYMBOL



SN54/74LS83A

FUNCTIONAL DESCRIPTION

The LS83A adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$$C_0 + (A_1+B_1)+2(A_2+B_2)+4(A_3+B_3)+8(A_4+B_4) = \Sigma_1+2\Sigma_2+4\Sigma_3+8\Sigma_4+16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS83A can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH Inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C ₀	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C ₄
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10+9 = 19)
(carry+5+6 = 12)

Interchanging inputs of equal weight does not affect the operation, thus C₀, A₁, B₁, can be arbitrarily assigned to pins 10, 11, 13, etc.

FUNCTIONAL TRUTH TABLE

C (n-1)	A _n	B _n	Σ _n	C _n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C₁ — C₃ are generated internally
 C₀ — is an external input
 C₄ — is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS83A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ per Truth Table
		74	2.7	3.5	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
		74	0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current C_0 A or B			20 40	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
	C_0 A or B			0.1 0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current C_0 A or B			-0.4 -0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current All Inputs Grounded All Inputs at 4.5 V, Except B All Inputs at 4.5 V			39 34 34	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

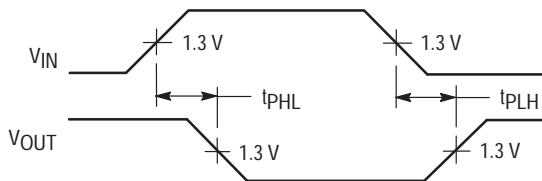


Figure 1

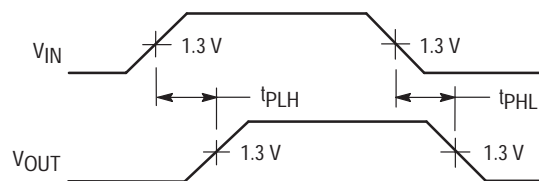


Figure 2



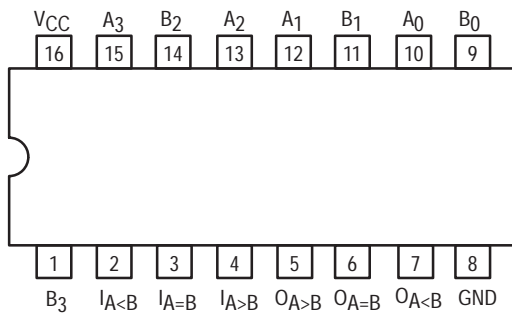
4-BIT MAGNITUDE COMPARATOR

The SN54/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}, I_{A<B}, I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B}=I_{A>B}=L, I_{A=B}=H$. For serial (ripple) expansion, the $O_{A>B}, O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}, I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}, O_{A<B}$, and $O_{A=B}$ Outputs Available

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0-A_3, B_0-B_3	Parallel Inputs
$I_{A=B}$	A = B Expander Inputs
$I_{A<B}, I_{A>B}$	A < B, A > B, Expander Inputs
$O_{A>B}$	A Greater Than B Output (Note b)
$O_{A<B}$	B Greater Than A Output (Note b)
$O_{A=B}$	A Equal to B Output (Note b)

LOADING (Note a)

	HIGH	LOW
Parallel Inputs	1.5 U.L.	0.75 U.L.
A = B Expander Inputs	1.5 U.L.	0.75 U.L.
A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

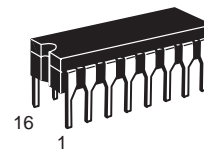
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

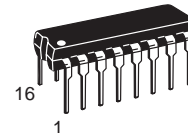
SN54/74LS85

4-BIT MAGNITUDE COMPARATOR

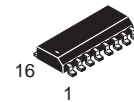
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

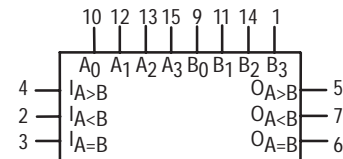


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

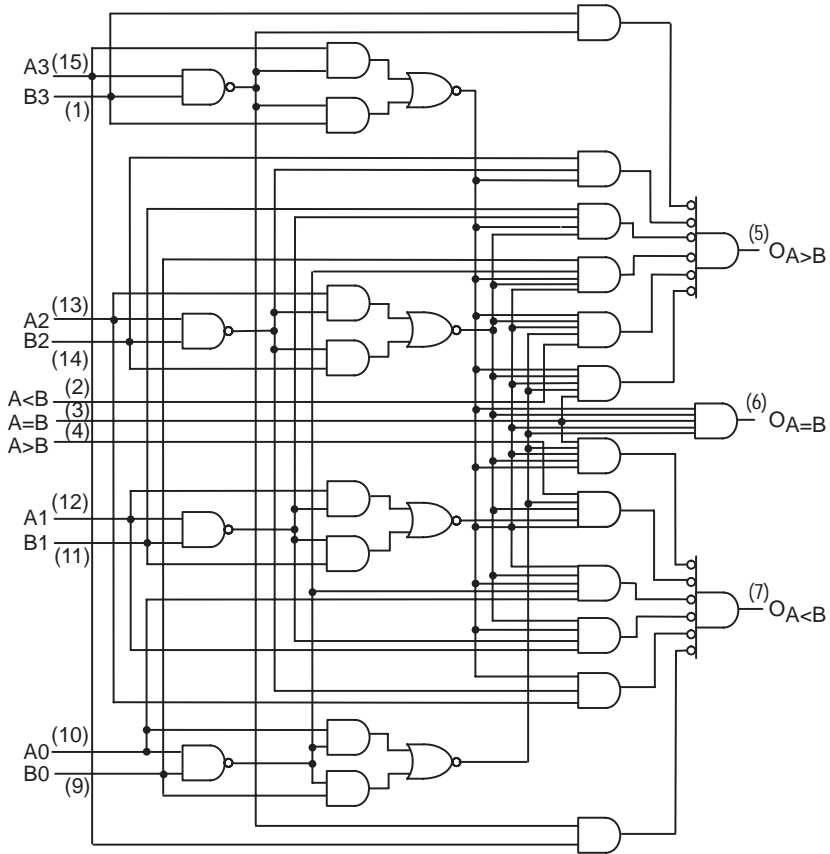
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS85

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A ₃ ,B ₃	A ₂ ,B ₂	A ₁ ,B ₁	A ₀ ,B ₀	I _{A>B}	I _{A<B}	I _{A=B}	O _{A>B}	O _{A<B}	O _{A=B}
A ₃ >B ₃	X	X	X	X	X	X	H	L	L
A ₃ <B ₃	X	X	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ >B ₂	X	X	X	X	X	H	L	L
A ₃ =B ₃	A ₂ <B ₂	X	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ >B ₁	X	X	X	X	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ <B ₁	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ >B ₀	X	X	X	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ <B ₀	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	H	L	L	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	L	H	L	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	X	X	H	L	L	H
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	H	H	L	L	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS85

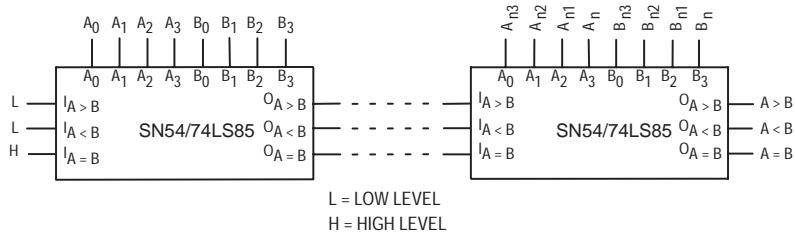


Figure 1. Comparing Two n-Bit Words

APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

WORD LENGTH	NUMBER OF PKGS.
1–4 Bits	1
5–24 Bits	2–6
25–120 Bits	8–31

NOTE:

The SN54/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A₀–A₃ and B₀–B₃ inputs of another SN54/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

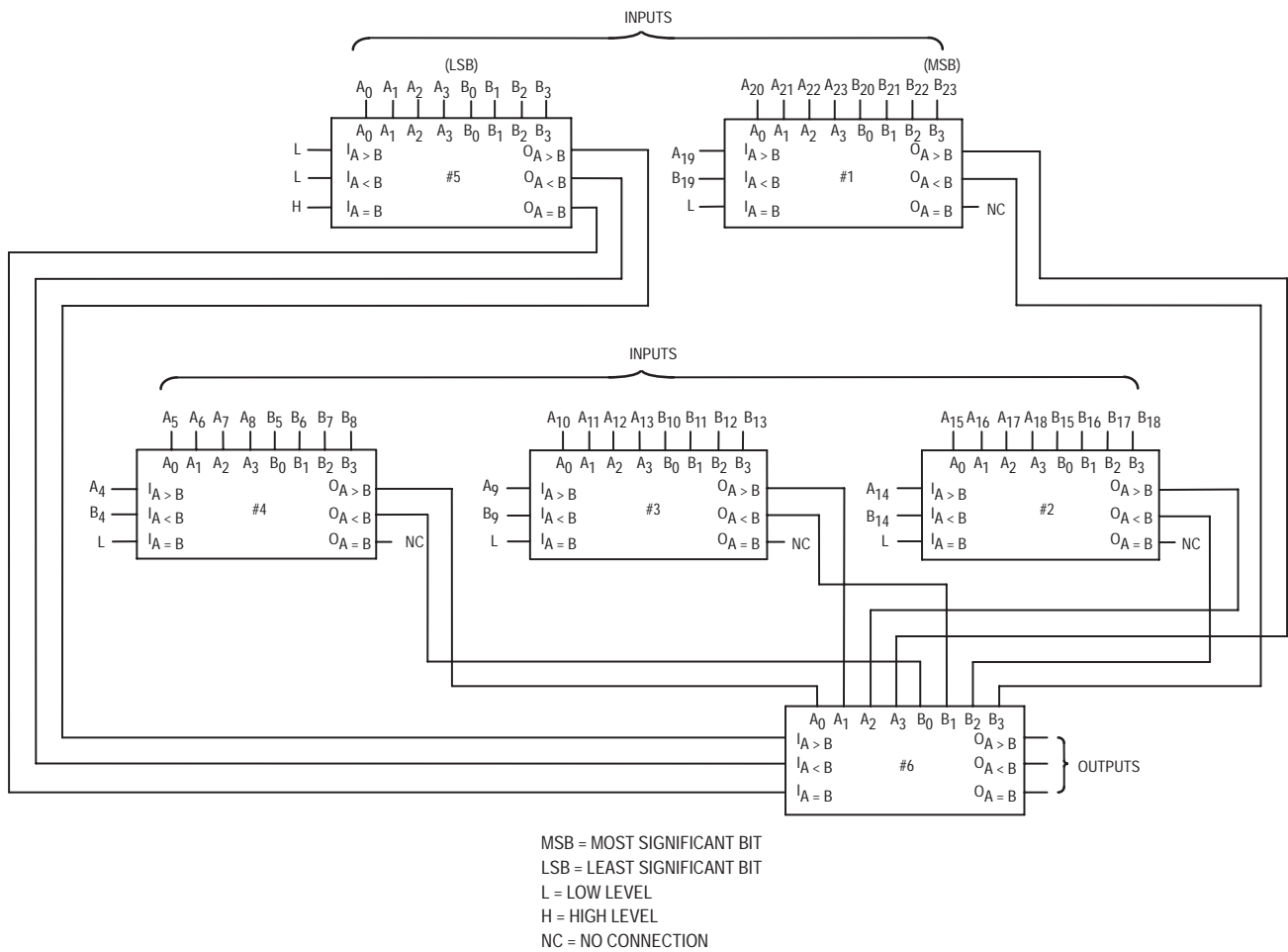


Figure 2. Comparison of Two 24-Bit Words

SN54/74LS85

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current A < B, A > B Other Inputs				20 60	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
	A < B, A > B Other Inputs				0.1 0.3	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current A < B, A > B Other Inputs				-0.4 -1.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Output Short Circuit Current (Note 1)	-20			-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current				20	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Any A or B to A < B, A > B		24 20	36 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Any A or B to A = B		27 23	45 45	ns	
t_{PLH} t_{PHL}	A < B or A = B to A > B		14 11	22 17	ns	
t_{PLH} t_{PHL}	A = B to A = B		13 13	20 26	ns	
t_{PLH} t_{PHL}	A > B or A = B to A < B		14 11	22 17	ns	

AC WAVEFORMS

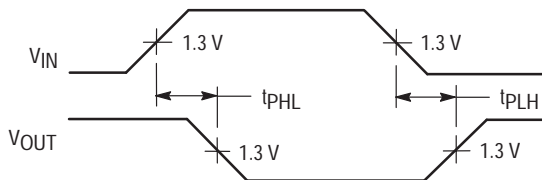


Figure 3

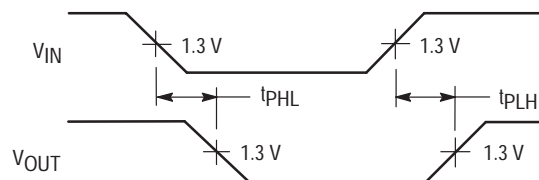
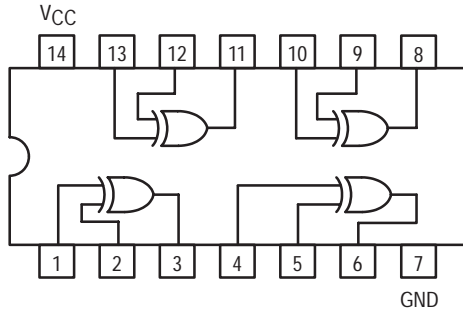


Figure 4



QUAD 2-INPUT EXCLUSIVE OR GATE

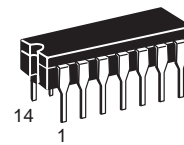


TRUTH TABLE

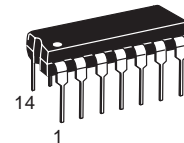
IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

SN54/74LS86

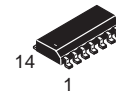
**QUAD 2-INPUT EXCLUSIVE OR GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS86

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			40	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		12 10	23 17	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		20 13	30 22	ns	



DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

CP ₀	Clock (Active LOW going edge) Input to +2 Section
CP ₁	Clock (Active LOW going edge) Input to +5 Section (LS90), +6 Section (LS92)
CP ₁	Clock (Active LOW going edge) Input to +8 Section (LS93)
MR ₁ , MR ₂	Master Reset (Clear) Inputs
MS ₁ , MS ₂	Master Set (Preset-9, LS90) Inputs
Q ₀	Output from +2 Section (Notes b & c)
Q ₁ , Q ₂ , Q ₃	Outputs from +5 (LS90), +6 (LS92), +8 (LS93) Sections (Note b)

LOADING (Note a)

	HIGH	LOW
CP ₀	0.5 U.L.	1.5 U.L.
CP ₁	0.5 U.L.	2.0 U.L.
CP ₁	0.5 U.L.	1.0 U.L.
MR ₁ , MR ₂	0.5 U.L.	0.25 U.L.
MS ₁ , MS ₂	0.5 U.L.	0.25 U.L.
Q ₀	10 U.L.	5 (2.5) U.L.
Q ₁ , Q ₂ , Q ₃	10 U.L.	5 (2.5) U.L.

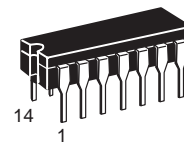
NOTES:

- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
- The Q₀ Outputs are guaranteed to drive the full fan-out plus the CP₁ input of the device.
- To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

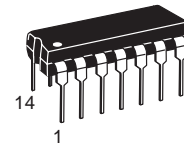
**SN54/74LS90
SN54/74LS92
SN54/74LS93**

**DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER**

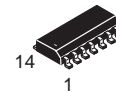
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**

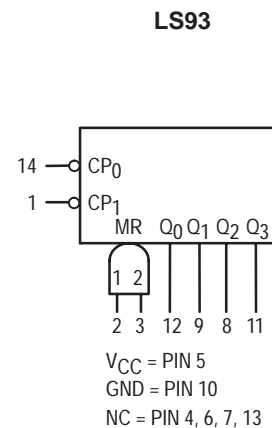
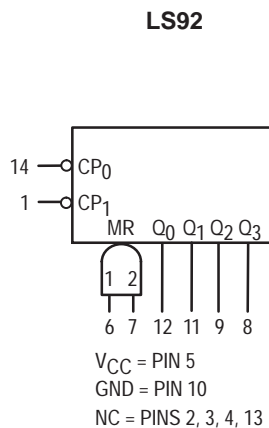
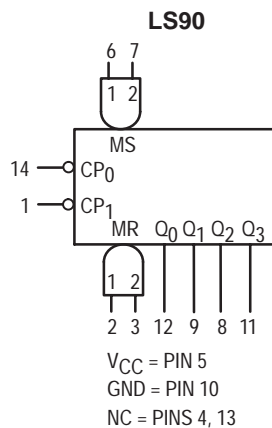


**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

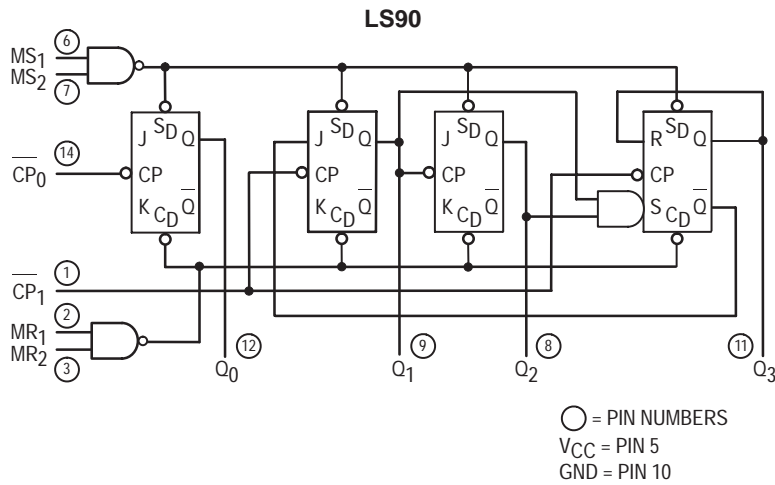
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC SYMBOL

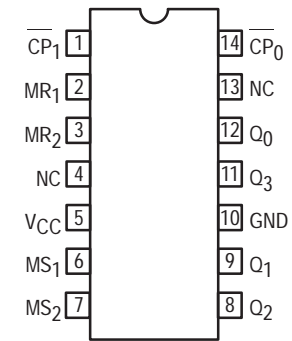


SN54/74LS90 • SN54/74LS92 • SN54/74LS93

LOGIC DIAGRAM



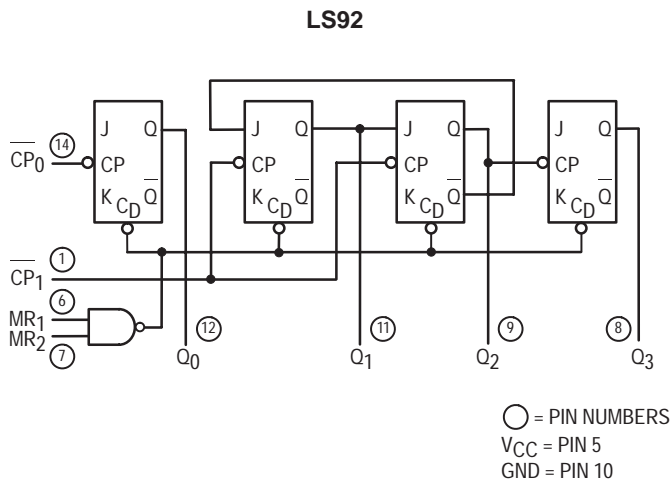
CONNECTION DIAGRAM DIP (TOP VIEW)



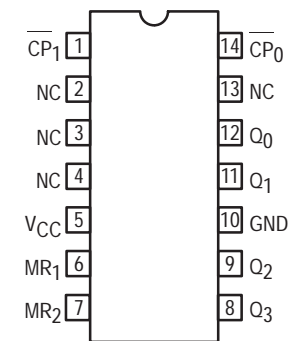
NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



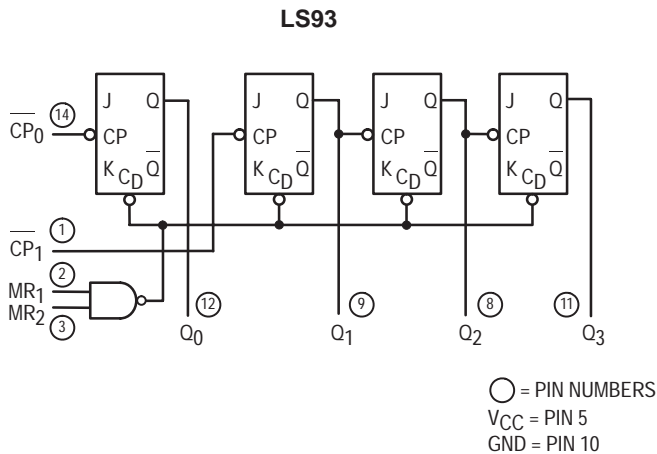
CONNECTION DIAGRAM DIP (TOP VIEW)



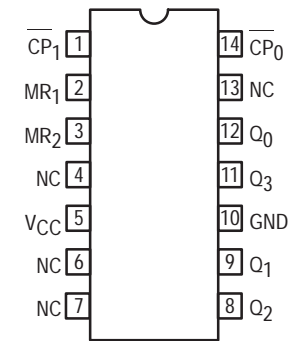
NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output of each device is designed and specified to drive the rated fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ • MR₂) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁ • MS₂) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

- A. BCD Decade (8421) Counter — The CP₁ input must be externally connected to the Q₀ output. The CP₀ input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q₃ output must be externally connected to the CP₀ input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at output Q₀.

- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP₀ as the input and Q₀ as the output). The CP₁ input is used to obtain binary divide-by-five operation at the Q₃ output.

LS92

- A. Modulo 12, Divide-By-Twelve Counter — The CP₁ input must be externally connected to the Q₀ output. The CP₀ input receives the incoming count and Q₃ produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The CP₁ input is used to obtain divide-by-three operation at the Q₁ and Q₂ outputs and divide-by-six operation at the Q₃ output.

LS93

- A. 4-Bit Ripple Counter — The output Q₀ must be externally connected to input CP₁. The input count pulses are applied to input CP₀. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q₀, Q₁, Q₂, and Q₃ outputs as shown in the truth table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input CP₁. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q₁, Q₂, and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

**LS90
MODE SELECTION**

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

**LS92 AND LS93
MODE SELECTION**

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

**LS90
BCD COUNT SEQUENCE**

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q₀ is connected to Input CP₁ for BCD count.

**LS92
TRUTH TABLE**

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q₀ is connected to Input CP₁.

**LS93
TRUTH TABLE**

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q₀ is connected to Input CP₁.

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current MS, MR CP ₀ CP ₁ (LS90, LS92) CP ₁ (LS93)			-0.4 -2.4 -3.2 -1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			15	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS90 • SN54/74LS92 • SN54/74LS93

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$)

Symbol	Parameter	Limits									Unit
		LS90			LS92			LS93			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	$\overline{\text{CP}}_0$ Input Clock Frequency	32			32			32			MHz
f_{MAX}	$\overline{\text{CP}}_1$ Input Clock Frequency	16			16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_3 Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_2 Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_3 Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		20	30							ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40							ns
t_{PHL}	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits						Unit
		LS90		LS92		LS93		
		Min	Max	Min	Max	Min	Max	
t_W	$\overline{\text{CP}}_0$ Pulse Width	15		15		15		ns
t_W	$\overline{\text{CP}}_1$ Pulse Width	30		30		30		ns
t_W	MS Pulse Width	15						ns
t_W	MR Pulse Width	15		15		15		ns
t_{rec}	Recovery Time MR to CP	25		25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

AC WAVEFORMS

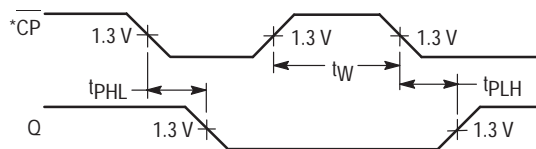


Figure 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

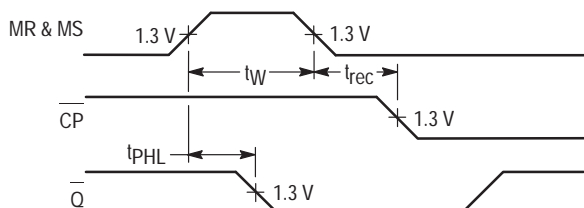


Figure 2

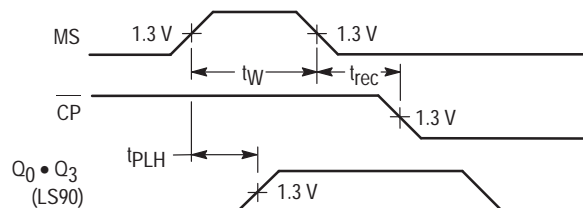


Figure 3



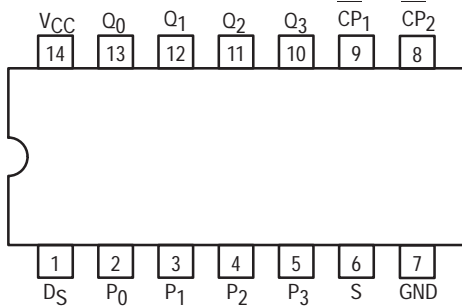
4-BIT SHIFT REGISTER

The SN54/74LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH to LOW transition of the appropriate clock input.

The LS95B is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Synchronous, Expandable Shift Right
- Synchronous Shift Left Capability
- Synchronous Parallel Load
- Separate Shift and Load Clock Inputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

V_{CC} = PIN 14
GND = PIN 7

PIN NAMES

S	Mode Control Input
D _S	Serial Data Input
P ₀ -P ₃	Parallel Data Inputs
CP ₁	Serial Clock (Active LOW Going Edge) Input
CP ₂	Parallel Clock (Active LOW Going Edge) Input
Q ₀ -Q ₃	Parallel Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
D _S	0.5 U.L.	0.25 U.L.
P ₀ -P ₃	0.5 U.L.	0.25 U.L.
CP ₁	0.5 U.L.	0.25 U.L.
CP ₂	0.5 U.L.	0.25 U.L.
Q ₀ -Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

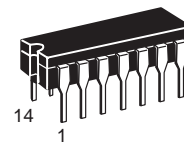
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

GUARANTEED OPERATING RANGES

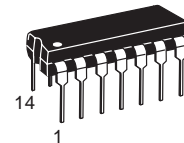
Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS95B

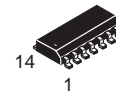
4-BIT SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



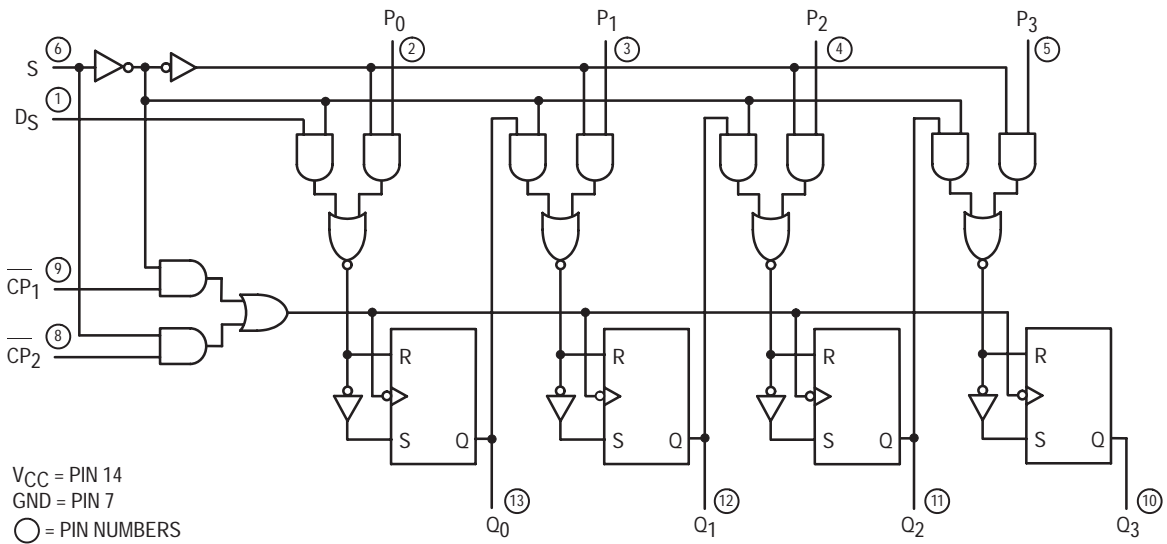
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

SN54/74LS95B

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS95B is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P_0 – P_3) Data inputs and four Parallel Data outputs (Q_0 – Q_3). The serial or parallel mode of operation is controlled by a Mode Control input (S) and two Clock Inputs (CP_1) and (CP_2). The serial (right-shift) or parallel data transfers occur synchronous with the HIGH to LOW transition of the selected clock input.

When the Mode Control input (S) is HIGH, CP_2 is enabled. A HIGH to LOW transition on enabled CP_2 transfers parallel data from the P_0 – P_3 inputs to the Q_0 – Q_3 outputs.

When the Mode Control input (S) is LOW, CP_1 is enabled. A

HIGH to LOW transition on enabled CP_1 transfers the data from Serial input (D_S) to Q_0 and shifts the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 respectively (right-shift). A left-shift is accomplished by externally connecting Q_3 to P_2 , Q_2 to P_1 , and Q_1 to P_0 , and operating the LS95B in the parallel mode ($S = \text{HIGH}$).

For normal operation, S should only change states when both Clock inputs are LOW. However, changing S from LOW to HIGH while CP_2 is HIGH, or changing S from HIGH to LOW while P_1 is HIGH and CP_2 is LOW will not cause any changes on the register outputs.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP ₁	CP ₂	D _S	P _n	Q ₀	Q ₁	Q ₂	Q ₃
Shift	L	⌋	X	l	X	L	q ₀	q ₁	q ₂
	L	⌋	X	h	X	H	q ₀	q ₁	q ₂
Parallel Load	H	X	⌋	X	P _n	P ₀	P ₁	P ₂	P ₃
Mode Change	⌋	L	L	X	X	No Change			
	⌋	L	L	X	X	No Change			
	⌋	H	L	X	X	No Change			
	⌋	H	L	X	X	Undetermined			
	⌋	L	H	X	X	Undetermined			
	⌋	L	H	X	X	No Change			
	⌋	H	H	X	X	Undetermined			
	⌋	H	H	X	X	No Change			

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW clock transition.

P_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS95B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input HIGH Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			21	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	36		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	CP to Output		18	27	ns	
			21	32	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	CP Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	Data Setup Time	20			ns	
t _H	Data Hold Time	20			ns	
t _S	Mode Control Setup Time	20			ns	
t _H	Mode Control Hold Time	20			ns	

SN54/74LS95B

DESCRIPTION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

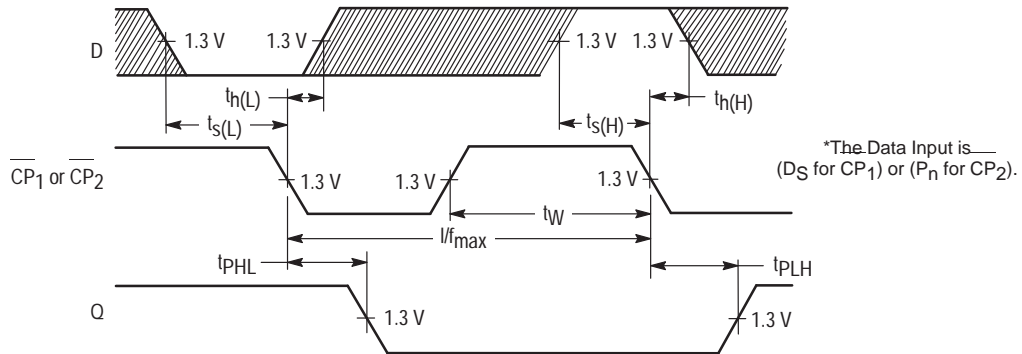


Figure 1

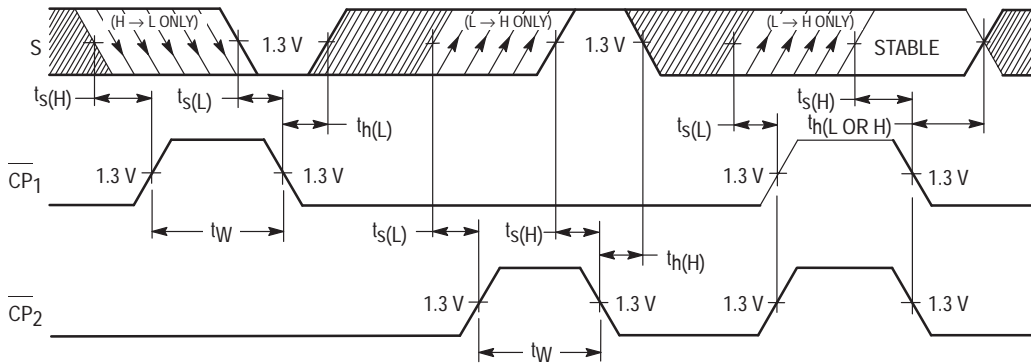


Figure 2

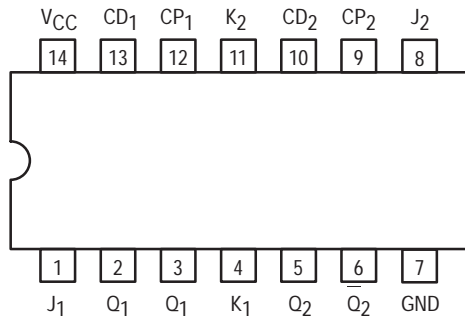


DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS107A is a Dual JK Flip-Flop with individual J, K, Direct Clear and Clock Pulse inputs. Output changes are initiated by the HIGH-to-LOW transition of the clock. A LOW signal on CD input overrides the other inputs and makes the Q output LOW.

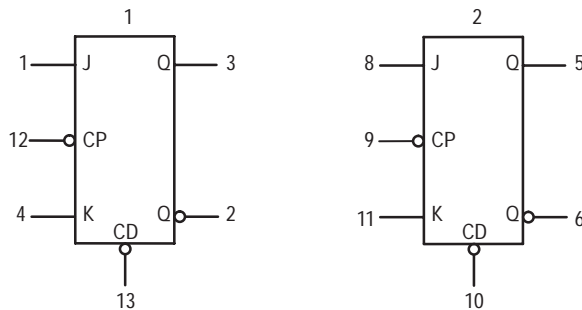
The SN54/74LS107A is the same as the SN54/74LS73A but has corner power pins.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

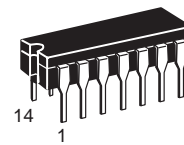
LOGIC SYMBOL



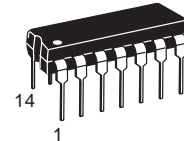
V_{CC} = PIN 14
GND = PIN 7

SN54/74LS107A

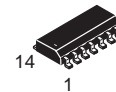
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS107A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		J, K Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	J, K Clear and Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
f _{MAX}	Maximum Clock Frequency		30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF	
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		15	20		ns		
			15	20		ns		

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

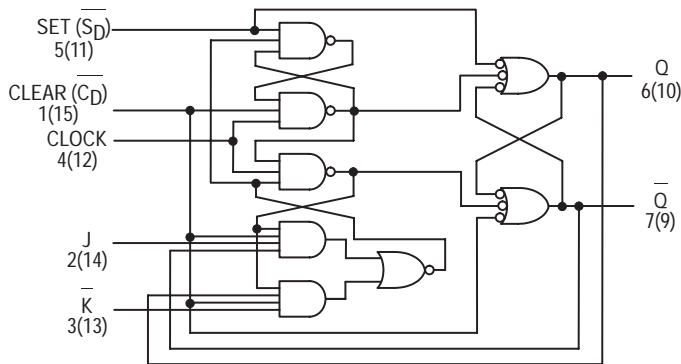
Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _W	Clock Pulse Width		20			ns	V _{CC} = 5.0 V	
t _W	Clear Pulse Width		25			ns		
t _s	Setup Time		20			ns		
t _h	Hold Time		0			ns		



DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS109A consists of two high speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by simply connecting the J and K pins together.

LOGIC DIAGRAM



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	S _D	C _D	J	K	Q	Q̄
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	L
Hold	H	H	l	h	q	q
Toggle	H	H	h	l	q	q
Load "0" (Reset)	H	H	l	l	L	H

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

H, h = HIGH Voltage Level

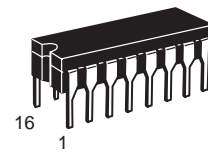
L, l = LOW Voltage Level

X = Don't Care

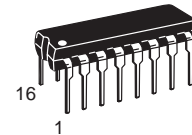
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

SN54/74LS109A

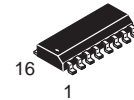
DUAL JK POSITIVE
EDGE-TRIGGERED FLIP-FLOP
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

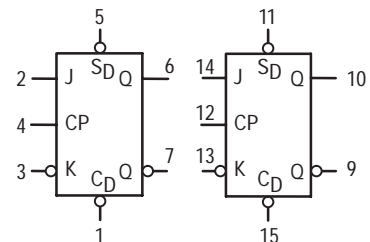


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS109A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current J, K, Clock Set, Clear			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	J, K, Clock Set, Clear			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current J, K, Clock Set, Clear			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			8.0	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	33		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Clock, Clear, Set to Output		13	25	ns	
t _{PHL}			25	40	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

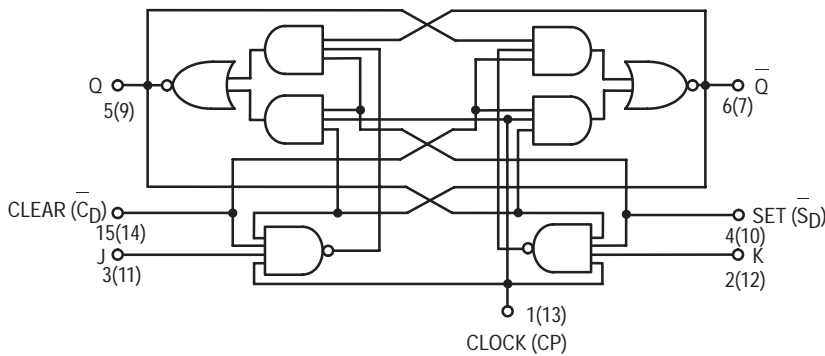
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock High Clear, Set Pulse Width	25			ns	V _{CC} = 5.0 V
t _s	Data Setup Time — HIGH LOW	20			ns	
		20			ns	
t _h	Hold time	5.0			ns	



DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS112A dual JK flip-flop features individual J, K, clock, and asynchronous set and clear inputs to each flip-flop. When the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up and hold time are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	S _D	C _D	J	K	Q	Q̄
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	q	q
Toggle	H	H	h	h	q	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

H, h = HIGH Voltage Level

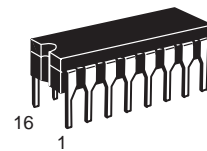
L, l = LOW Voltage Level

X = Don't Care

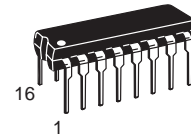
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS112A

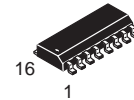
DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

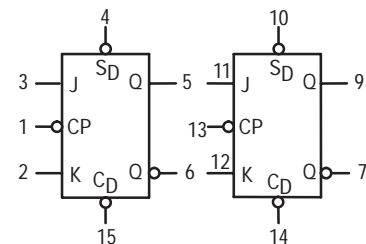


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS112A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	J, K Set, Clear Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		J, K Set, Clear Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Clear, Set, Clk			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Propagation Delay, Clock		15	20	ns	
t _{PHL}	Propagation Delay, Clear, Set to Output		15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

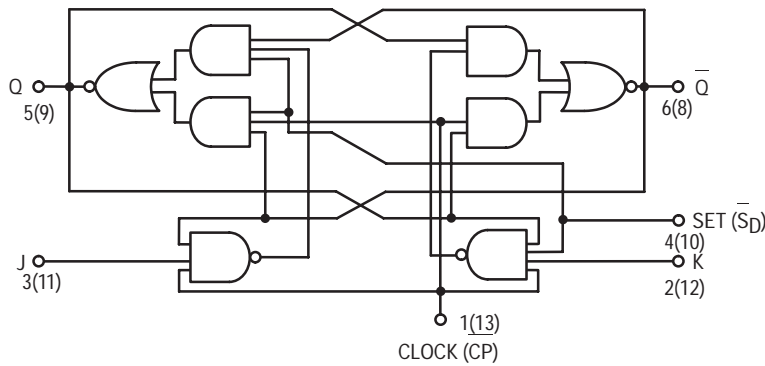
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	V _{CC} = 5.0 V
t _W	Clear, Set Pulse Width	25			ns	
t _S	Setup Time	20			ns	
t _H	Hold Time	0			ns	



DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	S _D	J	K	Q	Q̄
Set	L	X	X	H	L
Toggle	H	h	h	q	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	q

H, h = HIGH Voltage Level

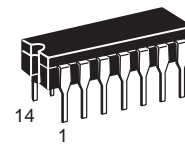
L, l = LOW Voltage Level

X = Don't Care

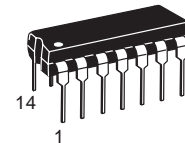
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

SN54/74LS113A

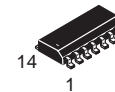
**DUAL JK NEGATIVE
EDGE-TRIGGERED FLIP-FLOP**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

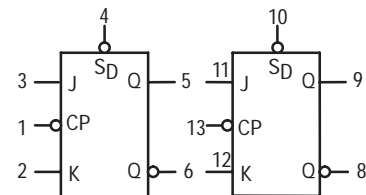


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

SN54/74LS113A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	J, K Set Clock			20 60 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		J, K Set Clock			0.1 0.3 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Set, Clock			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH}	Propagation Delay, Clock Set to Output		15	20	ns	
t _{PHL}			15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

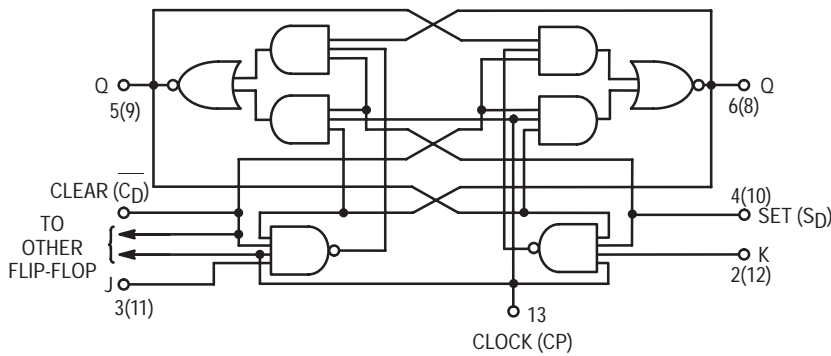
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width High	20			ns	V _{CC} = 5.0 V
t _W	Set Pulse Width	25			ns	
t _s	Setup Time	20			ns	
t _h	Hold Time	0			ns	



DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS114A offers common clock and common clear inputs and individual J, K, and set inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	S _D	C _D	J	K	Q	Q̄
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
*Undetermined	L	L	X	X	H	H
Toggle	H	H	h	h	q	q̄
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	l	l	q	q̄

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously.

H, h = HIGH Voltage Level

L, l = LOW Voltage Level

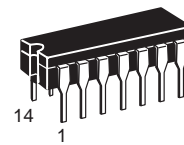
X = Don't Care

l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

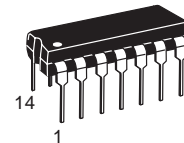
SN54/74LS114A

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

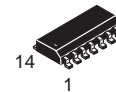
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

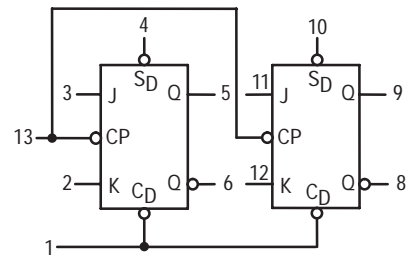


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

SN54/74LS114A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current	J, K Set Clear Clock			20 60 120 160	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		J, K Set Clear Clock			0.1 0.3 0.6 0.8	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	J, K Set Clear, Clock			-0.4 -0.8 -1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				6.0	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency		30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Clock, Clear, Set to Output			15	20	ns	
				15	20	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _W	Clock Pulse Width High		20			ns	V _{CC} = 5.0 V
t _W	Clear, Set Pulse Width		25			ns	
t _s	Setup Time		20			ns	
t _h	Hold Time		0			ns	

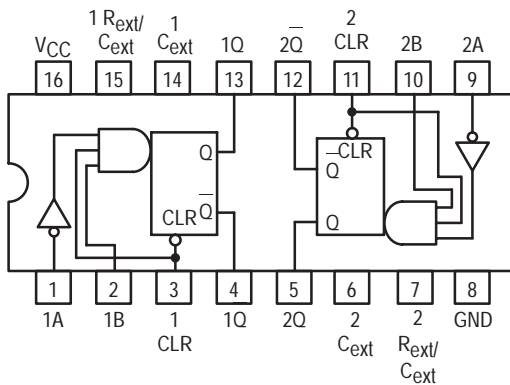


RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

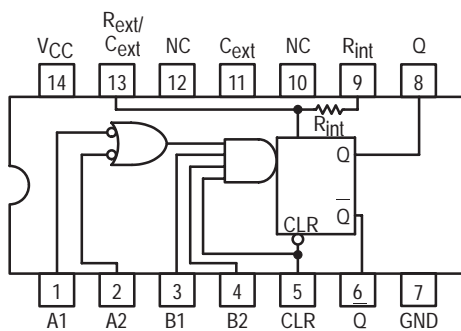
These dc triggered multivibrators feature pulse width control by three methods. The basic pulse width is programmed by selection of external resistance and capacitance values. The LS122 has an internal timing resistor that allows the circuits to be used with only an external capacitor. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear.

- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- DC Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle
- Internal Timing Resistors on LS122

SN54/74LS123 (TOP VIEW)
(SEE NOTES 1 THRU 4)



SN54/74LS122 (TOP VIEW)
(SEE NOTES 1 THRU 4)



NC — NO INTERNAL CONNECTION.

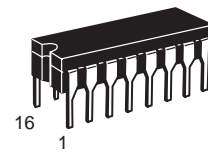
NOTES:

1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of the LS122, connect R_{int} to V_{CC} .
3. For improved pulse width accuracy connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int}/C_{ext} and V_{CC} .

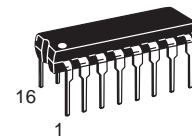
SN54/74LS122 SN54/74LS123

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

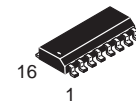
LOW POWER SCHOTTKY



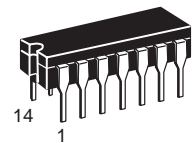
J SUFFIX
CERAMIC
CASE 620-09



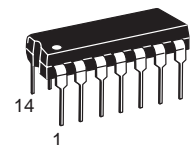
N SUFFIX
PLASTIC
CASE 648-08



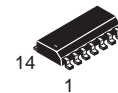
D SUFFIX
SOIC
CASE 751B-03



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS122 • SN54/74LS123

LS122
FUNCTIONAL TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H		
H	L	X	H	↑		
H	X	L	↑	H		
H	X	L	H	↑		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
↑	L	X	H	H		
↑	X	L	H	H		

LS123
FUNCTIONAL TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

TYPICAL APPLICATION DATA

The output pulse t_W is a function of the external components, C_{ext} and R_{ext} or C_{ext} and R_{int} on the LS122. For values of $C_{ext} \geq 1000$ pF, the output pulse at $V_{CC} = 5.0$ V and $V_{RC} = 5.0$ V (see Figures 1, 2, and 3) is given by

$$t_W = K R_{ext} C_{ext} \text{ where } K \text{ is nominally } 0.45$$

If C_{ext} is in pF and R_{ext} is in $k\Omega$ then t_W is in nanoseconds.

The C_{ext} terminal of the LS122 and LS123 is an internal connection to ground, however for the best system performance C_{ext} should be hard-wired to ground.

Care should be taken to keep R_{ext} and C_{ext} as close to the monostable as possible with a minimum amount of inductance between the R_{ext}/C_{ext} junction and the R_{ext}/C_{ext} pin. Good groundplane and adequate bypassing should be designed into the system for optimum performance to insure that no false triggering occurs.

It should be noted that the C_{ext} pin is internally connected to ground on the LS122 and LS123, but not on the LS221. Therefore, if C_{ext} is hard-wired externally to ground, substitution of a LS221 onto a LS123 socket will cause the LS221 to become non-functional.

The switching diode is not needed for electrolytic capacitance application and should not be used on the LS122 and LS123.

To find the value of K for $C_{ext} \geq 1000$ pF, refer to Figure 4. Variations on V_{CC} or V_{RC} can cause the value of K to change, as can the temperature of the LS123, LS122. Figures 5 and 6 show the behavior of the circuit shown in Figures 1 and 2 if

separate power supplies are used for V_{CC} and V_{RC} . If V_{CC} is tied to V_{RC} , Figure 7 shows how K will vary with V_{CC} and temperature. Remember, the changes in R_{ext} and C_{ext} with temperature are not calculated and included in the graph.

As long as $C_{ext} \geq 1000$ pF and $5K \leq R_{ext} \leq 260K$ (SN74LS122/123) or $5K \leq R_{ext} \leq 160K$ (SN54LS122/123), the change in K with respect to R_{ext} is negligible.

If $C_{ext} \leq 1000$ pF the graph shown on Figure 8 can be used to determine the output pulse width. Figure 9 shows how K will change for $C_{ext} \leq 1000$ pF if V_{CC} and V_{RC} are connected to the same power supply. The pulse width t_W in nanoseconds is approximated by

$$t_W = 6 + 0.05 C_{ext} (\text{pF}) + 0.45 R_{ext} (k\Omega) C_{ext} + 11.6 R_{ext}$$

In order to trim the output pulse width, it is necessary to include a variable resistor between V_{CC} and the R_{ext}/C_{ext} pin or between V_{CC} and the R_{ext} pin of the LS122. Figure 10, 11, and 12 show how this can be done. R_{ext} remote should be kept as close to the monostable as possible.

Retriggering of the part, as shown in Figure 3, must not occur before C_{ext} is discharged or the retrigger pulse will not have any effect. The discharge time of C_{ext} in nanoseconds is guaranteed to be less than $0.22 C_{ext}$ (pF) and is typically $0.05 C_{ext}$ (pF).

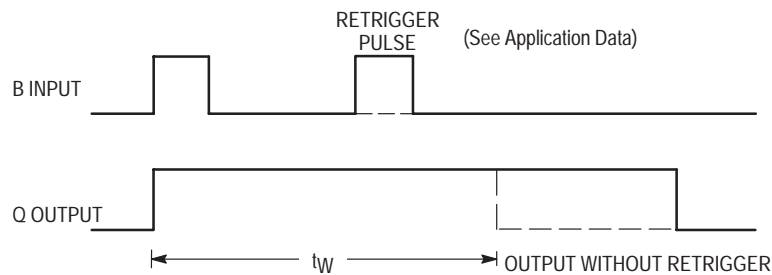
For the smallest possible deviation in output pulse widths from various devices, it is suggested that C_{ext} be kept ≥ 1000 pF.

SN54/74LS122 • SN54/74LS123

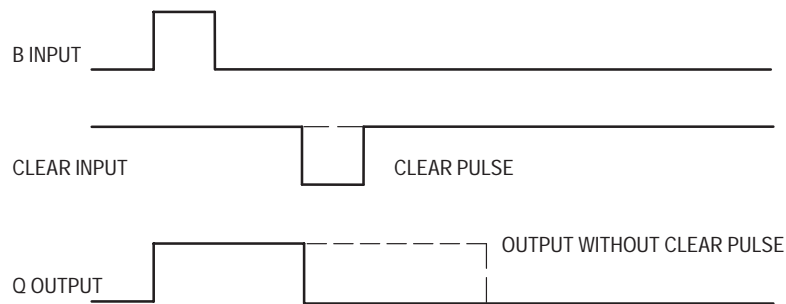
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA
R _{ext}	External Timing Resistance	54 74	5.0 5.0		180 260	kΩ
C _{ext}	External Capacitance	54, 74	No Restriction			
R _{ext} /C _{ext}	Wiring Capacitance at R _{ext} /C _{ext} Terminal	54, 74			50	pF

WAVEFORMS



EXTENDING PULSE WIDTH



OVERRIDING THE OUTPUT PULSE

SN54/74LS122 • SN54/74LS123

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current	LS122			11	mA	V _{CC} = MAX
		LS123			20		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, A to Q Propagation Delay, A to Q			23 32	33 45	ns	C _{ext} = 0 C _L = 15 pF R _{ext} = 5.0 kΩ R _L = 2.0 kΩ
t _{PLH} t _{PHL}	Propagation Delay, B to Q Propagation Delay, B to Q			23 34	44 56		
t _{PLH} t _{PHL}	Propagation Delay, Clear to Q Propagation Delay, Clear to Q			28 20	45 27	ns	
t _{W min}	A or B to Q			116	200		
t _{WQ}	A to B to Q		4.0	4.5	5.0	μs	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _W	Pulse Width		40			ns	

SN54/74LS122 • SN54/74LS123

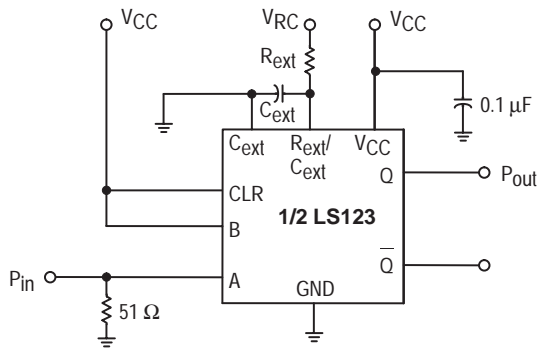


Figure 1

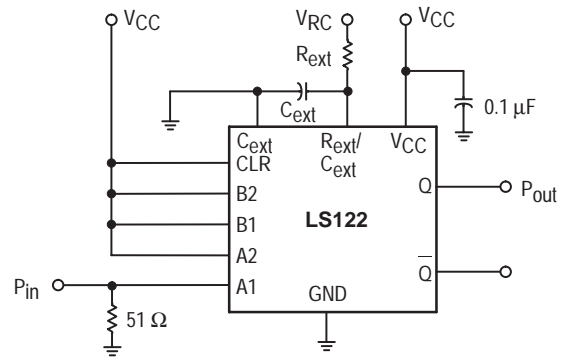


Figure 2

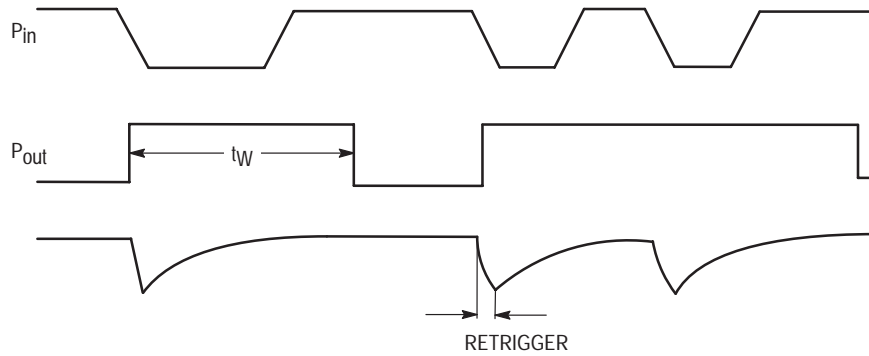


Figure 3

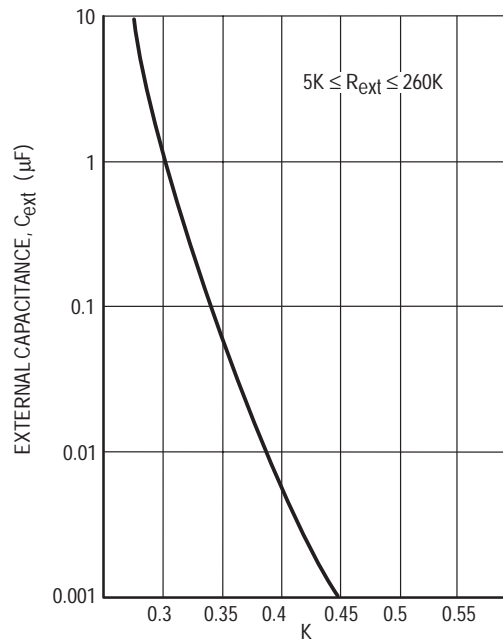


Figure 4

SN54/74LS122 • SN54/74LS123

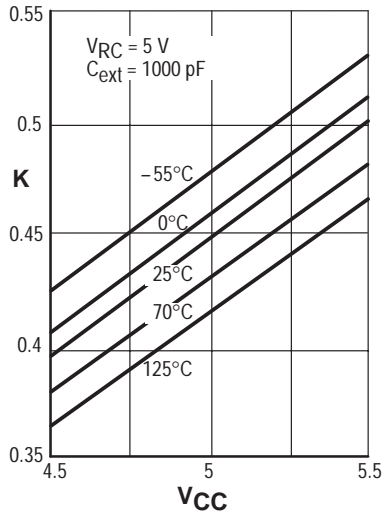


Figure 5. K versus V_{CC}

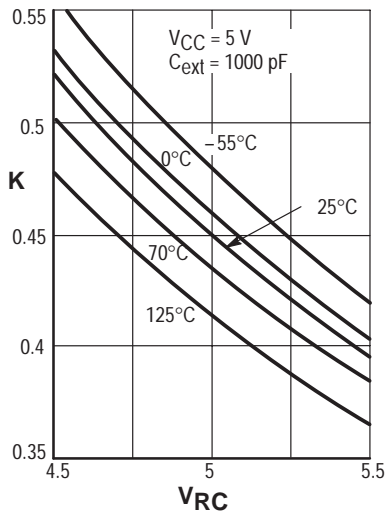


Figure 6. K versus V_{RC}

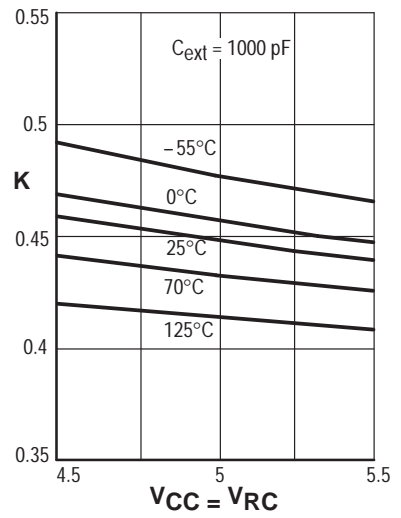


Figure 7. K versus V_{CC} and V_{RC}

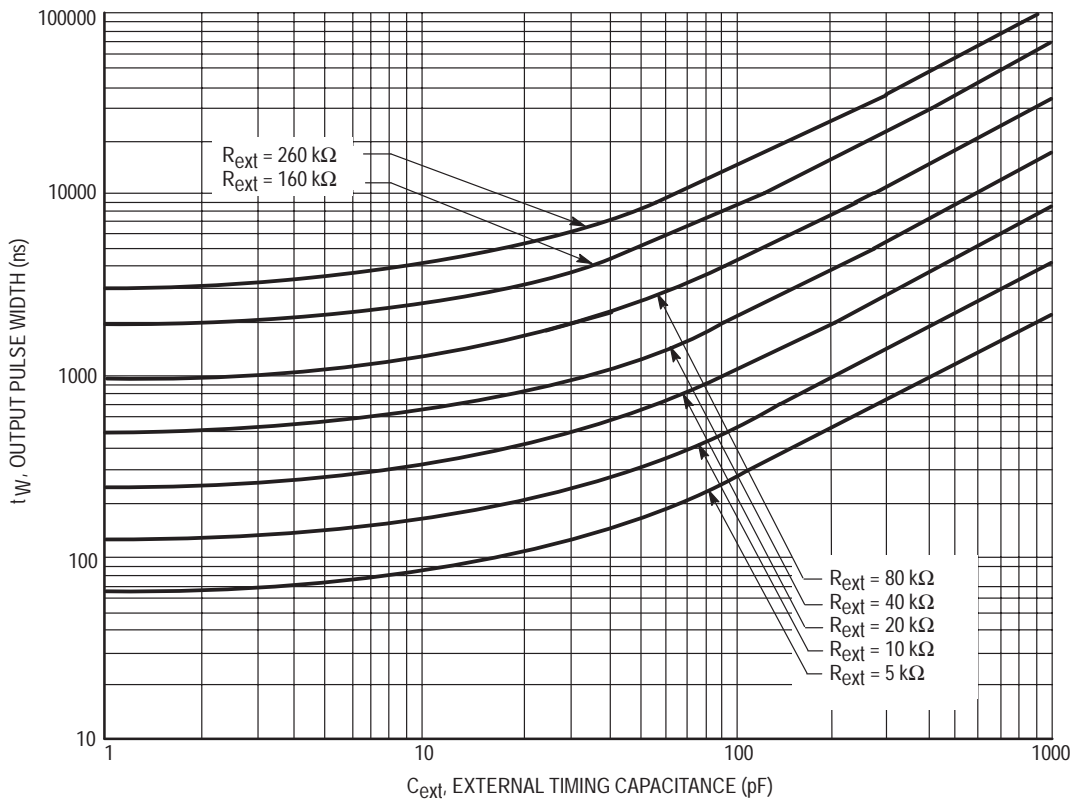


Figure 8

SN54/74LS122 • SN54/74LS123

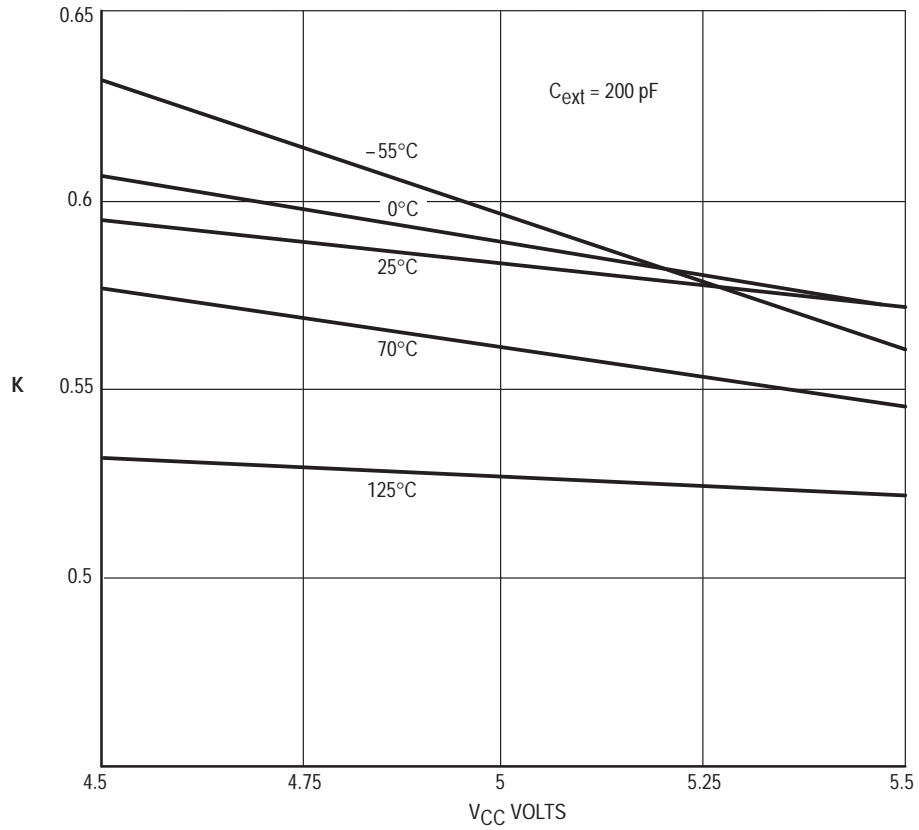


Figure 9

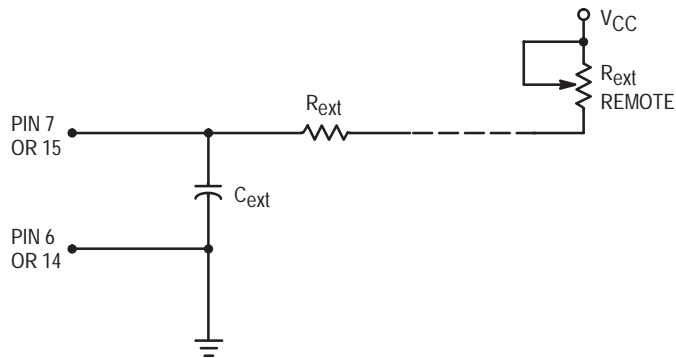


Figure 10. LS123 Remote Trimming Circuit

SN54/74LS122 • SN54/74LS123

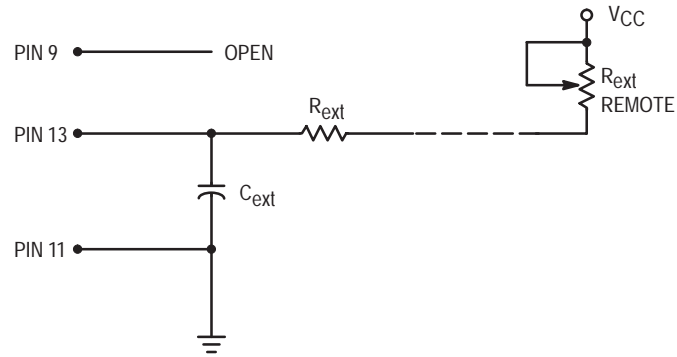


Figure 11. LS122 Remote Trimming Circuit Without R_{ext}

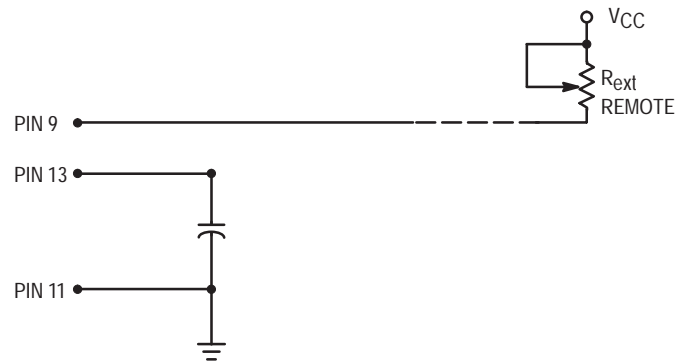
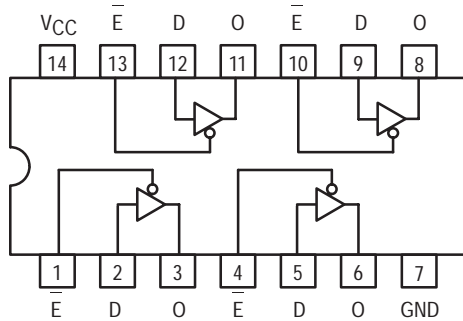


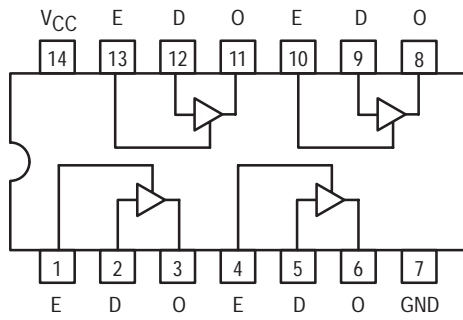
Figure 12. LS122 Remote Trimming Circuit with R_{int}



QUAD 3-STATE BUFFERS



LS125A



LS126A

TRUTH TABLES

LS125A

INPUTS		OUTPUT
E	D	
L	L	L
L	H	H
H	X	(Z)

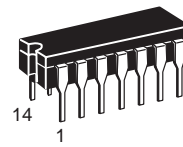
LS126A

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

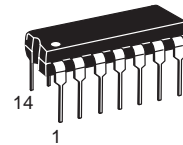
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

SN54/74LS125A SN54/74LS126A

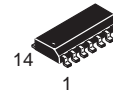
QUAD 3-STATE BUFFERS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS125A • SN54/74LS126A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4			V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4			V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.4 V	
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-40		-225	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current	LS125A			20	mA	V _{CC} = MAX	V _{IN} = 0 V, V _E = 4.5 V
		LS126A			22			V _{IN} = 0 V, V _E = 0 V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	Propagation Delay, Data to Output	LS125A		9.0	15	ns	Figure 2	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH}		LS126A		9.0	15			
t _{PHL}		LS125A		7.0	18			
t _{PHL}		LS126A		8.0	18			
t _{PZH}	Output Enable Time to HIGH Level	LS125A		12	20	ns	Figures 4, 5	
		LS126A		16	25			
t _{PZL}	Output Enable Time to LOW Level	LS125A		15	25	ns	Figures 3, 5	
		LS126A		21	35			
t _{PHZ}	Output Disable Time from HIGH Level	LS125A			20	ns	Figures 4, 5	
		LS126A			25			
t _{PLZ}	Output Disable Time from LOW Level	LS125A			20	ns	Figures 3, 5	
		LS126A			25			

SN54/74LS125A • SN54/74LS126A

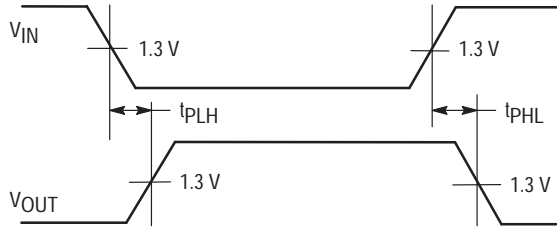


Figure 1

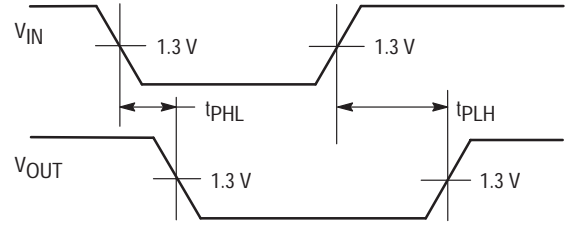


Figure 2

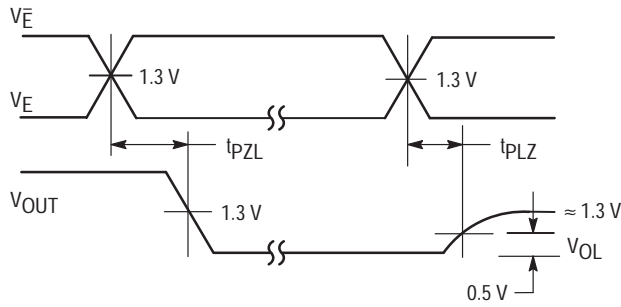


Figure 3

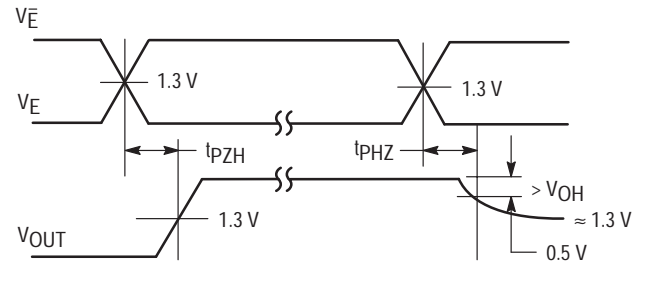


Figure 4

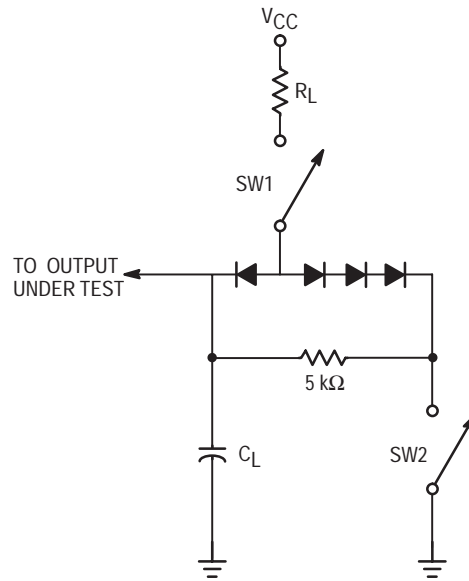


Figure 5

SWITCH POSITIONS

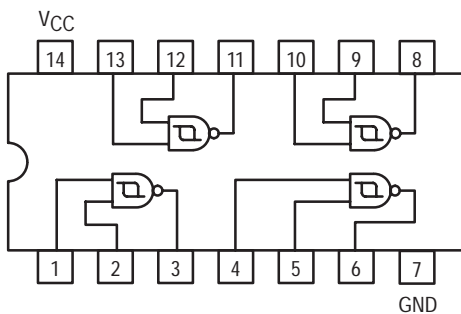
SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

The SN54/74LS132 contains four 2-Input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

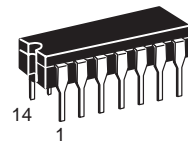
Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+} (MAX), the gate will respond to the transitions of the other input as shown in Figure 1.

LOGIC AND CONNECTION DIAGRAM DIP (TOP VIEW)

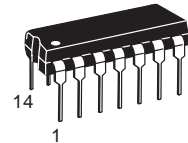


SN54/74LS132

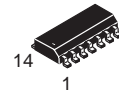
**QUAD 2-INPUT
SCHMITT TRIGGER NAND GATE**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

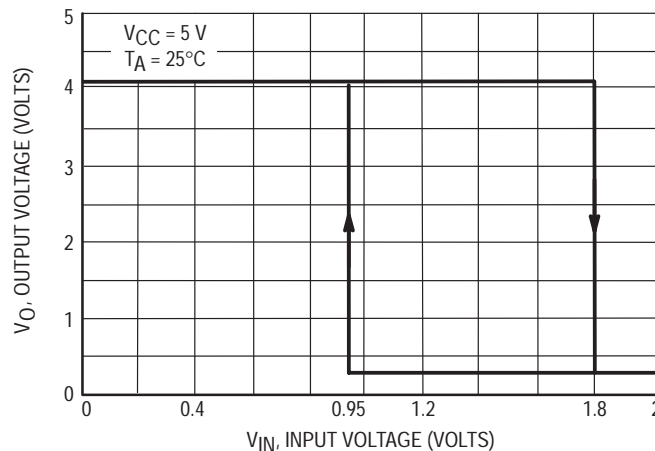


Figure 1. V_{IN} versus V_{OUT} Transfer Function

SN54/74LS132

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{T+}	Positive-Going Threshold Voltage	1.5		2.0	V	V _{CC} = 5.0 V	
V _{T-}	Negative-Going Threshold Voltage	0.6		1.1	V	V _{CC} = 5.0 V	
V _{T+} - V _{T-}	Hysteresis	0.4	0.8		V	V _{CC} = 5.0 V	
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.4	V	V _{CC} = MIN, I _{OH} = -400 μA, V _{IN} = V _{IL}	
		74	2.7	3.4			
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V _{CC} = MIN, I _{OL} = 4.0 mA, V _{IN} = 2.0 V
		74		0.35	0.5	V	V _{CC} = MIN, I _{OL} = 8.0 mA, V _{IN} = 2.0 V
I _{T+}	Input Current at Positive-Going Threshold		-0.14		mA	V _{CC} = 5.0 V, V _{IN} = V _{T+}	
I _{T-}	Input Current at Negative-Going Threshold		-0.18		mA	V _{CC} = 5.0 V, V _{IN} = V _{T-}	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX, V _{OUT} = 0 V	
I _{CC}	Power Supply Current Total, Output HIGH		5.9	11	mA	V _{CC} = MAX, V _{IN} = 0 V	
	Total, Output LOW		8.2	14	mA	V _{CC} = MAX, V _{IN} = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output			22	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output			22	ns	

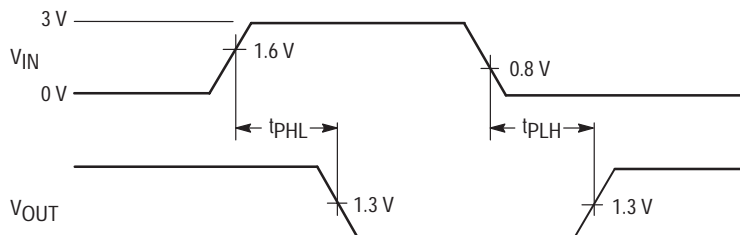


Figure 2. AC Waveforms

SN54/74LS132

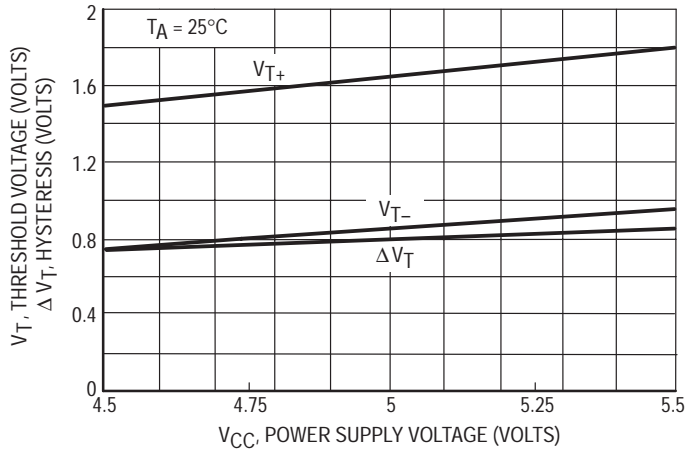


Figure 3. Threshold Voltage and Hysteresis versus Power Supply Voltage

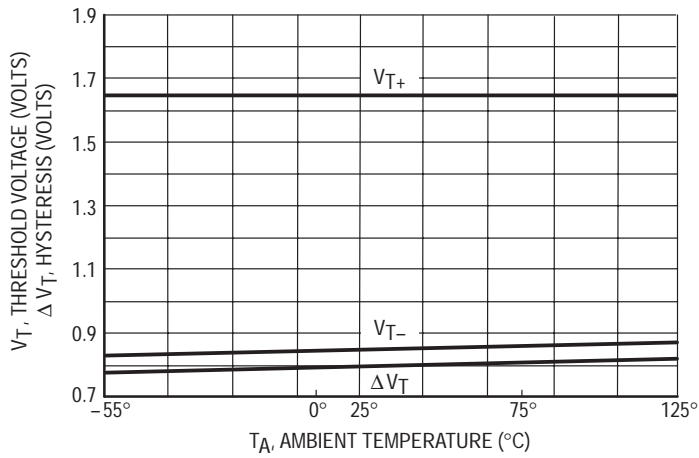
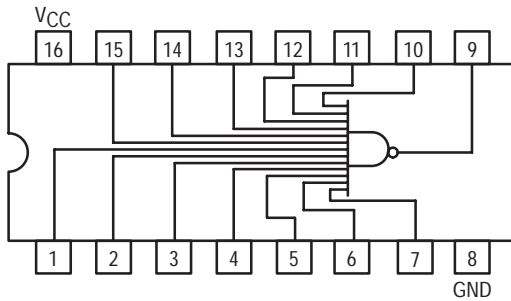


Figure 4. Threshold Voltage and Hysteresis versus Temperature



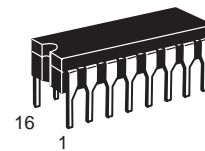
MOTOROLA

13-INPUT NAND GATE

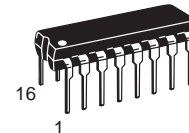


SN54/74LS133

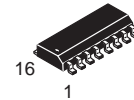
**13-INPUT NAND GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**



**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS133

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			0.5	mA	V _{CC} = MAX	
				1.1			

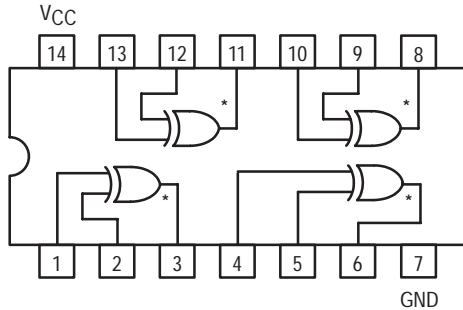
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Input to Output		10	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Turn-On Delay, Input to Output		40	59	ns	



QUAD 2-INPUT EXCLUSIVE OR GATE



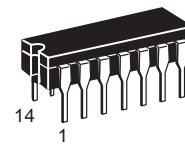
* OPEN COLLECTOR OUTPUTS

TRUTH TABLE

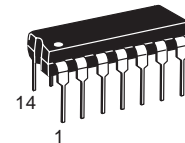
IN		OUT
A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

SN74LS136

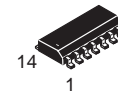
QUAD 2-INPUT
EXCLUSIVE OR GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
V _{OH}	Output Voltage — High			5.5	V
I _{OL}	Output Current — Low			8.0	mA

SN74LS136

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

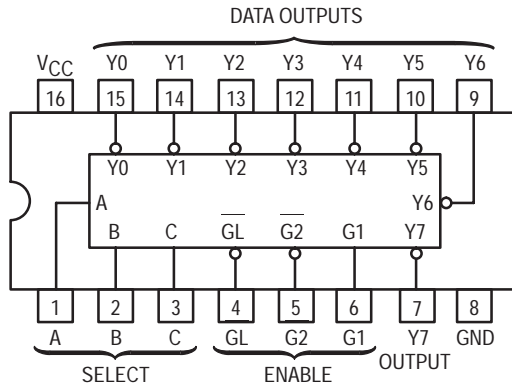
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
I_{OH}	Output HIGH Current			100	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			40	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Other Input LOW		18 18	30 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$, $R_L = 2.0 \text{ k}\Omega$
t_{PLH} t_{PHL}	Propagation Delay, Other Input HIGH		18 18	30 30	ns	



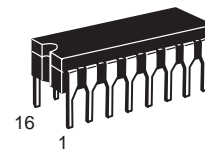
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



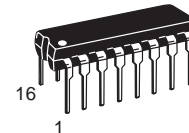
SN54/74LS137

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

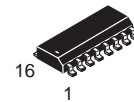
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

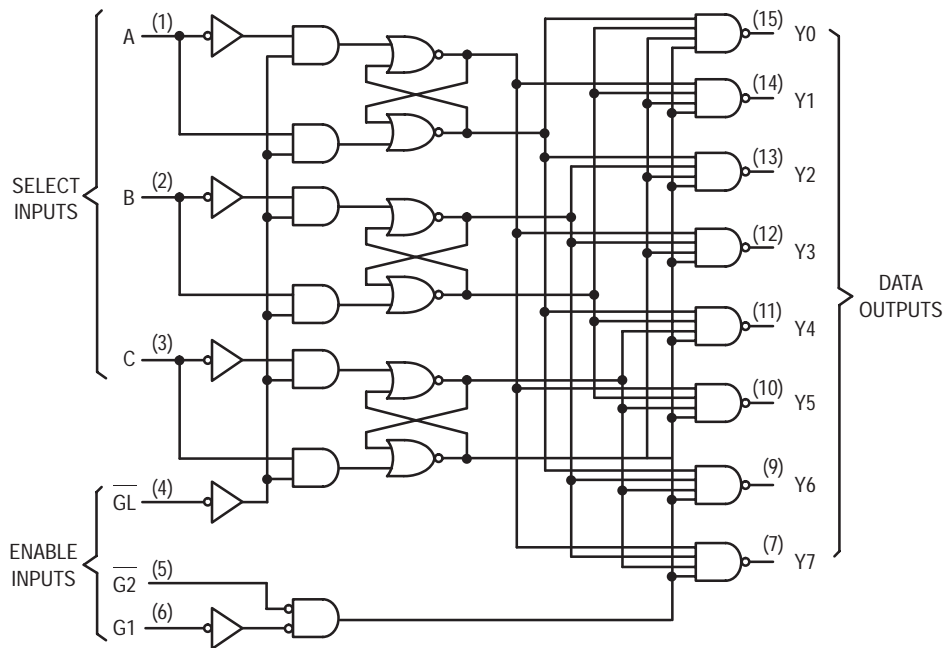
Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS137

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	L	H	L	L	H	H	H	H	H
L	H	L	L	L	L	H	L	L	L	H	H	H	H
L	H	L	L	L	L	H	L	L	L	L	H	H	H
L	H	L	L	L	L	H	L	L	L	L	L	H	H
L	H	L	L	L	L	H	L	L	L	L	L	L	H
L	H	L	L	L	L	H	L	L	L	L	L	L	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant



SN54/74LS137

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			18	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Time, A, B, C to Y	2 4		11 25	17 38	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Time, A, B, C to Y	3 3		16 19	24 29	ns	
t _{PLH} t _{PHL}	Propagation Delay Time, Enable G2 to Y	2 2		13 16	21 27	ns	
t _{PLH} t _{PHL}	Propagation Delay Time, Enable G1 to Y	3 3		14 18	21 27	ns	
t _{PLH} t _{PHL}	Propagation Delay Time, Enable GL to Y	3 4		18 25	27 38	ns	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Pulse Width — Enable at GL	15			ns	V _{CC} = 5.0 V
t _s	Setup Time, A, B, C	10			ns	
t _h	Hold Time, A, B, C	10			ns	

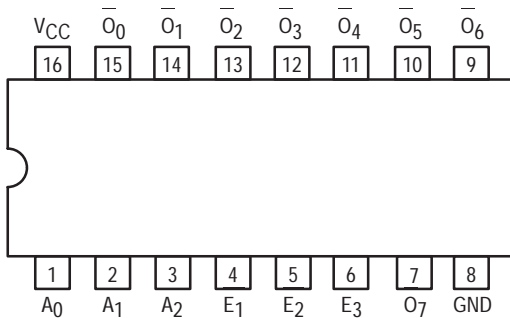


1-OF-8 DECODER/ DEMULTIPLEXER

The LSTTL/MSI SN54/74LS138 is a high speed 1-of-8 Decoder/Demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LS138 devices or to a 1-of-32 decoder using four LS138s and one inverter. The LS138 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Typical Power Dissipation of 32 mW
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0 – A_2	Address Inputs
E_1, E_2	Enable (Active LOW) Inputs
E_3	Enable (Active HIGH) Input
O_0 – O_7	Active LOW Outputs (Note b)

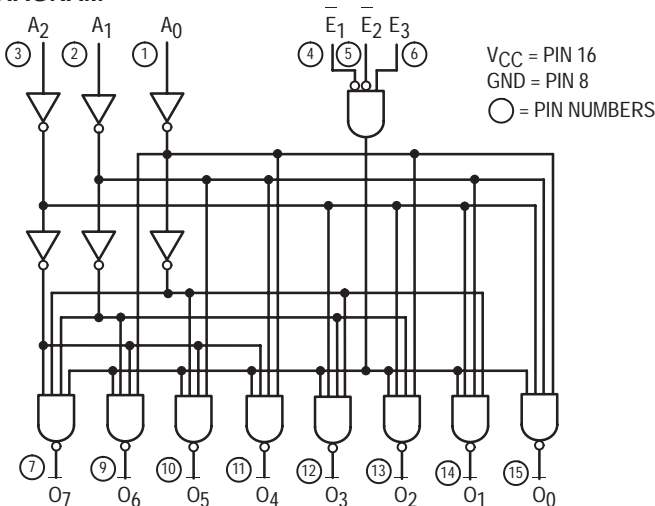
LOADING (Note a)

	HIGH	LOW
A_0 – A_2	0.5 U.L.	0.25 U.L.
E_1, E_2	0.5 U.L.	0.25 U.L.
E_3	0.5 U.L.	0.25 U.L.
O_0 – O_7	10 U.L.	5 (2.5) U.L.

NOTES:

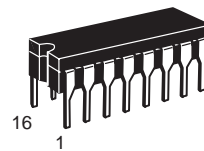
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

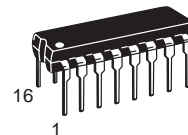


SN54/74LS138

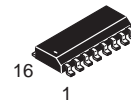
1-OF-8 DECODER/ DEMULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

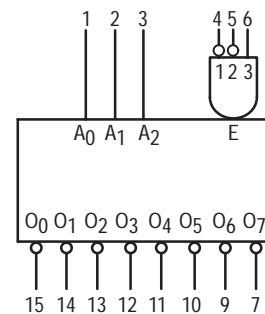


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
 GND = PIN 8

SN54/74LS138

FUNCTIONAL DESCRIPTION

The LS138 is a high speed 1-of-8 Decoder/Demultiplexer fabricated with the low power Schottky barrier diode process. The decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled provides eight mutually exclusive active LOW Outputs ($O_0 - O_7$). The LS138 features three Enable inputs, two active LOW (E_1, E_2) and one active HIGH (E_3). All outputs will be HIGH unless E_1 and E_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel ex-

pansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LS138s and one inverter. (See Figure a.)

The LS138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active HIGH or active LOW state.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E_1}$	$\overline{E_2}$	E_3	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

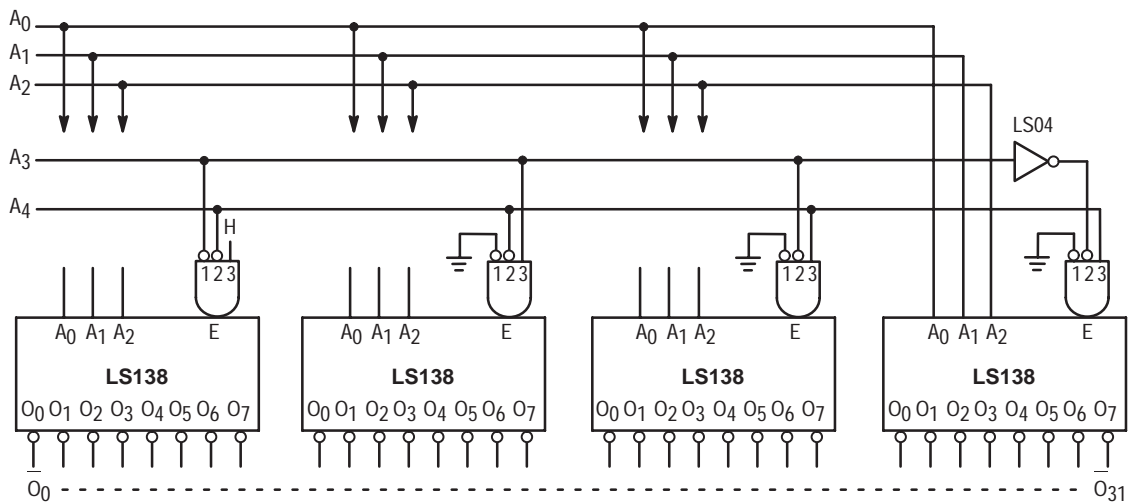


Figure a

SN54/74LS138

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			10	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Address to Output	2 2		13 27	20 41	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Address to Output	3 3		18 26	27 39		
t _{PLH} t _{PHL}	Propagation Delay E ₁ or E ₂ Enable to Output	2 2		12 21	18 32		
t _{PLH} t _{PHL}	Propagation Delay E ₃ Enable to Output	3 3		17 25	26 38		

AC WAVEFORMS

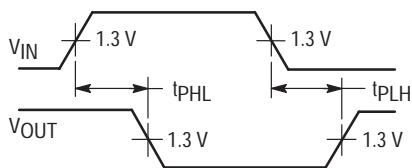


Figure 1

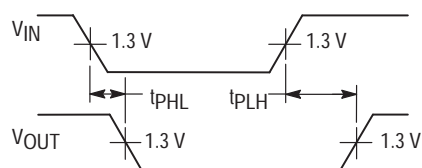


Figure 2

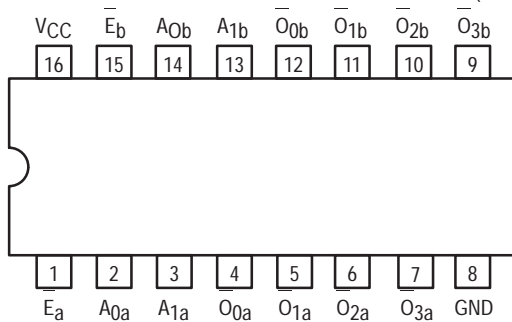


DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The LSTTL/MSI SN54/74LS139 is a high speed Dual 1-of-4 Decoder/De-multiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A₀, A₁ Address Inputs
E Enable (Active LOW) Input
O₀–O₃ Active LOW Outputs (Note b)

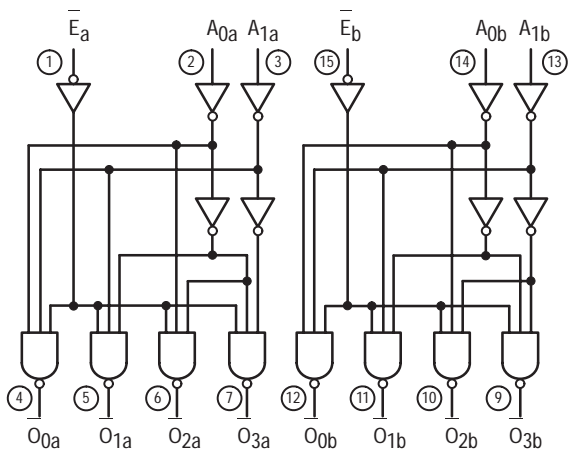
LOADING (Note a)

	HIGH	LOW
A ₀ , A ₁	0.5 U.L.	0.25 U.L.
E	0.5 U.L.	0.25 U.L.
O ₀ –O ₃	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

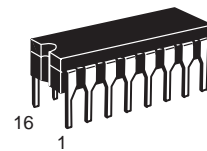
LOGIC DIAGRAM



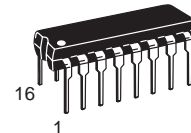
V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS139

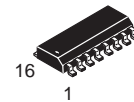
DUAL 1-OF-4 DECODER/ DEMULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

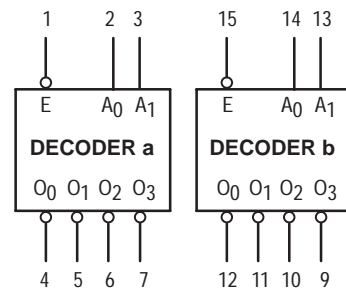


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS139

FUNCTIONAL DESCRIPTION

The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs (O_0-O_3). Each decoder has an active LOW Enable (E). When E is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output

demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
E	A ₀	A ₁	O ₀	O ₁	O ₂	O ₃
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

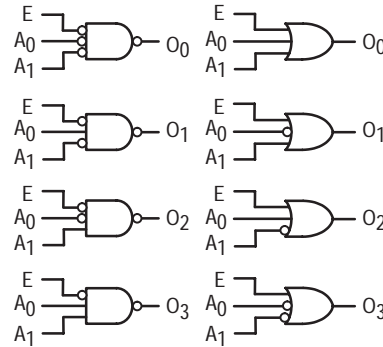


Figure a

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS139

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
		74	0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			11	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Levels of Delay	Limits			Unit	Test Conditions
			Min	Typ	Max		
t_{PLH}	Propagation Delay Address to Output	2		13	20	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PHL}		2		22	33		
t_{PLH}	Propagation Delay Address to Output	3		18	29	ns	
t_{PHL}		3		25	38		
t_{PLH}	Propagation Delay Enable to Output	2		16	24	ns	
t_{PHL}		2		21	32		

AC WAVEFORMS

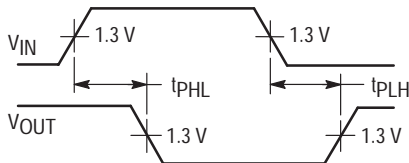


Figure 1

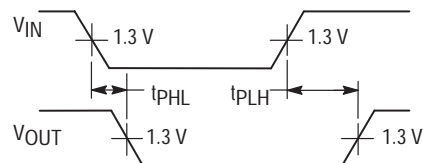


Figure 2

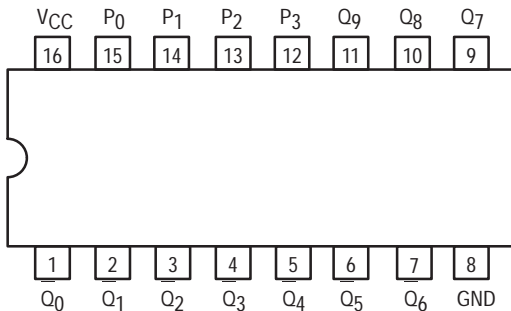


1-OF-10 DECODER/DRIVER OPEN-COLLECTOR

The SN54/74LS145, 1-of-10 Decoder/Driver, is designed to accept BCD inputs and provide appropriate outputs to drive 10-digit incandescent displays. All outputs remain off for all invalid binary input conditions. It is designed for use as indicator/relay drivers or as an open-collector logic circuit driver. Each of the high breakdown output transistors will sink up to 80 mA of current. Typical power dissipation is 35 mW. This device is fully compatible with all TTL families.

- Low Power Version of 54/74145
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

P_0, P_1, P_2, P_3 BCD Inputs
 Q_0 to Q_9 Outputs (Note b)

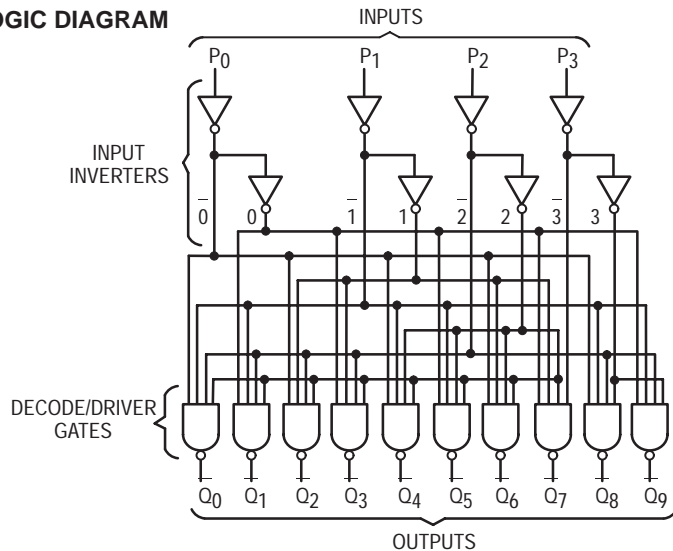
LOADING (Note a)

	HIGH	LOW
Open Collector	0.5 U.L.	0.25 U.L.
		15 (7.5) U.L.

NOTES:

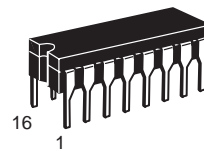
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

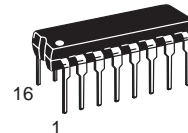


SN54/74LS145

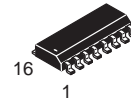
**1-OF-10 DECODER/DRIVER
OPEN-COLLECTOR
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**

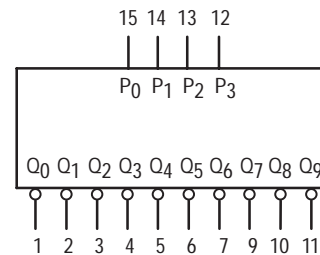


**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS145

TRUTH TABLE

INPUTS				OUTPUTS									
P ₃	P ₂	P ₁	P ₀	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			15	V
I _{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS145

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
I_{OH}	Output HIGH Current	54, 74		250	μA	$V_{CC} = \text{MIN}$, $V_{OH} = \text{MAX}$	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table	
		74	0.35	0.5	V		$I_{OL} = 12 \text{ mA}$
		54, 74	2.3	3.0	V		$I_{OL} = 24 \text{ mA}$ $I_{OL} = 80 \text{ mA}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{CC}	Power Supply Current			13	mA	$V_{CC} = \text{MAX}$, $V_{IN} = \text{GND}$	

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PHL}	Propagation Delay P_n Input to Q_n Output			50	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$
t_{PLH}				50		

AC WAVEFORMS

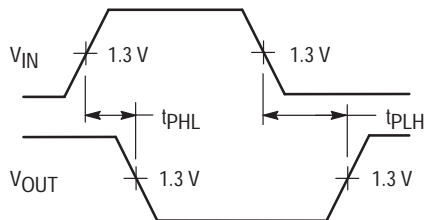


Figure 1

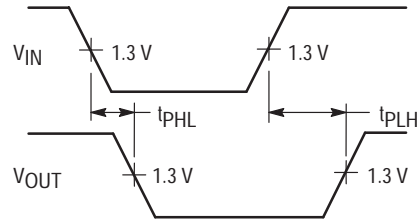


Figure 2



10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

The SN54/74LS147 and the SN54/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0-7 are at logical ones.

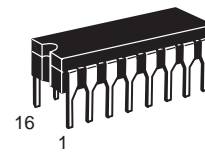
The only dc parameter differences between the LS148 and the LS748 are that (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that t_{PHL} from EI to EO is changed from 40 to 45 ns.

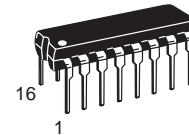
**SN54/74LS147
SN54/74LS148
SN54/74LS748**

**10-LINE-TO-4-LINE
AND 8-LINE-TO-3-LINE
PRIORITY ENCODERS**

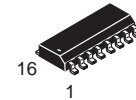
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**

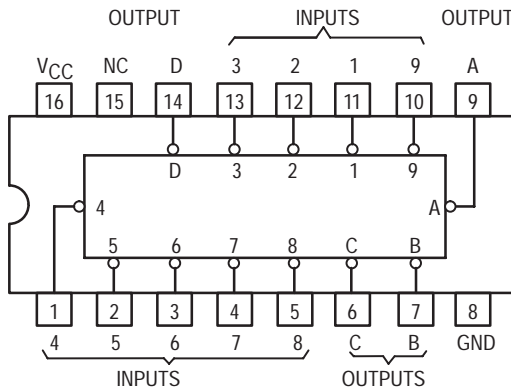


**D SUFFIX
SOIC
CASE 751B-03**

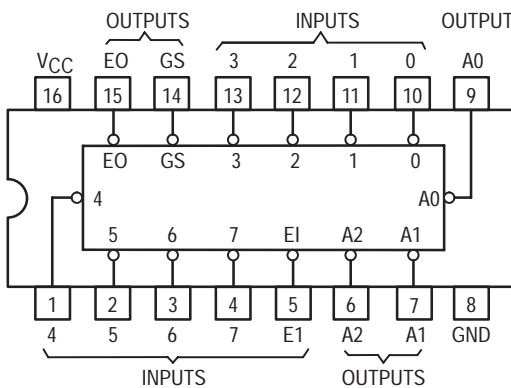
ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

**SN54/74LS147
(TOP VIEW)**



**SN54/74LS148
SN54/74LS748
(TOP VIEW)**



SN54/74LS147 • SN54/74LS148 • SN54/74LS748

**SN54/74LS147
FUNCTION TABLE**

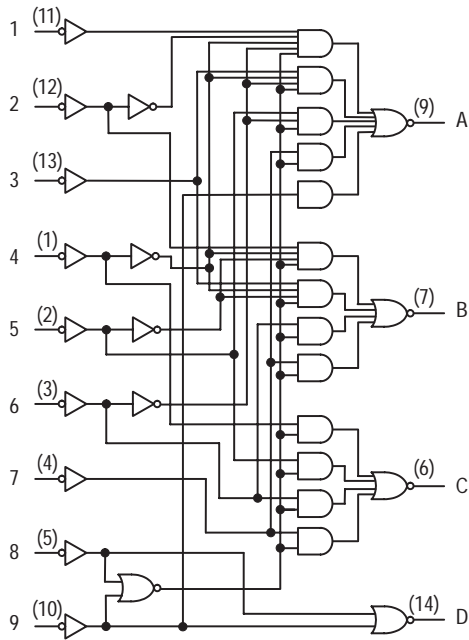
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	L
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

**SN54/74LS148
SN54/74LS748
FUNCTION TABLE**

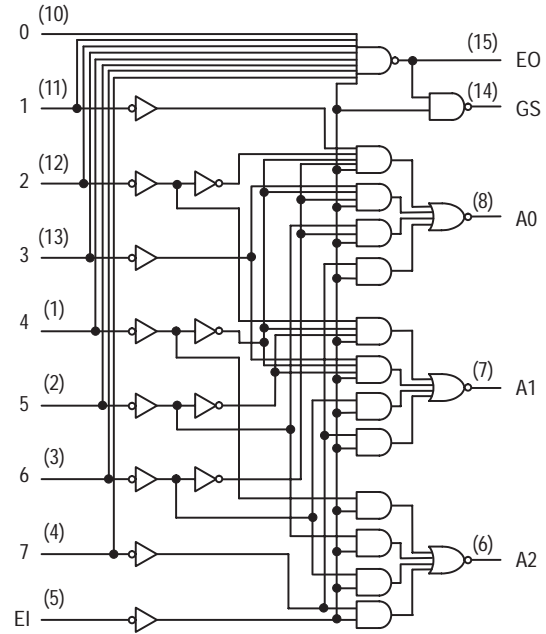
INPUTS								OUTPUTS					
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	L	H	H	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

FUNCTIONAL BLOCK DIAGRAMS



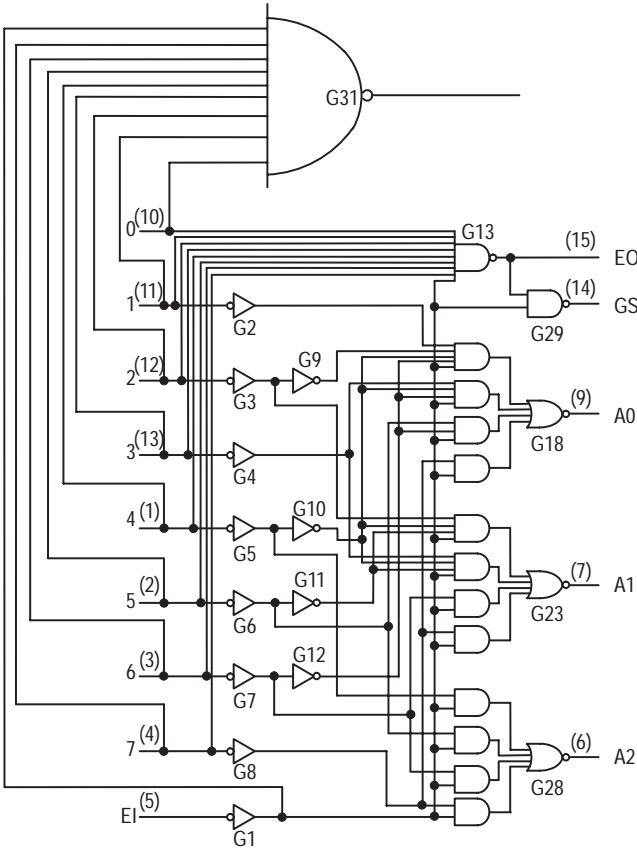
SN54/74LS147



SN54/74LS148

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

FUNCTIONAL BLOCK DIAGRAMS (continued)



SN54/74LS748

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			20 40 40 60	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			0.1 0.2 0.2 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)			-0.4 -0.8 -0.8 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CCH}	Power Supply Current Output HIGH			17	mA	V _{CC} = MAX, All Inputs = 4.5 V	
I _{CCL}	Output LOW			20	mA	V _{CC} = MAX, Inputs 7 & E1 = GND All Other Inputs = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS147 • SN54/74LS148 • SN54/74LS748

AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

SN54/74LS147

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	Test Conditions
				Min	Typ	Max		
t _{PLH}	Any	Any	In-phase output		12	18	ns	C _L = 15 pF, R _L = 2.0 kΩ
t _{PHL}					12	18		
t _{PLH}	Any	Any	Out-of-phase output		21	33	ns	
t _{PHL}					15	23		

SN54/74LS148

SN54/74LS748

Symbol	From (Input)	To (Output)	Waveform	Limits			Unit	Test Conditions	
				Min	Typ	Max			
t _{PLH}	1 thru 7	A0, A1, or A2	In-phase output		14	18	ns	C _L = 15 pF, R _L = 2.0 kΩ	
t _{PHL}					15	25			
t _{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output		20	36	ns		
t _{PHL}					16	29			
t _{PLH}	0 thru 7	EO	Out-of-phase output		7.0	18	ns		
t _{PHL}					25	40			
t _{PLH}	0 thru 7	GS	In-phase output		35	55	ns		
t _{PHL}					9.0	21			
t _{PLH}	EI	A0, A1, or A2	In-phase output		16	25	ns		
t _{PHL}					12	25			
t _{PLH}	EI	GS	In-phase output		12	17	ns		
t _{PHL}					14	36			
t _{PLH}	EI	EO	In-phase output		12	21	ns		
t _{PHL}					28	40			
					30	45			(LS148) (LS748)

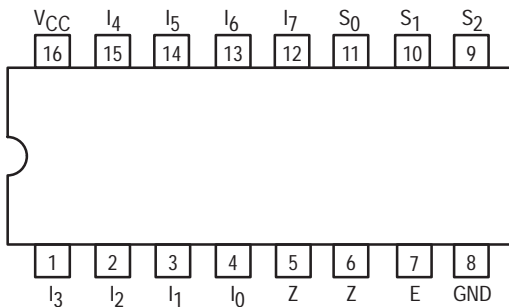


8-INPUT MULTIPLEXER

The TTL/MSI SN54/74LS151 is a high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

S_0-S_2	Select Inputs
E	Enable (Active LOW) Input
I_0-I_7	Multiplexer Inputs
Z	Multiplexer Output (Note b)
Z	Complementary Multiplexer Output (Note b)

LOADING (Note a)

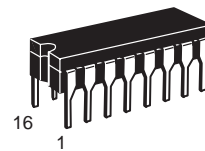
	HIGH	LOW
S_0-S_2	0.5 U.L.	0.25 U.L.
E	0.5 U.L.	0.25 U.L.
I_0-I_7	0.5 U.L.	0.25 U.L.
Z	10 U.L.	5 (2.5) U.L.
Z	10 U.L.	5 (2.5) U.L.

NOTES:

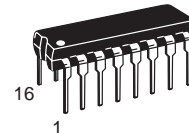
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS151

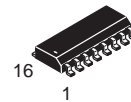
8-INPUT MULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

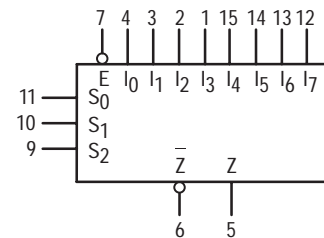


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

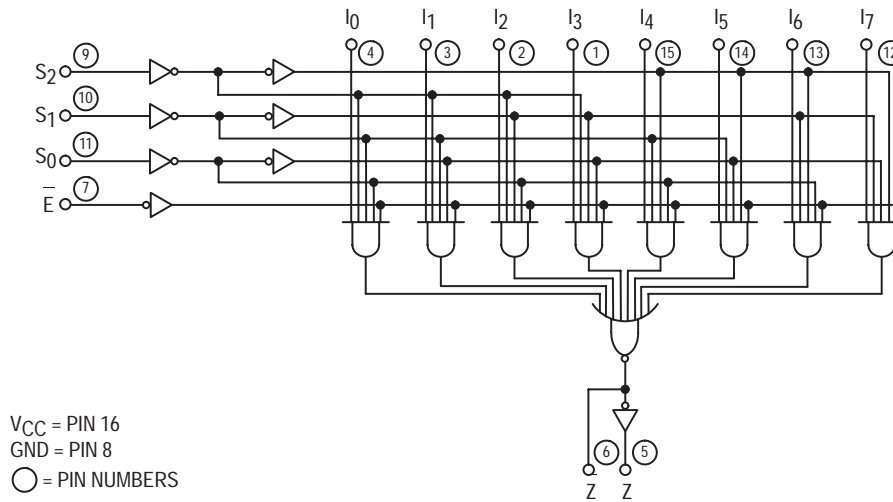
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS151

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

TRUTH TABLE

\bar{E}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\bar{Z}	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

SN54/74LS151

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Select to Output Z		27 18	43 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay Select to Output Z		14 20	23 32	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output Z		26 20	42 32	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output Z		15 18	24 30	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to Output Z		20 16	32 26	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to Output Z		13 12	21 20	ns	

AC WAVEFORMS

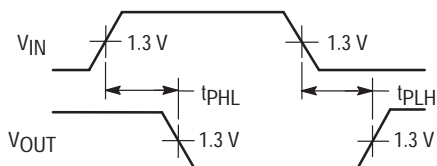


Figure 1

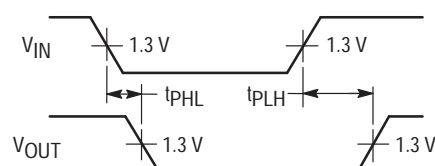


Figure 2

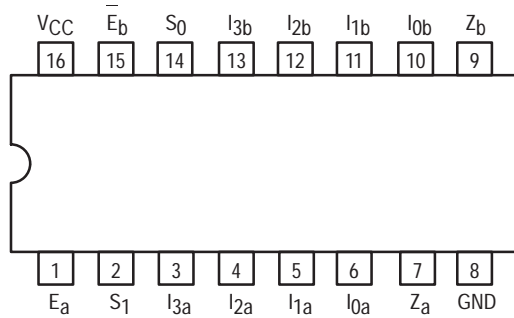


DUAL 4-INPUT MULTIPLEXER

The LSTTL/MSI SN54/74LS153 is a very high speed Dual 4-Input Multiplexer with common select inputs and individual enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the LS153 can generate any two functions of three variables. The LS153 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Non-Inverting Outputs
- Separate Enable for Each Multiplexer
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0	Common Select Input
E	Enable (Active LOW) Input
I_0, I_1	Multiplexer Inputs
Z	Multiplexer Output (Note b)

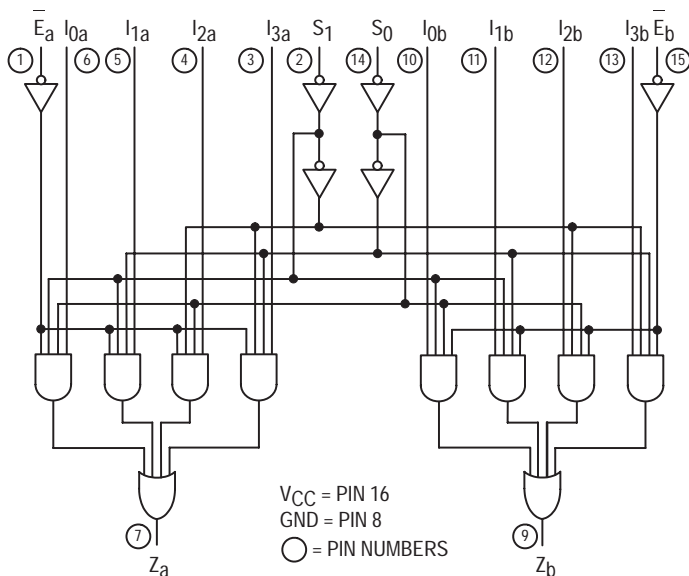
LOADING (Note a)

	HIGH	LOW
S_0	0.5 U.L.	0.25 U.L.
E	0.5 U.L.	0.25 U.L.
I_0, I_1	0.5 U.L.	0.25 U.L.
Z	10 U.L.	5 (2.5) U.L.

NOTES:

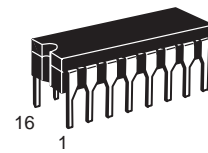
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

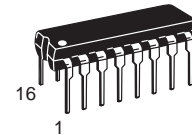


SN54/74LS153

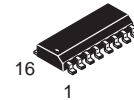
DUAL 4-INPUT MULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

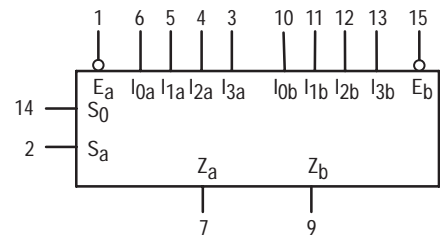


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS153

FUNCTIONAL DESCRIPTION

The LS153 is a Dual 4-input Multiplexer fabricated with Low Power, Schottky barrier diode process for high speed. It can select two bits of data from up to four sources under the control of the common Select Inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active LOW Enables (E_a , E_b) which can be used to strobe the outputs independently. When the Enables (E_a , E_b) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW.

The LS153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select Inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The LS153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function generator. The LS153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	E	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS153

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output		10 17	15 26	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay Select to Output		19 25	29 38	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output		16 21	24 32	ns	

AC WAVEFORMS

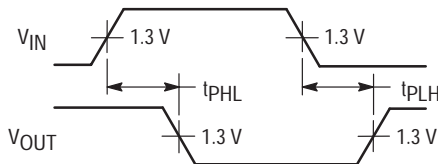


Figure 1

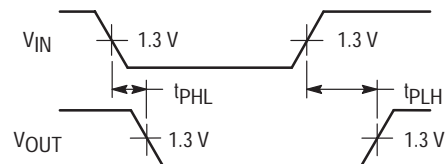


Figure 2

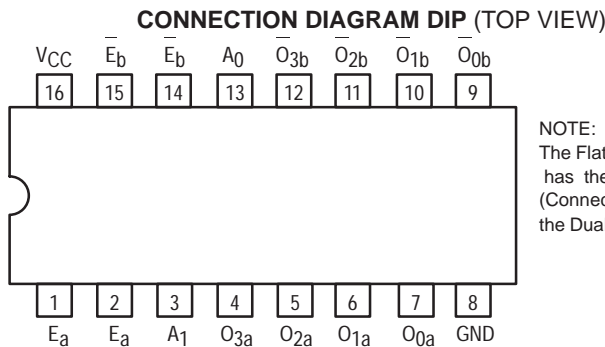


DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The SN54/74LS155 and SN54/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0, A_1	Address Inputs
E_a, E_b	Enable (Active LOW) Inputs
E_a —	Enable (Active HIGH) Input
O_0-O_3	Active LOW Outputs (Note b)

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

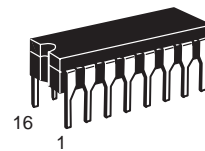
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

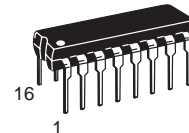
**SN54/74LS155
SN54/74LS156**

**DUAL 1-OF-4 DECODER/
DEMULTIPLEXER**

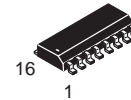
**LS156-OPEN-COLLECTOR
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**

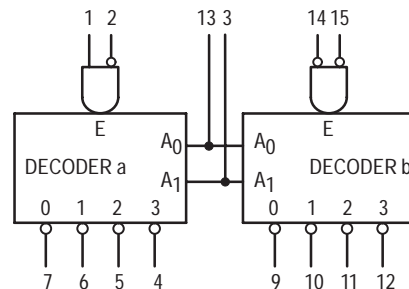


**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

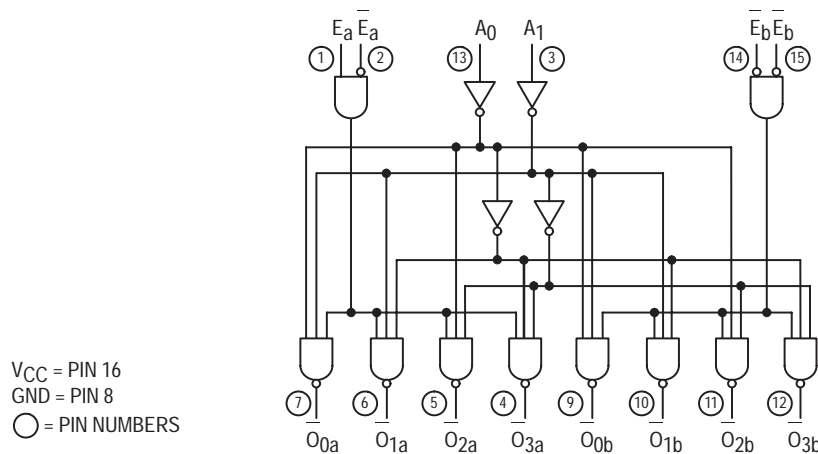
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS155 • SN54/74LS156

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs ($O_0 - O_3$). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \cdot \bar{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the E_a or \bar{E}_a inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\bar{E}_b \cdot E_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying \bar{E}_a to \bar{E}_b and relabeling the common connection as (A_2). The other E_b and E_a are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to

AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (\bar{E}_a + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + A_0 + A_1)$$

$$\text{where } E = E_a + \bar{E}_a; \bar{E} = E_b + E_b$$

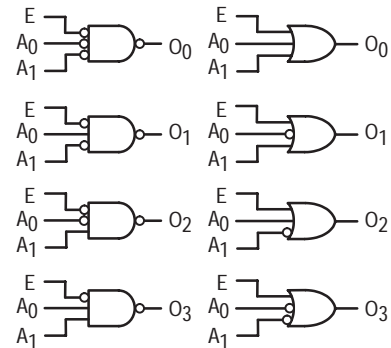


Figure a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	O_0	O_1	O_2	O_3	\bar{E}_b	E_b	O_0	O_1	O_2	O_3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

SN54/74LS155

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Address, E_a or E_b to Output		10 19	15 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay Address to Output		17 19	26 30	ns	
t_{PLH} t_{PHL}	Propagation Delay E_a to Output		18 18	27 27	ns	

AC WAVEFORMS

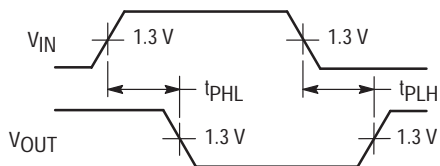


Figure 1

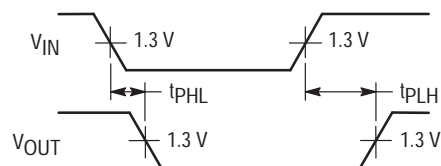


Figure 2

SN54/74LS156

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54, 74		100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current			10	mA	V _{CC} = MAX

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Address, E _a or E _b to Output		25 34	40 51	ns	V _{CC} = 5.0 V C _L = 15 pF R _L = 2.0 kΩ
t _{PLH} t _{PHL}	Propagation Delay Address to Output		31 34	46 51	ns	
t _{PLH} t _{PHL}	Propagation Delay E _a to Output		32 32	48 48	ns	

AC WAVEFORMS

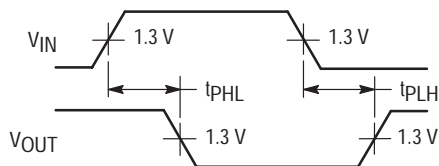


Figure 1

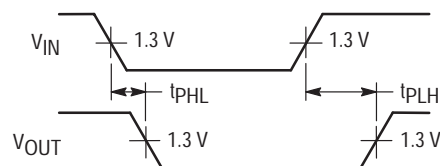


Figure 2

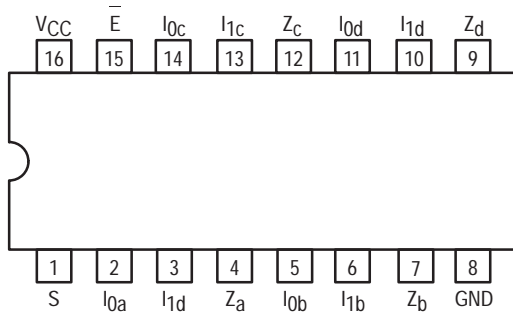


QUAD 2-INPUT MULTIPLEXER

The LSTTL/MSI SN54/74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S	Common Select Input
E	Enable (Active LOW) Input
I0a-I0d	Data Inputs from Source 0
I1a-I1d	Data Inputs from Source 1
Za-Zd	Multiplexer Outputs (Note b)

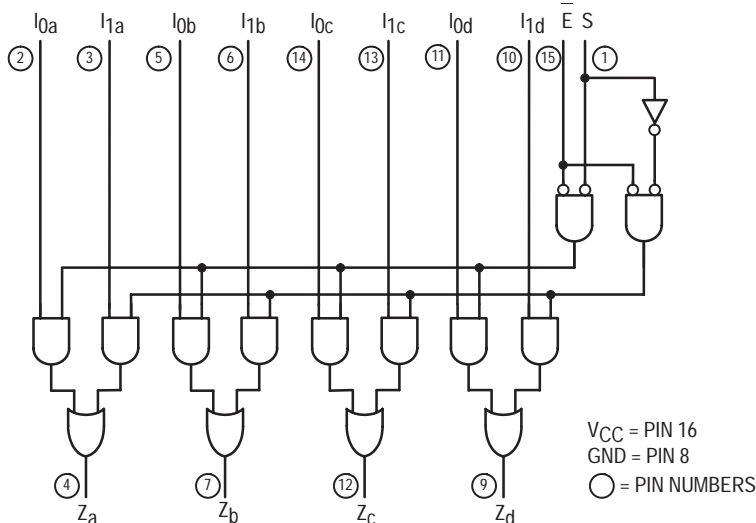
LOADING (Note a)

	HIGH	LOW
S	1.0 U.L.	0.5 U.L.
E	1.0 U.L.	0.5 U.L.
I0a-I0d	0.5 U.L.	0.25 U.L.
I1a-I1d	0.5 U.L.	0.25 U.L.
Za-Zd	10 U.L.	5 (2.5) U.L.

NOTES:

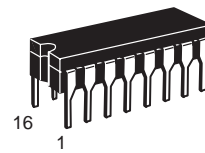
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

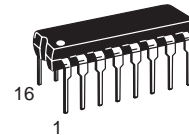


SN54/74LS157

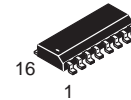
QUAD 2-INPUT MULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

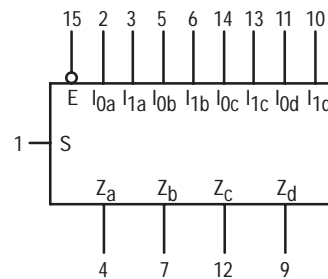


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS157

FUNCTIONAL DESCRIPTION

The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are:

$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \quad Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \quad Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
E	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS157

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current I_{Q}, I_1 E, S				20 40	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
	I_{Q}, I_1 E, S				0.1 0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current I_{Q}, I_1 E, S				-0.4 -0.8	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-20			-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current				16	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output		9.0	14	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay Enable to Output		13	20	ns	
t_{PLH} t_{PHL}	Propagation Delay Select to Output		15	23	ns	

AC WAVEFORMS

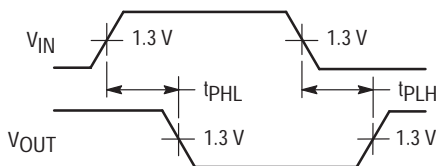


Figure 1

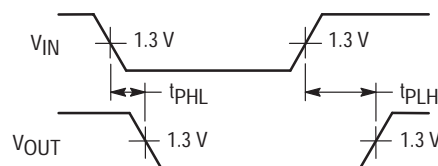


Figure 2

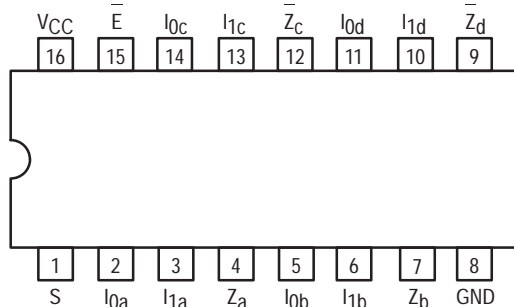


QUAD 2-INPUT MULTIPLEXER

The LSTTL/MSI SN54L/74LS158 is a high speed Quad 2-input Multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The LS158 can also generate any four of the 16 different functions of two variables. The LS158 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Inverted Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts
- Special Circuitry Ensures Glitch Free Multiplexing

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S	Common Select Input
E	Enable (Active LOW) Input
I0a-I0d	Data Inputs from Source 0
I1a-I1d	Data Inputs from Source 1
Za-Zd	Inverted Outputs (Note b)

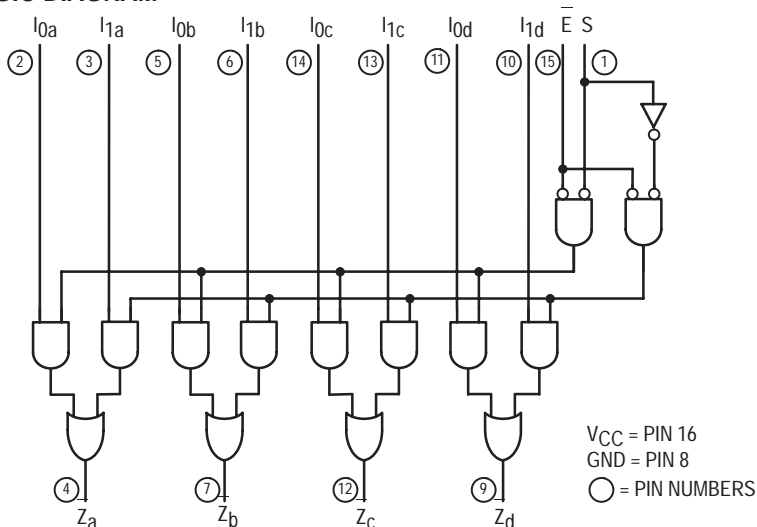
LOADING (Note a)

	HIGH	LOW
S	1.0 U.L.	0.5 U.L.
E	1.0 U.L.	0.5 U.L.
I0a-I0d	0.5 U.L.	0.25 U.L.
I1a-I1d	0.5 U.L.	0.25 U.L.
Za-Zd	10 U.L.	5 (2.5) U.L.

NOTES:

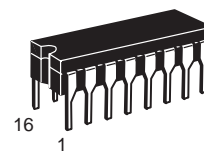
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

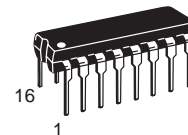


SN54/74LS158

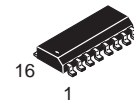
QUAD 2-INPUT MULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

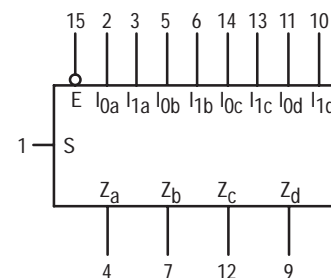


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS158

FUNCTIONAL DESCRIPTION

The LS158 is a Quad 2-input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is deter-

mined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
E	S	I ₀	I ₁	Z
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS158

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current I _Q , I ₁ E, S			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	I _Q , I ₁ E, S			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current I _Q , I ₁ E, S			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			8.0	mA	V _{CC} = MAX All inputs at 4.5 V. All outputs open.	
I _{CC}	Power Supply Current			11	mA	V _{CC} = MAX All other input combinations. All outputs open.	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Data to Output		7.0 10	12 15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Enable to Output		11 18	17 24	ns	
t _{PLH} t _{PHL}	Propagation Delay Select to Output		13 16	20 24	ns	

AC WAVEFORMS

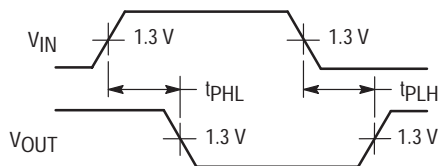


Figure 1

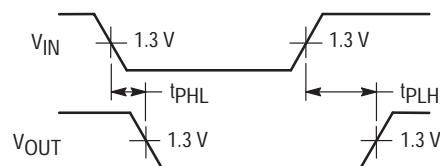


Figure 2



BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

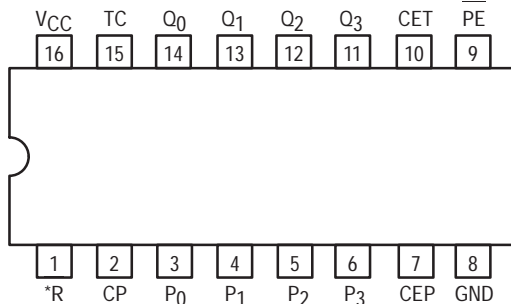
The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary).

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

PE	Parallel Enable (Active LOW) Input
P ₀ -P ₃	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
SR	Synchronous Reset (Active LOW) Input
Q ₀ -Q ₃	Parallel Outputs (Note b)
TC	Terminal Count Output (Note b)

LOADING (Note a)

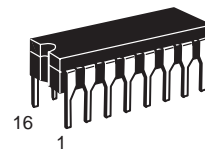
	HIGH	LOW
PE	1.0 U.L.	0.5 U.L.
P ₀ -P ₃	0.5 U.L.	0.25 U.L.
CEP	0.5 U.L.	0.25 U.L.
CET	1.0 U.L.	0.5 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
SR	1.0 U.L.	0.5 U.L.
Q ₀ -Q ₃	10 U.L.	5 (2.5) U.L.
TC	10 U.L.	5 (2.5) U.L.

NOTES:

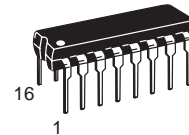
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A

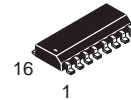
**BCD DECADE COUNTERS/
4-BIT BINARY COUNTERS**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

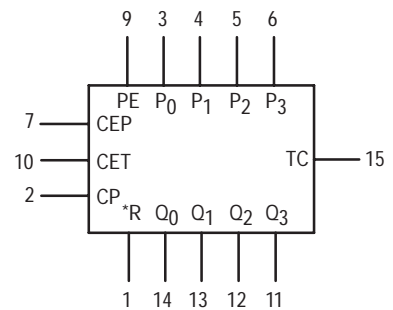


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

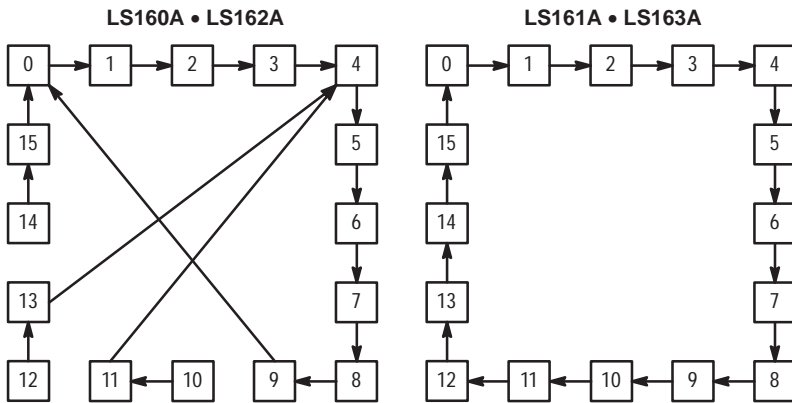
LOGIC SYMBOL



*MR for LS160A and LS161A
*SR for LS162A and LS163A

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = $\overline{\text{CEP}} \cdot \overline{\text{CET}} \cdot \overline{\text{PE}}$
 TC for LS160A & LS162A = $\text{CET} \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3}$
 TC for LS161A & LS163A = $\text{CET} \cdot \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3}$
 Preset = $\overline{\text{PE}} \cdot \text{CP} +$ (rising clock edge)
 Reset = $\overline{\text{MR}}$ (LS160A & LS161A)
 Reset = $\overline{\text{SR}} \cdot \text{CP} +$ (rising clock edge)
 (LS162A & LS163A)

NOTE:

The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel ($\overline{\text{CEP}}$) and Count Enable Trickle ($\overline{\text{CET}}$) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the $\overline{\text{CEP}}$, $\overline{\text{CET}}$, and $\overline{\text{PE}}$ inputs are HIGH. When the $\overline{\text{PE}}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ can be used to inhibit the count sequence. With the $\overline{\text{PE}}$ held HIGH, a LOW on either the $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs ($\overline{\text{CET}} \cdot \overline{\text{CEP}}$) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle ($\overline{\text{CET}}$) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for

the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the $\overline{\text{CET}}$ input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the $\overline{\text{CET}}$ input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{\text{MR}}$) of the LS160A and LS161A is asynchronous. When the $\overline{\text{MR}}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{\text{MR}}$ pin should never be left open. If not used, the $\overline{\text{MR}}$ pin should be tied through a resistor to V_{CC} , or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{\text{SR}}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding $\overline{\text{CET}}$, $\overline{\text{CEP}}$ and $\overline{\text{PE}}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (\uparrow)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

**SN54/74LS160A • SN54/74LS161A
SN54/74LS162A • SN54/74LS163A**

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

LS160A and LS161A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current MR, Data, CEP, Clock PE, CET			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	MR, Data, CEP, Clock PE, CET			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

LS162A and LS163A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current Data, CEP, Clock PE, CET, SR			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Data, CEP, Clock PE, CET, SR			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Data, CEP, Clock, PE, SR CET			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			31 32	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	32		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t _{PHL}	MR or SR to Q		20	28	ns	

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{WCP}	Clock Pulse Width Low	25			ns	$V_{CC} = 5.0\text{ V}$
t_W	MR or SR Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time PE or SR	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time MR to CP	15			ns	

*CEP, CET or DATA

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

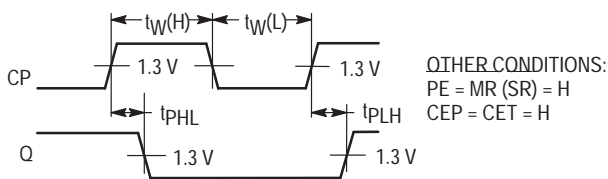


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

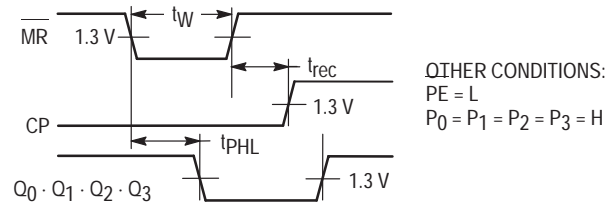


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

SN54/74LS160A • SN54/74LS161A SN54/74LS162A • SN54/74LS163A

AC WAVEFORMS (continued)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive \overline{TC} pulse occurs when the outputs are in the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS160 and LS162 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161 and LS163.

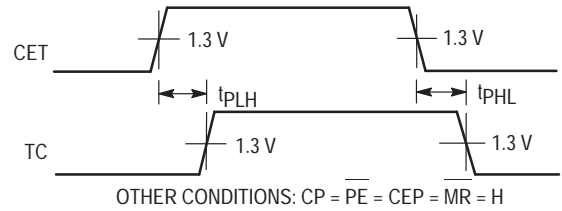


Figure 3

CLOCK TO TERMINAL COUNT DELAYS

The positive \overline{TC} pulse is coincident with the output state ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161 and LS163 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the LS161 and LS163.

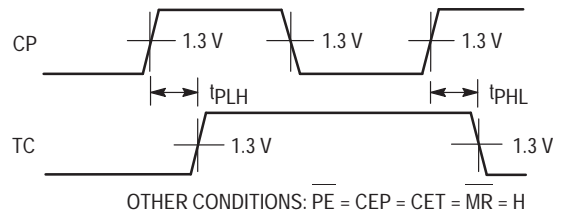


Figure 4

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

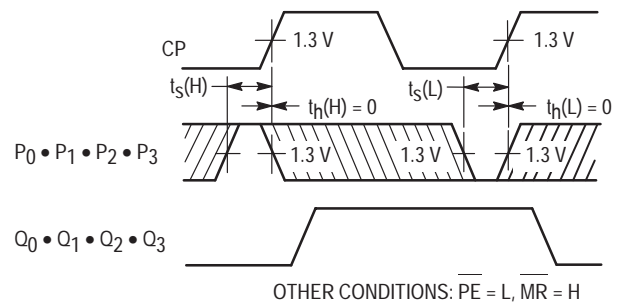


Figure 5

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (PE) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

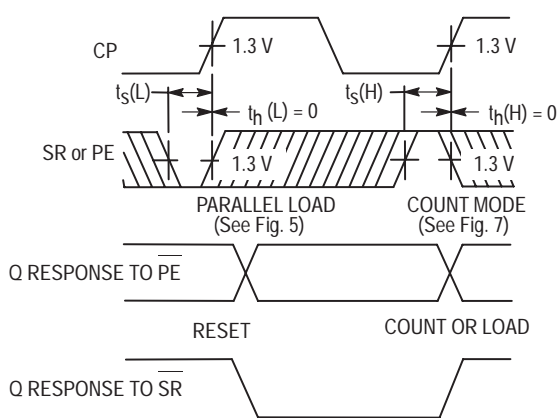


Figure 6

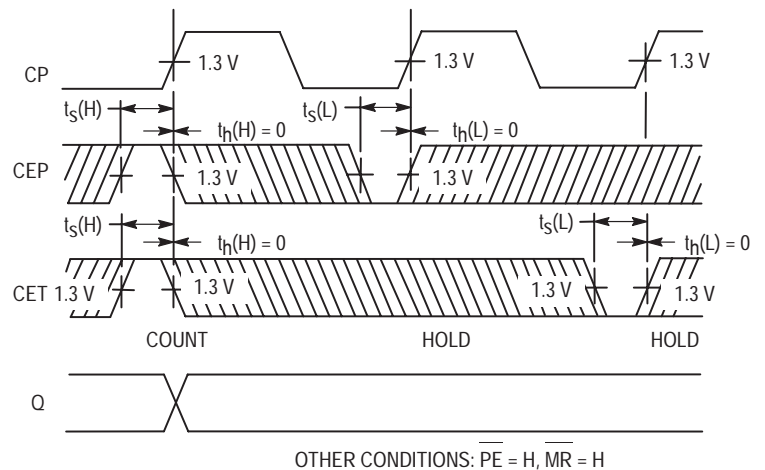


Figure 7

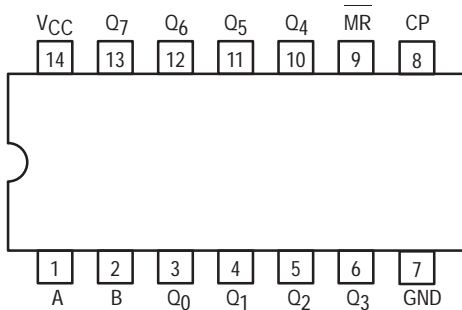


SERIAL-IN PARALLEL-OUT SHIFT REGISTER

The SN54/74LS164 is a high speed 8-Bit Serial-In Parallel-Out Shift Register. Serial data is entered through a 2-Input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A, B	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ -Q ₇	Outputs (Note b)

LOADING (Note a)

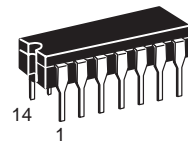
	HIGH	LOW
A, B	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ -Q ₇	10 U.L.	5 (2.5) U.L.

NOTES:

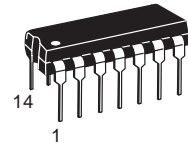
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS164

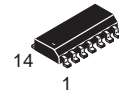
SERIAL-IN PARALLEL-OUT SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

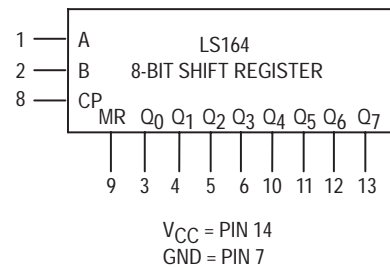


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

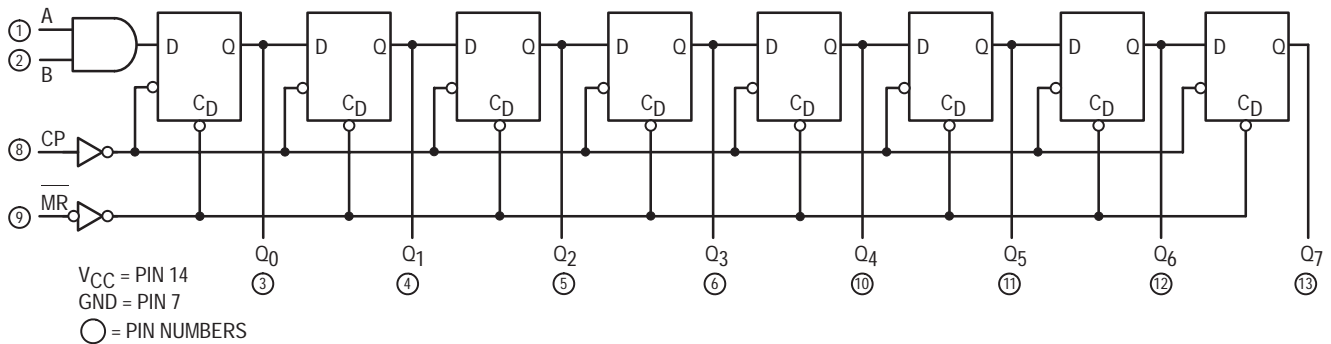
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS164

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A•B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	A	B	Q ₀	Q ₁ -Q ₇
Reset (Clear)	L	X	X	L	L - L
Shift	H	l	l	L	q ₀ - q ₆
	H	l	h	L	q ₀ - q ₆
	H	h	l	L	q ₀ - q ₆
	H	h	h	H	q ₀ - q ₆

L (l) = LOW Voltage Levels

H (h) = HIGH Voltage Levels

X = Don't Care

q_n = Lower case letters indicate the state of the referenced input or output one set-up time prior to the LOW to HIGH clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS164

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5				
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74		0.35	0.5	V		
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				27	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
f _{MAX}	Maximum Clock Frequency		25	36		MHz	V _{CC} = 5.0 V C _L = 15 pF	
t _{PHL}	Propagation Delay MR to Output Q			24	36	ns		
t _{PLH} t _{PHL}	Propagation Delay Clock to Output Q			17 21	27 32	ns		

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _W	CP, MR Pulse Width		20			ns	V _{CC} = 5.0 V	
t _S	Data Setup Time		15			ns		
t _H	Data Hold Time		5.0			ns		
t _{rec}	MR to Clock Recovery Time		20			ns		

SN54/74LS164

AC WAVEFORMS

*The shaded areas indicate when the input is permitted to change for predictable output performance.

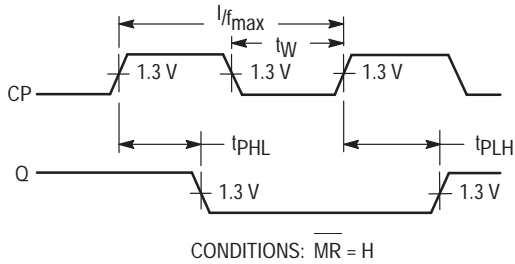


Figure 1. Clock to Output Delays and Clock Pulse Width

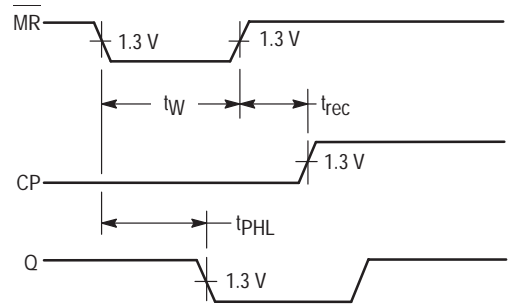


Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

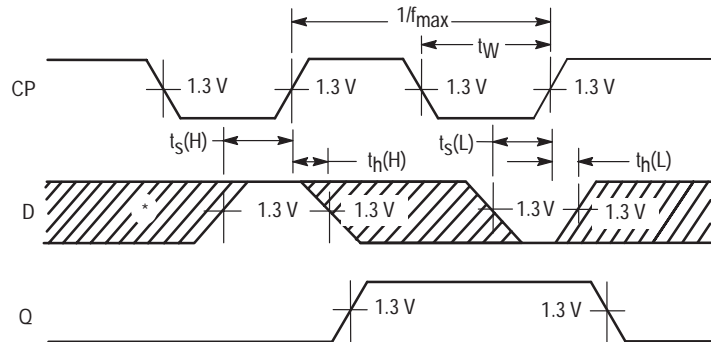


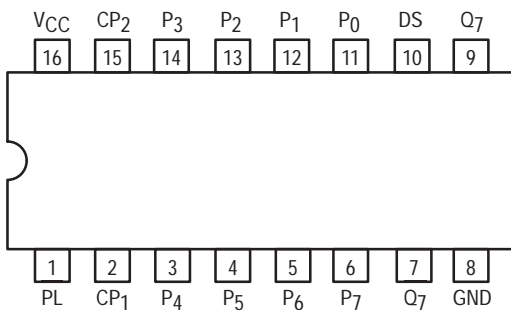
Figure 3. Data Setup and Hold Times



8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER

The SN54/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the Parallel Load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

CP₁, CP₂ Clock (LOW-to-HIGH Going Edge) Inputs
 DS Serial Data Input
 PL Asynchronous Parallel Load (Active LOW) Input
 P₀–P₇ Parallel Data Inputs
 Q₇ Serial Output from Last State (Note b)
 Q₇ Complementary Output (Note b)

LOADING (Note a)

	HIGH	LOW
CP ₁ , CP ₂	0.5 U.L.	0.25 U.L.
DS	0.5 U.L.	0.25 U.L.
PL	1.5 U.L.	0.75 U.L.
P ₀ –P ₇	0.5 U.L.	0.25 U.L.
Q ₇	10 U.L.	5 (2.5) U.L.
Q ₇	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

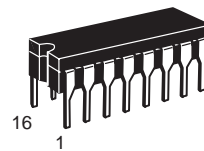
TRUTH TABLE

PL	CP		CONTENTS								RESPONSE
	1	2	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	P ₀	P ₁	P ₂	P ₃	P ₄	P ₅	P ₆	P ₇	Parallel Entry
H	L	↗	DS	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H	H	↗	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change
H	↗	L	DS	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Right Shift
H	↗	H	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	No Change

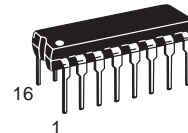
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

SN54/74LS165

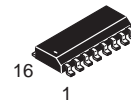
8-BIT PARALLEL-TO-SERIAL SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

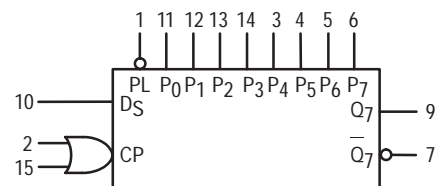


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXD SOIC

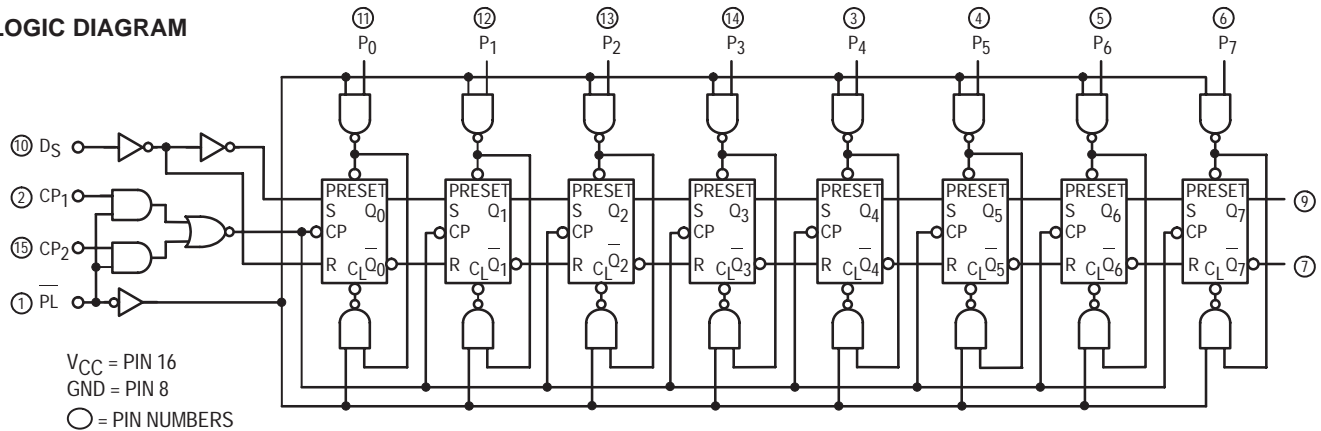
LOGIC SYMBOL



VCC = PIN 16
 GND = PIN 8

SN54/74LS165

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the PL signal is LOW. The parallel data can change while PL is LOW, provided that the recommended set-up and hold times are observed.

For clock operation, PL must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by

applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended setup and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS165

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5	V	
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current Other Inputs PL Input			20 60	μA	V _{CC} = MAX, V _{IN} = 2.7 V
	Other Inputs PL Input			0.1 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Other Inputs PL Input			-0.4 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			36	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency	25	35		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay PL to Output		22 22	35 35	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to Output		27 28	40 40	ns	
t _{PLH} t _{PHL}	Propagation Delay P ₇ to Q ₇		14 21	25 30	ns	
t _{PLH} t _{PHL}	Propagation Delay P ₇ to Q ₇		21 16	30 25	ns	

SN54/74LS165

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	CP Clock Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
t_W	PL Pulse Width	15			ns	
t_S	Parallel Data Setup Time	10			ns	
t_S	Serial Data Setup Time	20			ns	
t_S	CP ₁ to CP ₂ Setup Time ¹	30			ns	
t_H	Hold Time	0			ns	
t_{rec}	Recovery Time, PL to CP	45			ns	

¹ The role of CP₁, and CP₂ in an application may be interchanged.

DEFINITION OF TERMS:

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the PL pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer loaded Data to the Q outputs.

AC WAVEFORMS

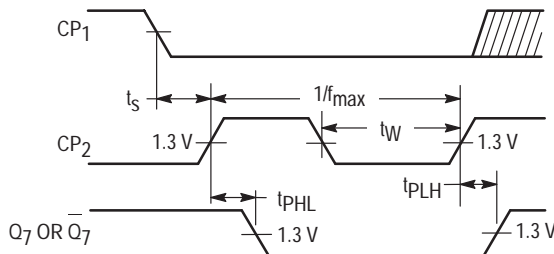


Figure 1

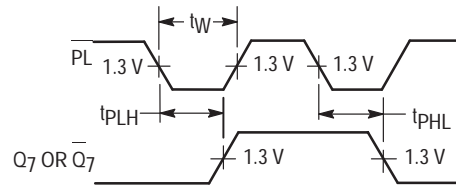


Figure 2

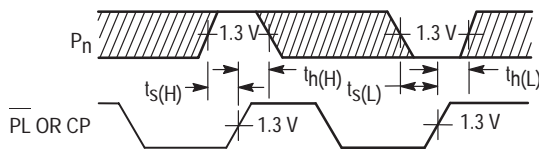


Figure 3

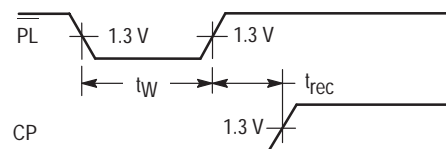


Figure 4

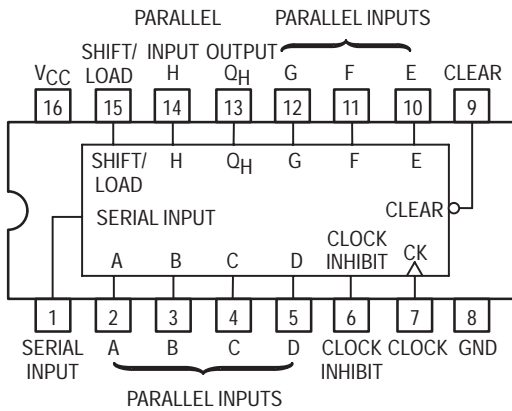


8-BIT SHIFT REGISTERS

The SN54L/74LS166 is an 8-Bit Shift Register. Designed with all inputs buffered, the drive requirements are lowered to one 54/74LS standard load. By utilizing input clamping diodes, switching transients are minimized and system design simplified.

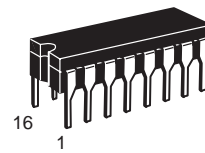
The LS166 is a parallel-in or serial-in, serial-out shift register and has a complexity of 77 equivalent gates with gated clock inputs and an overriding clear input. The shift/load input establishes the parallel-in or serial-in mode. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. Synchronous loading occurs on the next clock pulse when this is low and the parallel data inputs are enabled. Serial data flow is inhibited during parallel loading. Clocking is done on the low-to-high level edge of the clock pulse via a two input positive NOR gate, which permits one input to be used as a clock enable or clock inhibit function. Clocking is inhibited when either of the clock inputs are held high, holding either input low enables the other clock input. This will allow the system clock to be free running and the register stopped on command with the other clock input. A change from low-to-high on the clock inhibit input should only be done when the clock input is high. A buffered direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

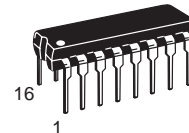


SN54/74LS166

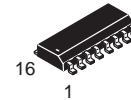
8-BIT SHIFT REGISTERS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

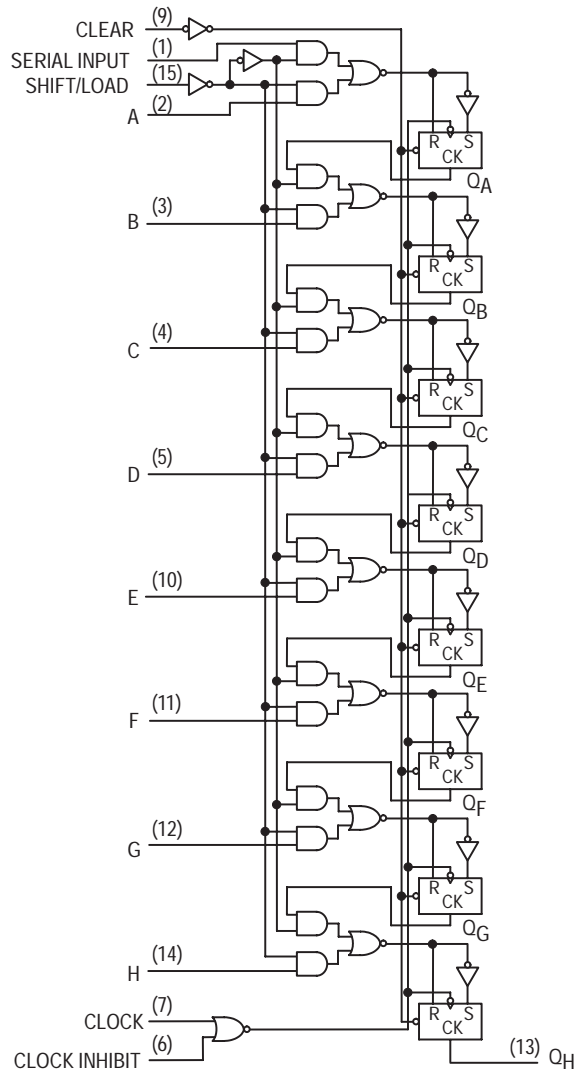
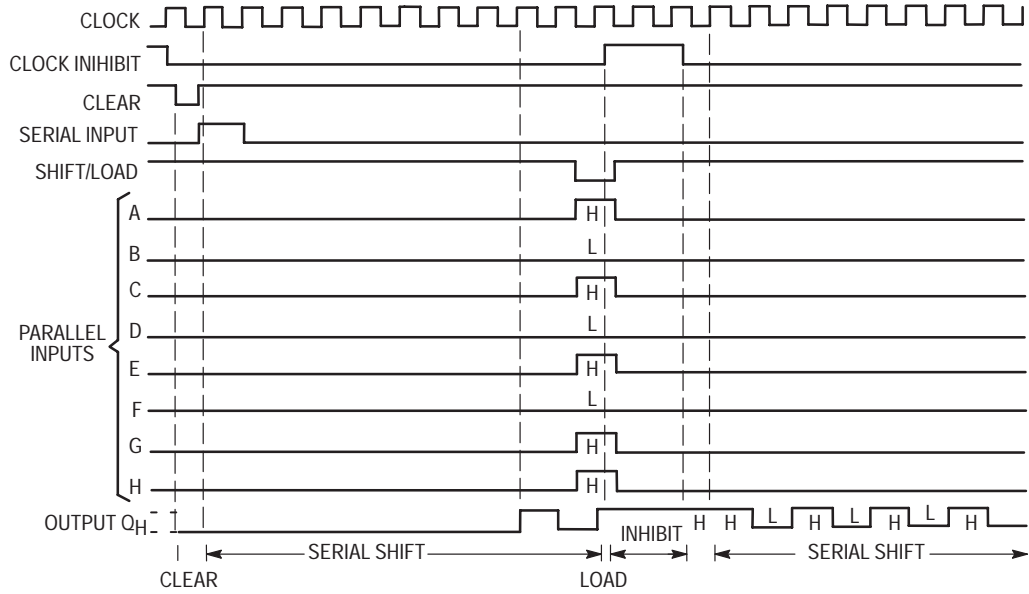
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT Q _H	
CLEAR	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q _A		Q _B
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}

SN54/74LS166

Typical Clear, Shift, Load, Inhibit, and Shift Sequences



SN54/74LS166

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			38	mA	V _{CC} = MAX	

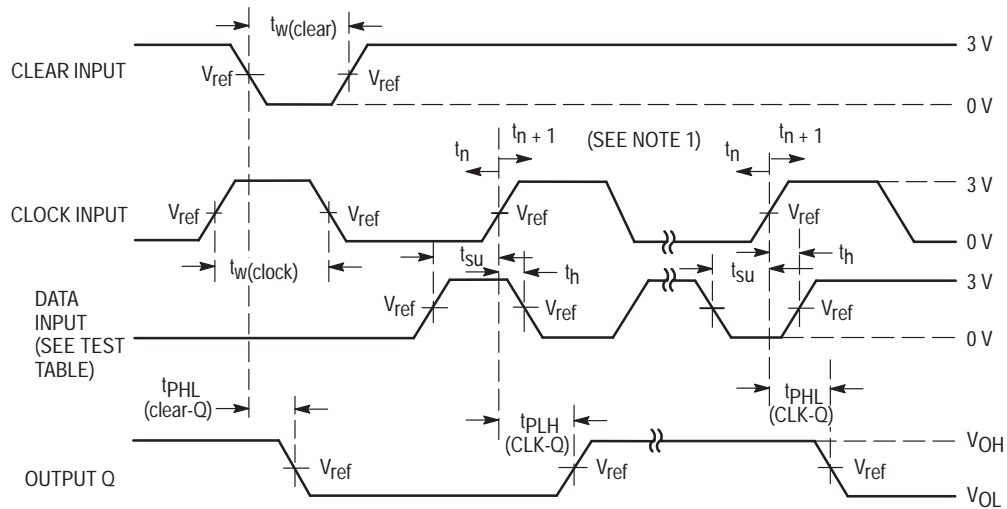
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS166

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}

AC WAVEFORMS



NOTE 1. t_n = bit time before clocking transition
 t_{n+1} = bit time after one clocking transition
 t_{n+8} = bit time after eight clocking transition
 LS166 $V_{\text{ref}} = 1.3$ V.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	35		MHz	$V_{\text{CC}} = 5.0$ V $C_L = 15$ pF
t_{PHL}	Clear to Output		19	30	ns	
t_{PLH} t_{PHL}	Clock to Output		23 24	35 35	ns	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_w	Clock Clear Pulse Width	30			ns	$V_{\text{CC}} = 5.0$ V
t_s	Mode Control Setup Time	30			ns	
t_s	Data Setup Time	20			ns	
t_h	Hold Time, Any Input	15			ns	

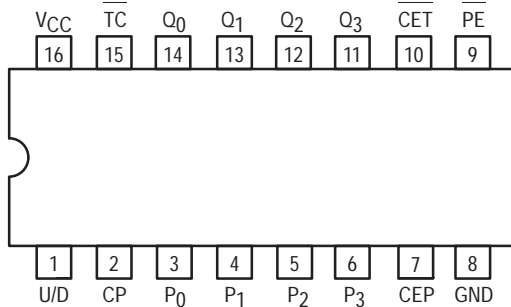


BCD DECADE/MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

The SN54/74LS168 and SN54/74LS169 are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. The SN54/74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the SN54/74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- Low Power Dissipation 100 mW Typical
- High-Speed Count Frequency 30 MHz Typical
- Fully Synchronous Operation
- Full Carry Lookahead for Easy Cascading
- Single Up/Down Control Input
- Positive Edge-Trigger Operation
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

\overline{CEP}	Count Enable Parallel (Active LOW) Input
\overline{CET}	Count Enable Trickle (Active LOW) Input
\overline{CP}	Clock Pulse (Active positive going edge) Input
\overline{PE}	Parallel Enable (Active LOW) Input
U/D	Up-Down Count Control Input
P_0 - P_3	Parallel Data Inputs
Q_0 - Q_3	Flip-Flop Outputs
TC	Terminal Count (Active LOW) Output

LOADING (Note a)

	HIGH	LOW
\overline{CEP}	0.5 U.L.	0.25 U.L.
\overline{CET}	1.0 U.L.	0.5 U.L.
\overline{CP}	0.5 U.L.	0.25 U.L.
\overline{PE}	0.5 U.L.	0.25 U.L.
U/D	0.5 U.L.	0.25 U.L.
P_0 - P_3	0.5 U.L.	0.25 U.L.
Q_0 - Q_3	10 U.L.	5 (2.5) U.L.
TC	10 U.L.	5 (2.5) U.L.

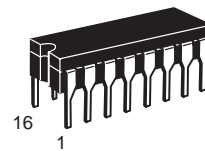
NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

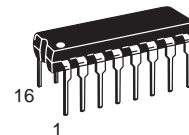
**SN54/74LS168
SN54/74LS169**

**BCD DECADE/MODULO
16 BINARY SYNCHRONOUS
BI-DIRECTIONAL COUNTERS**

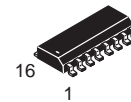
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**

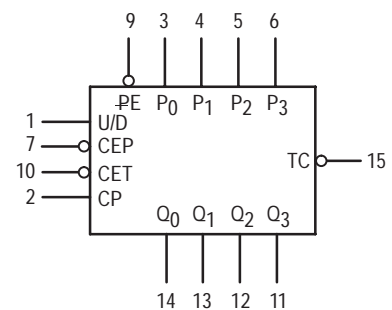


**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL

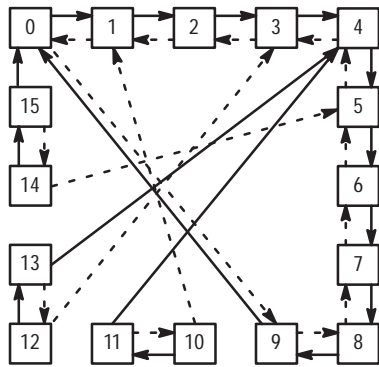


V_{CC} = PIN 16
GND = PIN 8

SN54/74LS168 • SN54/74LS169

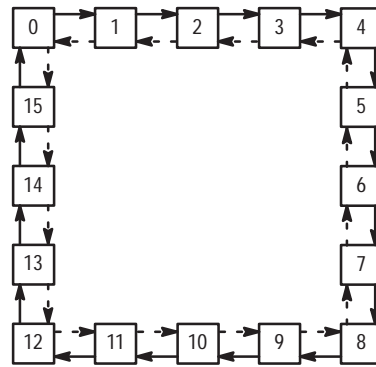
STATE DIAGRAMS

SN54/74LS168
UP/DOWN DECADE COUNTER



→ Count Up
- - - Count Down

SN54/74LS169



SN54/74LS168

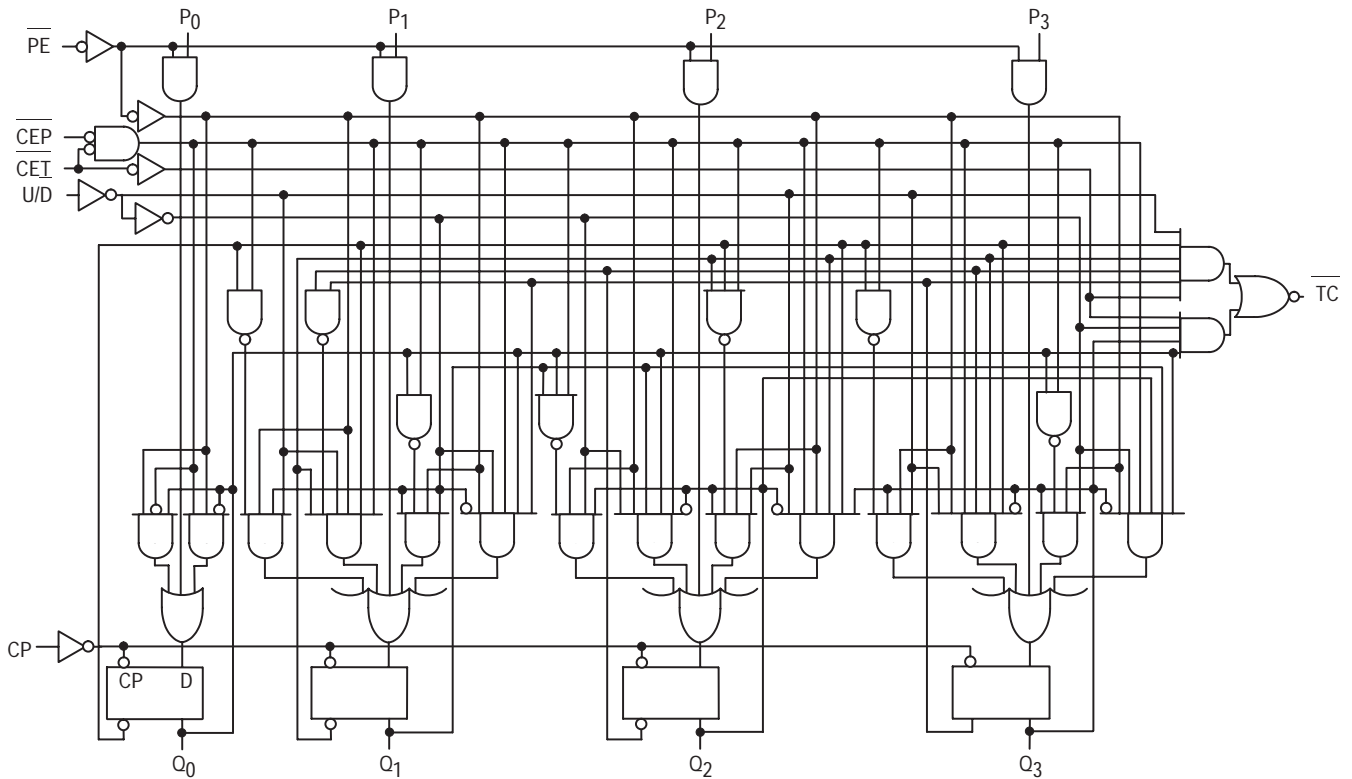
UP: $TC = \overline{Q_0} \cdot \overline{Q_3} \cdot \overline{(U/D)}$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

SN54/74LS169

UP: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{(U/D)}$
DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

LOGIC DIAGRAMS

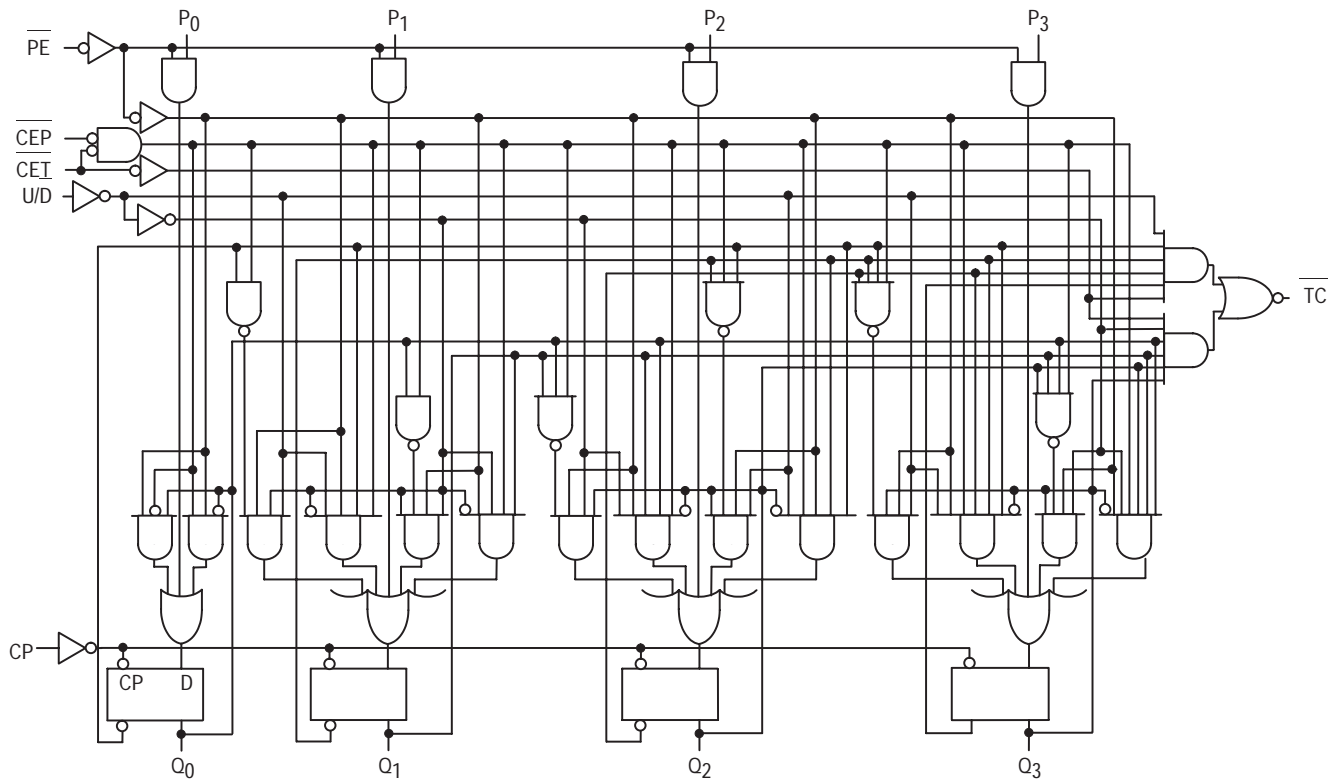
SN54/74LS168



SN54/74LS168 • SN54/74LS169

LOGIC DIAGRAMS (continued)

SN54/74LS169



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS168 • SN54/74LS169

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V		
I _{IH}	Input HIGH Current Other Inputs CET Input				20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Other Input CET Input				0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Other Input CET Input				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				34	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at one time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The SN54/74LS168 and SN54/74LS169 use edge-triggered D-type flip-flops that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the P₀–P₃ inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be LOW and PE must be HIGH. The U/D input then determines the direction of counting.

The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the SN54/74LS168) in the COUNT UP mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. The TC output of the SN54/74LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If illegal state occurs, the SN54/74LS168 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on TC. For this reason the use of TC as a clock signal is not recommended.

MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load (P _n → Q _n)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN54/74LS168 • SN54/74LS169

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	$V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, Clock to TC		23 23	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to any Q		13 15	20 23	ns	
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		15 15	20 20	ns	
t_{PLH} t_{PHL}	Propagation Delay, U/D to TC		17 19	25 29	ns	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
t_s	Setup Time, Data or Enable	20			ns	
t_s	Setup Time PE	25			ns	
t_s	Setup Time U/D	30			ns	
t_h	Hold Time Any Input	0			ns	

SN54/74LS168 • SN54/74LS169

AC WAVEFORMS

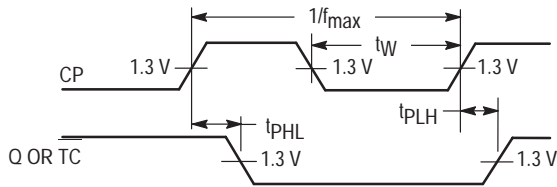


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

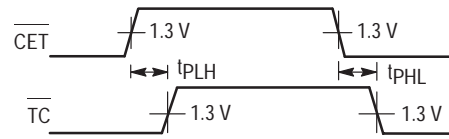


Figure 2. Count Enable Trickle Input To Terminal Count Output Delays

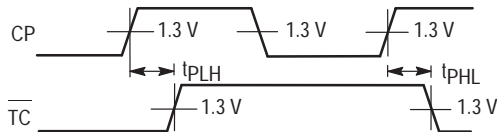


Figure 3. Clock to Terminal Delays

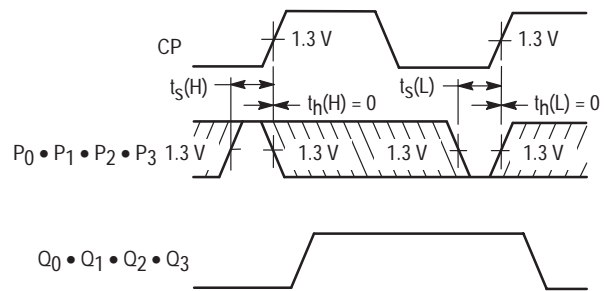
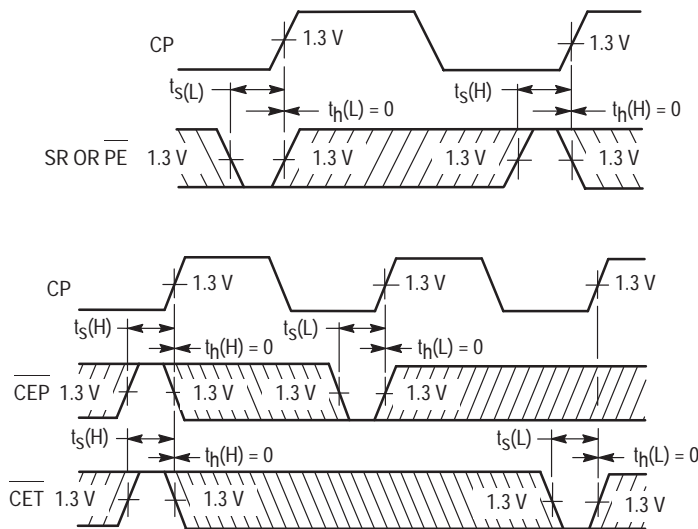


Figure 4. Setup Time (t_s) and Hold (t_h) for Parallel Data Inputs



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Setup Time and Hold Time for Count Enable and Parallel Enable Inputs, and Up-Down Control Inputs

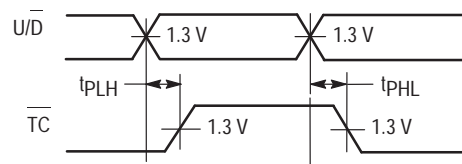


Figure 6. Up-Down Input to Terminal Count Output Delays



4 x 4 REGISTER FILE OPEN-COLLECTOR

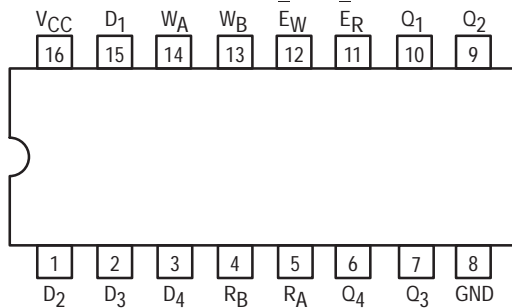
The TTL/MSI SN54/74LS170 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54/74LS670 provides a similar function to this device but it features 3-state outputs.

- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- Low Leakage Open-Collector Outputs for Expansion
- Typical Power Dissipation of 125 mW

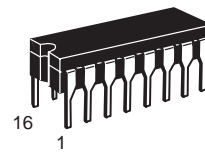
CONNECTION DIAGRAM DIP (TOP VIEW)



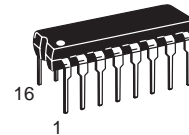
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS170

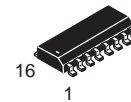
4 x 4 REGISTER FILE
OPEN-COLLECTOR
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

PIN NAMES

D₁–D₄ Data Inputs
W_A, W_B Write Address Inputs
E_W Write Enable (Active LOW) Input
R_A, R_B Read Address Inputs
E_R Read Enable (Active LOW) Input
Q₁–Q₄ Outputs (Note b)

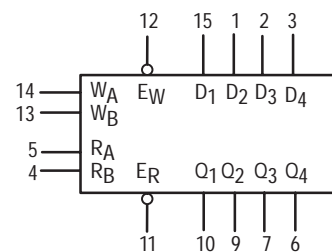
LOADING (Note a)

	HIGH	LOW
D ₁ –D ₄	0.5 U.L.	0.25 U.L.
W _A , W _B	0.5 U.L.	0.25 U.L.
E _W	1.0 U.L.	0.5 U.L.
R _A , R _B	0.5 U.L.	0.25 U.L.
E _R	1.0 U.L.	0.5 U.L.
Q ₁ –Q ₄	Open-Collector	5 (2.5) U.L.

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive must be supplied by an external resistor to V_{CC}.

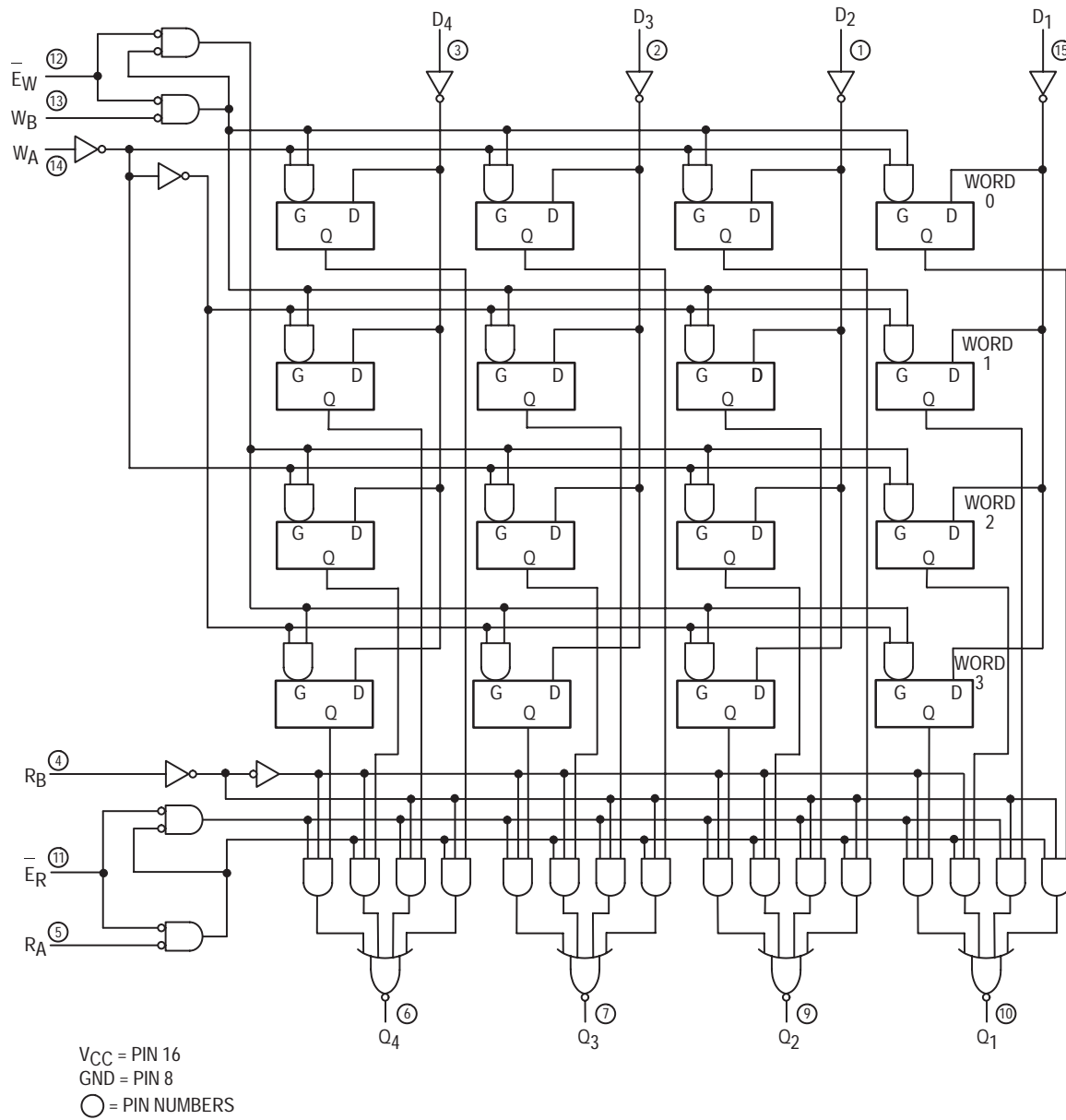
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS170

LOGIC DIAGRAM



SN54/74LS170

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W _B	W _A	E _W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R _B	R _A	E _R	Q ₁	Q ₂	Q ₃	Q ₄
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = HIGH Level. L = LOW Level. X = Irrelevant.

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q₀ = the level of Q before the indicated input conditions were established.

D. W_{0B1} = The first bit of word 0, etc.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54, 74		100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current Any <u>D</u> , R, W E _R , E _W			20 40	μA	V _{CC} = MAX, V _{IN} = 2.4 V
	Any <u>D</u> , R, W E _R , E _W			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Any <u>D</u> , R, W E _R , E _W			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current			40	mA	V _{CC} = MAX

SN54/74LS170

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going E_R to Q Outputs		20	30	ns	Figure 1 Figure 2 Figure 1 Figure 1 $V_{CC} = 5.0\text{ V}$ $C_L = 15\text{ pF}$ $R_L = 2.0\text{ k}\Omega$
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Q Outputs		25	40	ns	
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going E_W to Q Outputs		30	45	ns	
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to Q Outputs		30	45	ns	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Pulse Width, E_R , E_W	25			ns	$V_{CC} = 5.0\text{ V}$ $R_L = 2.0\text{ k}\Omega$
t_s	Setup Time, Data to E_W	10			ns	
t_s	Setup Time, W_A , W_B to E_W	15			ns	
t_h	Hold Time, Data to E_W	15			ns	
t_h	Hold Time, W_A , W_B to E_W	5.0			ns	
t_{LATCH}	Latch Time	25			ns	

VOLTAGE WAVEFORMS

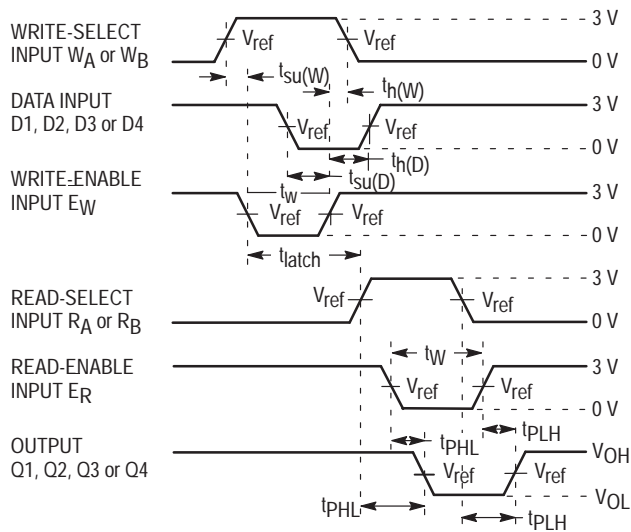


Figure 1

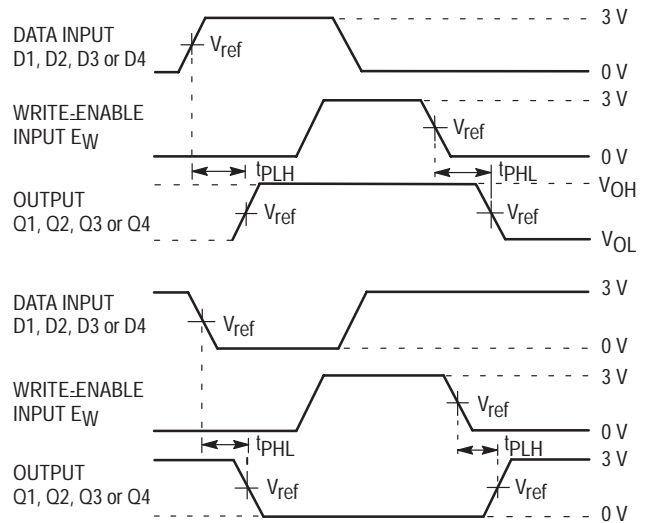


Figure 2

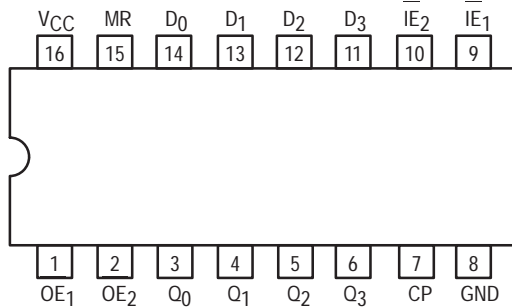


4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines (IE_1 , IE_2). A HIGH on either Output Enable line (OE_1 , OE_2) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable (OE_1 , OE_2) or the Input Enable (IE_1 , IE_2) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D_0 – D_3	Data Inputs
IE_1 – IE_2	Input Enable (Active LOW)
OE_1 – OE_2	Output Enable (Active LOW) Inputs
CP	Clock Pulse (Active HIGH Going Edge) Input
MR	Master Reset Input (Active HIGH)
Q_0 – Q_3	Outputs (Note b)

LOADING (Note a)

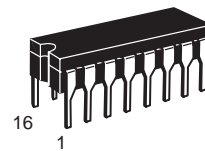
	HIGH	LOW
D_0 – D_3	0.5 U.L.	0.25 U.L.
IE_1 – IE_2	0.5 U.L.	0.25 U.L.
OE_1 – OE_2	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q_0 – Q_3	65 (25) U.L.	15 (7.5) U.L.

NOTES:

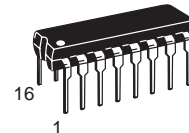
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS173A

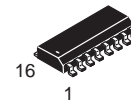
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

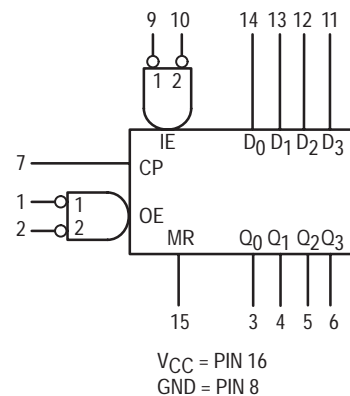


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

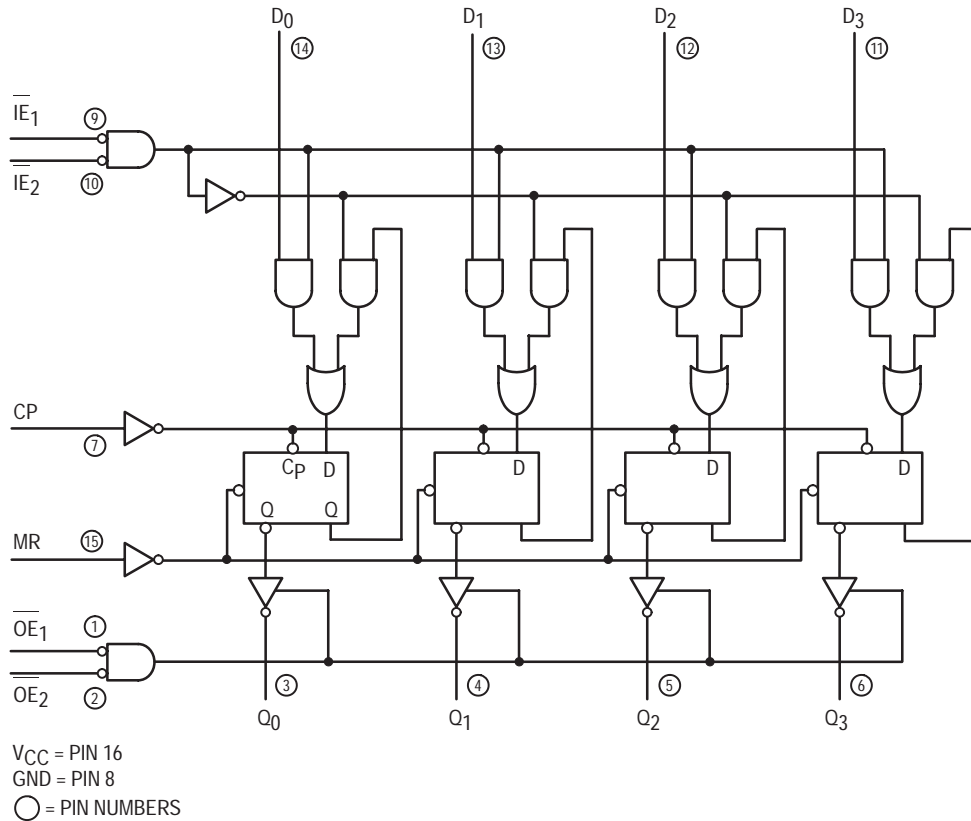
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS173A

LOGIC DIAGRAM



TRUTH TABLE

MR	CP	IE ₁	IE ₂	D _n	Q _n
H	x	x	x	x	L
L	L	x	x	x	Q _n
L	↯	H	x	x	Q _n
L	↯	x	H	x	Q _n
L	↯	L	L	L	L
L	↯	L	L	H	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

When either OE₁, or OE₂ are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-1.0	mA
74				-2.6		
I _{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS173A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.4	3.4	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.4	3.1	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74	0.35	0.5	V	
I_{OZH}	Output Off Current HIGH			20	μA	$V_{CC} = \text{MAX}$, $V_O = 2.7 \text{ V}$
I_{OZL}	Output Off Current LOW			-20	μA	$V_{CC} = \text{MAX}$, $V_O = 0.4 \text{ V}$
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			30	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Input Clock Frequency	30	50		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		17 22	25 30	ns	
		t_{PHL}	Propagation Delay, MR to Output	26	35	
t_{PZH} t_{PZL}	Output Enable Time		15 18	23 27	ns	
		t_{PLZ} t_{PHZ}	Output Disable Time	11 11	17 17	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock or MR Pulse Width	20			ns	$V_{CC} = 5.0 \text{ V}$
t_s	Data Enable Setup Time	35			ns	
t_s	Data Setup Time	17			ns	
t_h	Hold Time, Any Input	0			ns	
t_{rec}	Recovery Time	10			ns	

SN54/74LS173A

AC WAVEFORMS

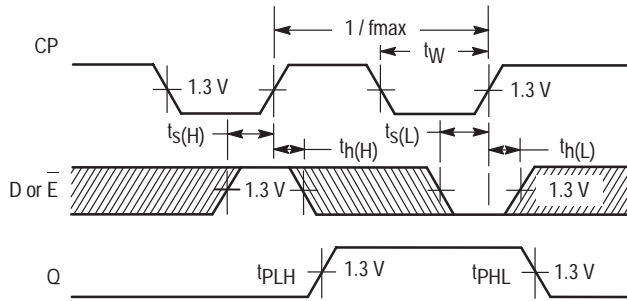


Figure 1

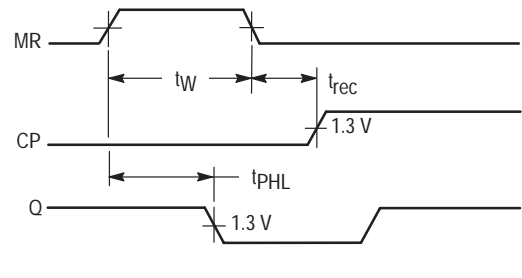


Figure 2

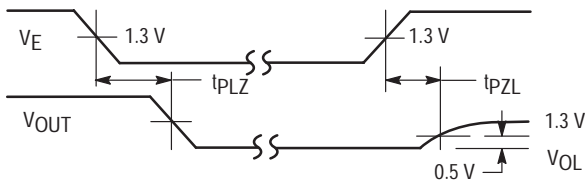


Figure 3

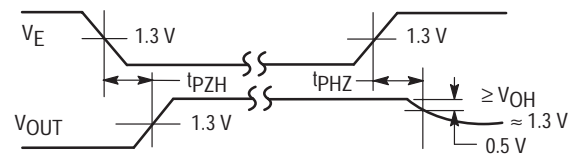
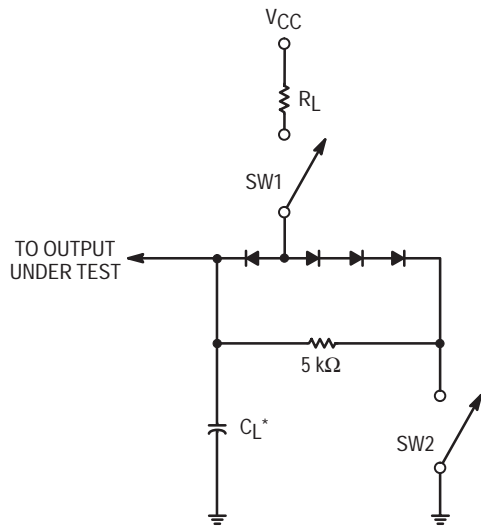


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

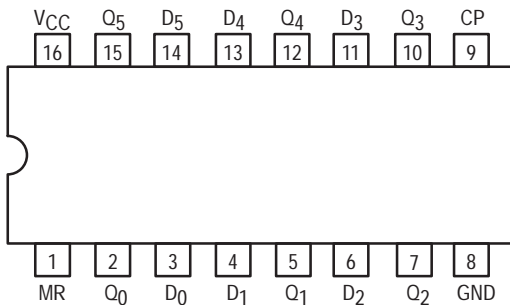
SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

HEX D FLIP-FLOP

The LSTTL/MSI SN54/74LS174 is a high speed Hex D Flip-Flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW to HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops. The LS174 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Asynchronous Common Reset
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D ₀ –D ₅	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ –Q ₅	Outputs (Note b)

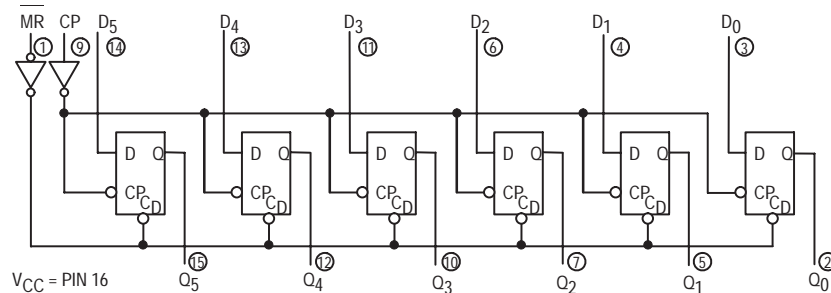
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

NOTES:

- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

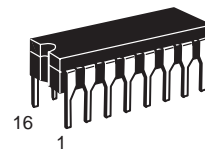
LOGIC DIAGRAM



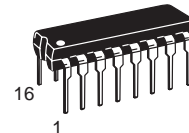
V_{CC} = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS174

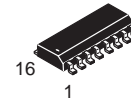
HEX D FLIP-FLOP LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

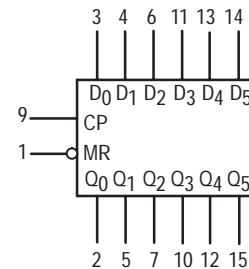


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS174

FUNCTIONAL DESCRIPTION

The LS174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{\text{MR}}$) will force all outputs LOW independent of Clock or Data inputs. The LS174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

TRUTH TABLE

Inputs (t = n, MR = H)	Outputs (t = n+1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			26	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS174

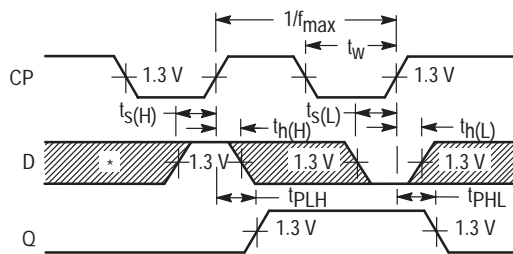
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency	30	40		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Propagation Delay, MR to Output		23	35	ns	
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		20 21	30 30	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock or MR Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	Data Setup Time	20			ns	
t _H	Data Hold Time	5.0			ns	
t _{rec}	Recovery Time	25			ns	

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

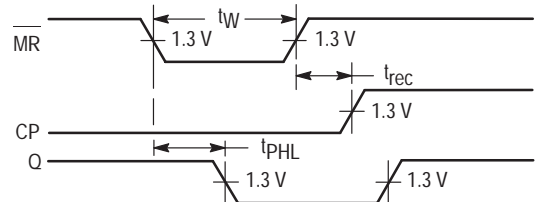


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.



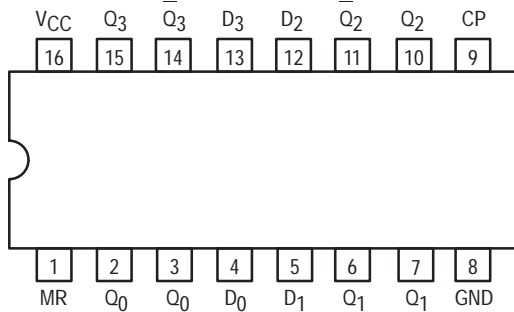
QUAD D FLIP-FLOP

The LSTTL/MSI SN54/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D ₀ –D ₃	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ –Q ₃	True Outputs (Note b)
Q̄ ₀ –Q̄ ₃	Complemented Outputs (Note b)

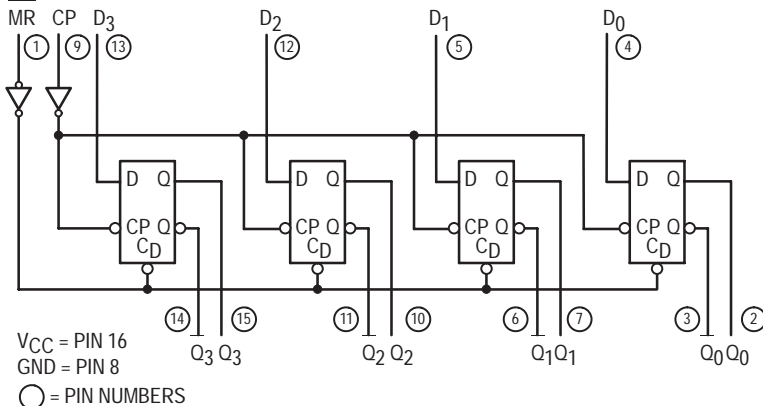
LOADING (Note a)

	HIGH	LOW
D ₀ –D ₃	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ –Q ₃	10 U.L.	5 (2.5) U.L.
Q̄ ₀ –Q̄ ₃	10 U.L.	5 (2.5) U.L.

NOTES:

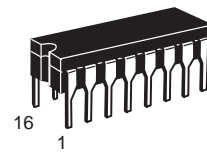
- 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

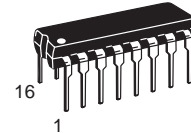


SN54/74LS175

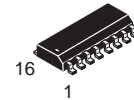
QUAD D FLIP-FLOP LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

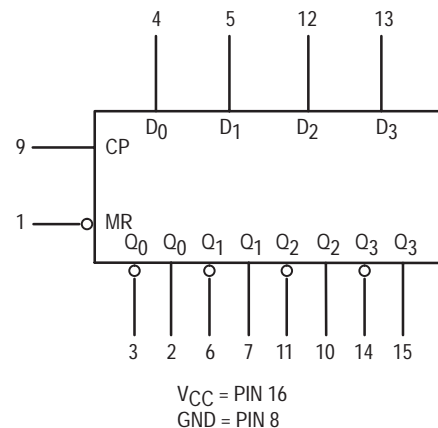


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS175

FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and \bar{Q} outputs to follow. A

LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \bar{Q} outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, MR = H)	Outputs (t = n+1) Note 1	
D	Q	\bar{Q}
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			18	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS175

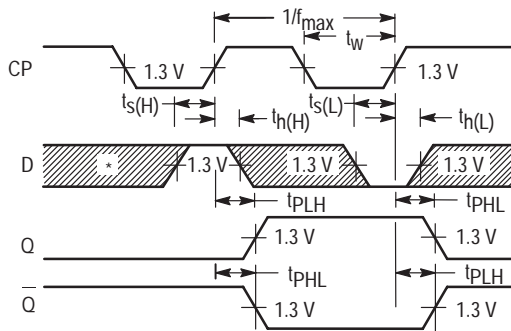
AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency	30	40		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, MR to Output		20 20	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		13 16	25 25	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock or MR Pulse Width	20			ns	V _{CC} = 5.0 V
t _s	Data Setup Time	20			ns	
t _h	Data Hold Time	5.0			ns	
t _{rec}	Recovery Time	25			ns	

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

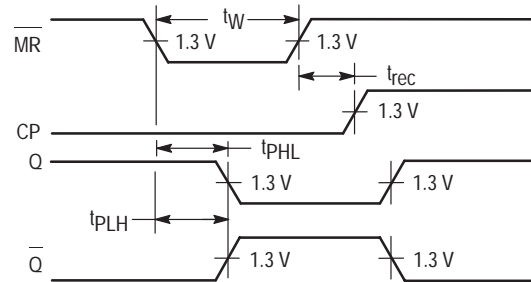


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recog-

niton. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

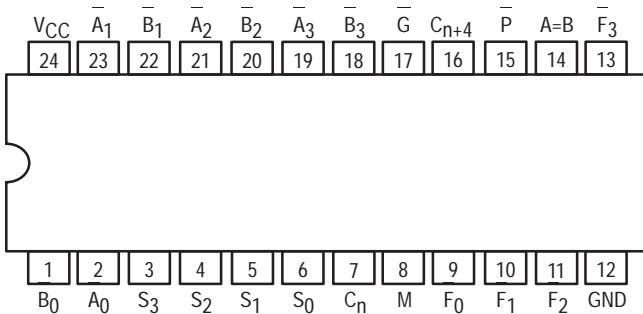


4-BIT ARITHMETIC LOGIC UNIT

The SN54/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables Exclusive — OR, Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations
- Full Lookahead for High Speed Arithmetic Operation on Long Words
- Input Clamp Diodes

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

\bar{A}_0 – \bar{A}_3 , \bar{B}_0 – \bar{B}_3	Operand (Active LOW) Inputs
\bar{S}_0 – \bar{S}_3	Function — Select Inputs
M	Mode Control Input
C_n	Carry Input
F_0 – F_3	Function (Active LOW) Outputs
$\bar{A} = \bar{B}$	Comparator Output
G	Carry Generator (Active LOW) Output
P	Carry Propagate (Active LOW) Output
C_{n+4}	Carry Output

LOADING (Note a)

	HIGH	LOW
\bar{A}_0 – \bar{A}_3 , \bar{B}_0 – \bar{B}_3	1.5 U.L.	0.75 U.L.
\bar{S}_0 – \bar{S}_3	2.0 U.L.	1.0 U.L.
M	0.5 U.L.	0.25 U.L.
C_n	2.5 U.L.	1.25 U.L.
F_0 – F_3	10 U.L.	5 (2.5) U.L.
$\bar{A} = \bar{B}$	Open Collector	5 (2.5) U.L.
G	10 U.L.	10 U.L.
P	10 U.L.	5 U.L.
C_{n+4}	10 U.L.	5 (2.5) U.L.

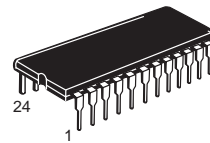
NOTES:

- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

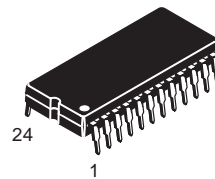
SN54/74LS181

4-BIT ARITHMETIC LOGIC UNIT

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 623-05

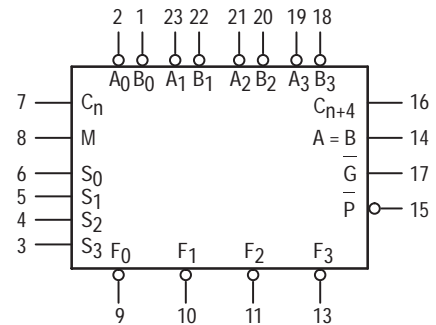


N SUFFIX
PLASTIC
CASE 649-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic

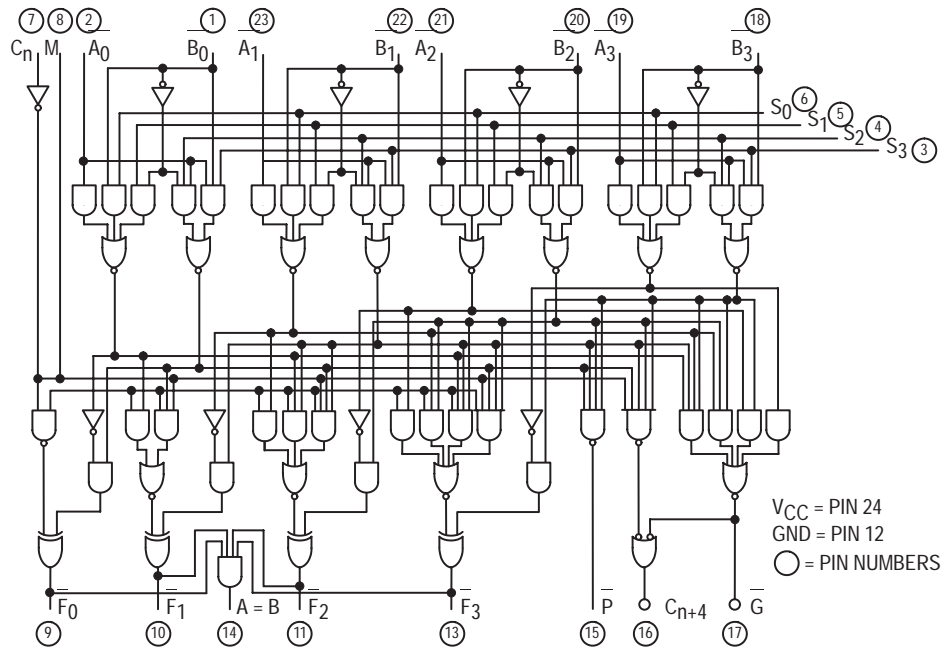
LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

SN54/74LS181

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \dots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate), P and G are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability

over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHH generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

SN54/74LS181

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	LOGIC (M = H)	ARITHMETIC** (M = L) (C _n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C _n = H)
L	L	L	L	\overline{A}	A minus 1	\overline{A}	A
L	L	L	H	\overline{AB}	\overline{AB} minus 1	$\overline{A + B}$	A + \overline{B}
L	L	H	L	A + \overline{B}	\overline{AB} minus 1	AB	A + B
L	L	H	H	$\overline{A + B}$	Logical 1 minus 1	\overline{A}	Logical 0 minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + \overline{B})	\overline{AB}	A plus AB
L	H	L	H	\overline{B}	AB plus (A + B)	B	(A + B) plus AB
L	H	H	L	$A \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$\overline{A + B}$	A + B	\overline{AB}	AB minus 1
H	L	L	L	AB	A plus (A + B)	$\overline{A + B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	AB plus (A + B)	B	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A*	Logical 1	A plus A*
H	H	L	H	AB	\overline{AB} plus A	A + B	(A + \overline{B}) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) Plus A
H	H	H	H	A	A	A	A minus 1

L = LOW Voltage Level

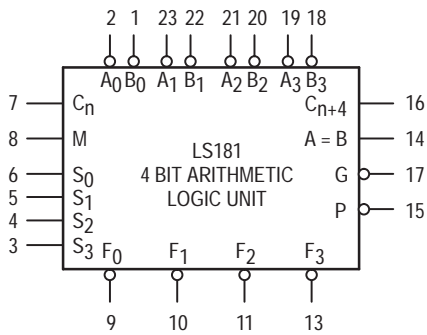
H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

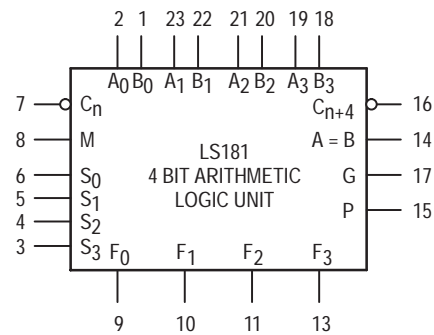
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA
V _{OH}	Output Voltage — High (A = B only)	54, 74			5.5	V

SN54/74LS181

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage Except G and P	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table	
		74		0.35	0.5	V		
	Output \bar{G}	54, 74			0.7	V		
	Output \bar{P}	54 74			0.6 0.5	V		
I_{OH}	Output HIGH Current		54, 74			100	μA	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
I_{IH}	Input HIGH Current Mode Input Any A or B Input Any S Input C_n Input					20 60 80 100	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
	Mode Input Any A or B Input Any S Input C_n Input					0.1 0.3 0.4 0.5	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current Mode Input Any A or B Input Any S Input C_n Input					-0.4 -1.2 -1.6 -2.0	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 2)		-20			-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current See Note 1A	54				32	mA	$V_{CC} = \text{MAX}$
		74				34		
	See Note 1B	54				35		
		74				37		

Note 1.

With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

Note 2: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS181

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, Pin 12 = GND, $C_L = 15\text{ pF}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, (C_n to C_{n+4})		18 13	27 20	ns	$M = 0\text{ V}$, (Sum or Diff Mode) See Fig. 4 and Tables I and II
t_{PLH} t_{PHL}	(C_n to \bar{F} Outputs)		17 13	26 20	ns	$M = 0\text{ V}$, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to \bar{G} Output)		19 15	29 23	ns	$M = S_1 = S_2 = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to \bar{G} Output)		21 21	32 32	ns	$M = S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to \bar{P} Output)		20 20	30 30	ns	$M = S_1 = S_2 = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to \bar{P} Output)		20 22	30 33	ns	$M = S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_X Output)		21 13	32 20	ns	$M = S_1 = S_2 = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_X Output)		21 21	32 32	ns	$M = S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 26	ns	$M = S_1 = S_2 = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$ (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	(A_X or B_X Inputs to F_{XH} Outputs)			38 38	ns	$M = S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to \bar{F} Outputs)		22 26	33 38	ns	$M = 4.5\text{ V}$ (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to C_{n+4} Output)		25 25	38 38	ns	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to C_{n+4} Output)		27 27	41 41	ns	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (Diff Mode)
t_{PLH} t_{PHL}	(\bar{A} or \bar{B} Inputs to $A = B$ Output)		33 41	50 62	ns	$M = S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ $R_L = 2.0\text{ k}\Omega$ (Diff Mode) See Fig. 5 and Table II

AC WAVEFORMS

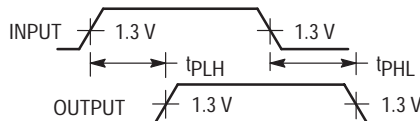


Figure 4

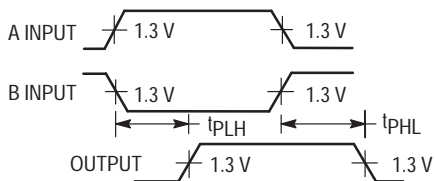


Figure 5

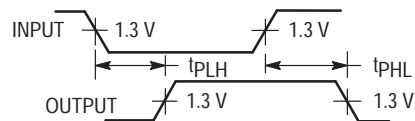


Figure 6

SN54/74LS181

SUM MODE TEST TABLE I
FUNCTION INPUTS: $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = M = 0\text{ V}$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	Remaining A and B	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining A and B	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	C _n	Remaining A and B	\bar{F}_{i+1}
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	C _n	Remaining A and B	\bar{F}_{i+1}
t _{PLH} t _{PHL}	\bar{A}	\bar{B}	None	None	Remaining A and B, C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{B}	\bar{A}	None	None	Remaining A and B, C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{A}	None	\bar{B}	Remaining B	Remaining A, C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{B}	None	\bar{A}	Remaining B	Remaining A, C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{A}	None	\bar{B}	Remaining B	Remaining A, C _n	C _{n+4}
t _{PLH} t _{PHL}	\bar{B}	None	\bar{A}	Remaining B	Remaining A, C _n	C _{n+4}
t _{PLH} t _{PHL}	C _n	None	None	All A	All B	Any F or C _{n+4}

SN54/74LS181

DIFF MODE TEST TABLE II
FUNCTION INPUTS: $S_1 = S_2 = 4.5\text{ V}$, $S_0 = S_3 = M = 0\text{ V}$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND	
t_{PLH} t_{PHL}	\bar{A}	None	\bar{B}	Remaining A	Remaining B, C_n	\bar{F}_l
t_{PLH} t_{PHL}	\bar{B}	\bar{A}	None	Remaining A	Remaining B, C_n	\bar{F}_l
t_{PLH} t_{PHL}	\bar{A}_l	None	\bar{B}_l	Remaining B, C_n	Remaining A	\bar{F}_{l+1}
t_{PLH} t_{PHL}	\bar{B}_l	\bar{A}_l	None	Remaining B, C_n	Remaining A	\bar{F}_{l+1}
t_{PLH} t_{PHL}	\bar{A}	None	\bar{B}	None	Remaining A and B, C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}	\bar{A}	None	None	Remaining A and B, C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}	\bar{B}	None	None	Remaining A and B_l , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}	None	\bar{A}	None	Remaining A and B, C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}	None	\bar{B}	Remaining A	Remaining B, C_n	A = B
t_{PLH} t_{PHL}	\bar{B}	\bar{A}	None	Remaining A	Remaining B, C_n	A = B
t_{PLH} t_{PHL}	\bar{A}	\bar{B}	None	None	Remaining A and B, C_n	C_{n+4}
t_{PLH} t_{PHL}	\bar{B}	None	\bar{A}	None	Remaining A and B, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_{n+4}

LOGIC MODE TEST TABLE III

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Function Inputs
		Apply 4.5 V	Apply GND	Apply 4.5 V	Apply GND		
t_{PLH} t_{PHL}	\bar{A}	None	\bar{B}	None	Remaining A and B, C_n	Any \bar{F}	$S_1 = S_2 = M = 4.5\text{ V}$ $S_0 = S_3 = 0\text{ V}$
t_{PLH} t_{PHL}	\bar{B}	None	\bar{A}	None	Remaining A and B, C_n	Any \bar{F}	$S_1 = S_2 = M = 4.5\text{ V}$ $S_0 = S_3 = 0\text{ V}$



PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

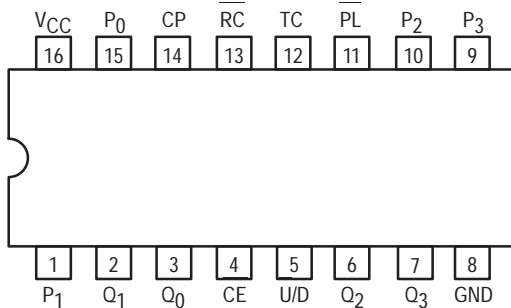
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

The SN54/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load (PL) input overrides counting and loads the data present on the P_n inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable (CE) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control (U/D) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock (RC) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multistage counter applications.

- Low Power . . . 90 mW Typical Dissipation
- High Speed . . . 25 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Individual Preset Inputs
- Count Enable and Up/Down Control Inputs
- Cascadable
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

CE	Count Enable (Active LOW) Input
CP	Clock Pulse (Active HIGH going edge) Input
U/D	Up/Down Count Control Input
PL	Parallel Load Control (Active LOW) Input
P _n	Parallel Data Inputs
Q _n	Flip-Flop Outputs (Note b)
RC	Ripple Clock Output (Note b)
TC	Terminal Count Output (Note b)

NOTES:

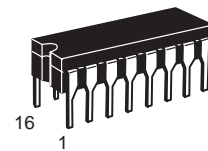
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)

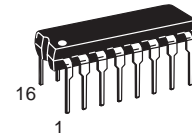
	HIGH	LOW
CE	1.5 U.L.	0.7 U.L.
CP	0.5 U.L.	0.25 U.L.
U/D	0.5 U.L.	0.25 U.L.
PL	0.5 U.L.	0.25 U.L.
P _n	0.5 U.L.	0.25 U.L.
Q _n	10 U.L.	5 (2.5) U.L.
RC	10 U.L.	5 (2.5) U.L.
TC	10 U.L.	5 (2.5) U.L.

SN54/74LS190 SN54/74LS191

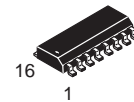
PRESETTABLE BCD/DECADE
UP/DOWN COUNTERS
PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTERS
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

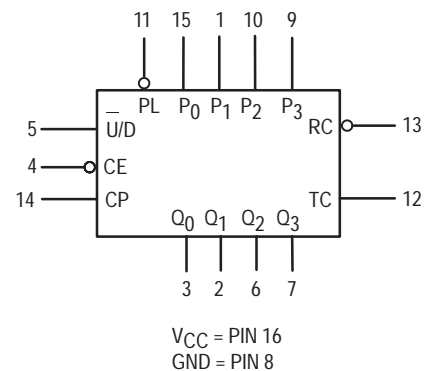


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

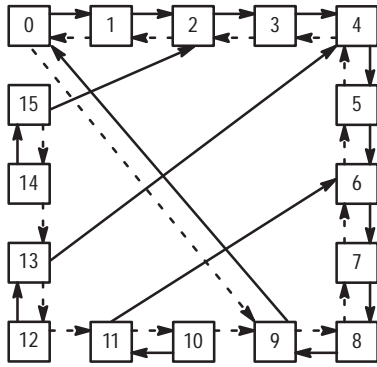
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS190 • SN54/74LS191

STATE DIAGRAMS

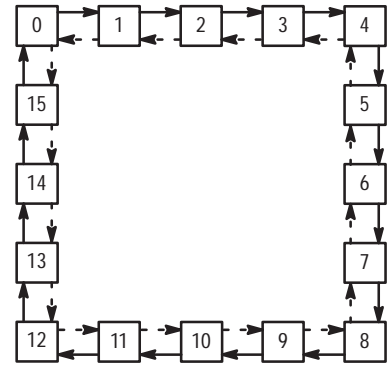


LS190

LS190
 UP: $TC = Q_0 \cdot Q_3 \cdot \overline{(U/D)}$
 DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

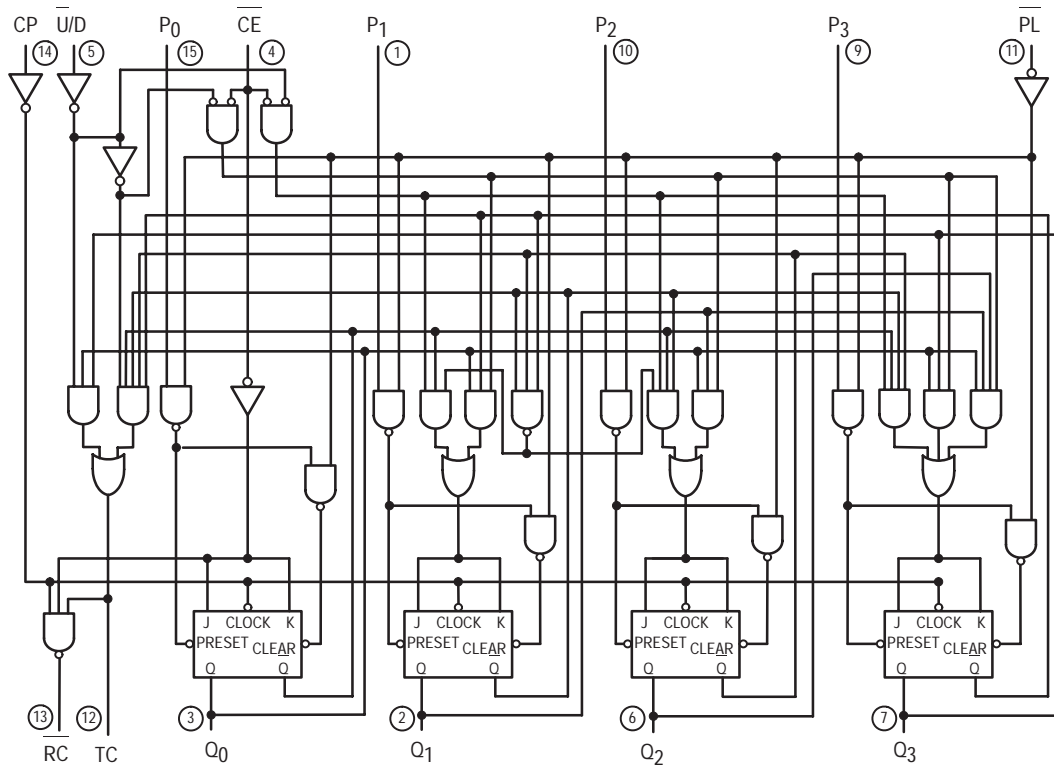
LS191
 UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{(U/D)}$
 DOWN: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

COUNT UP ———
 COUNT DOWN - - - - -



LS191

LOGIC DIAGRAMS

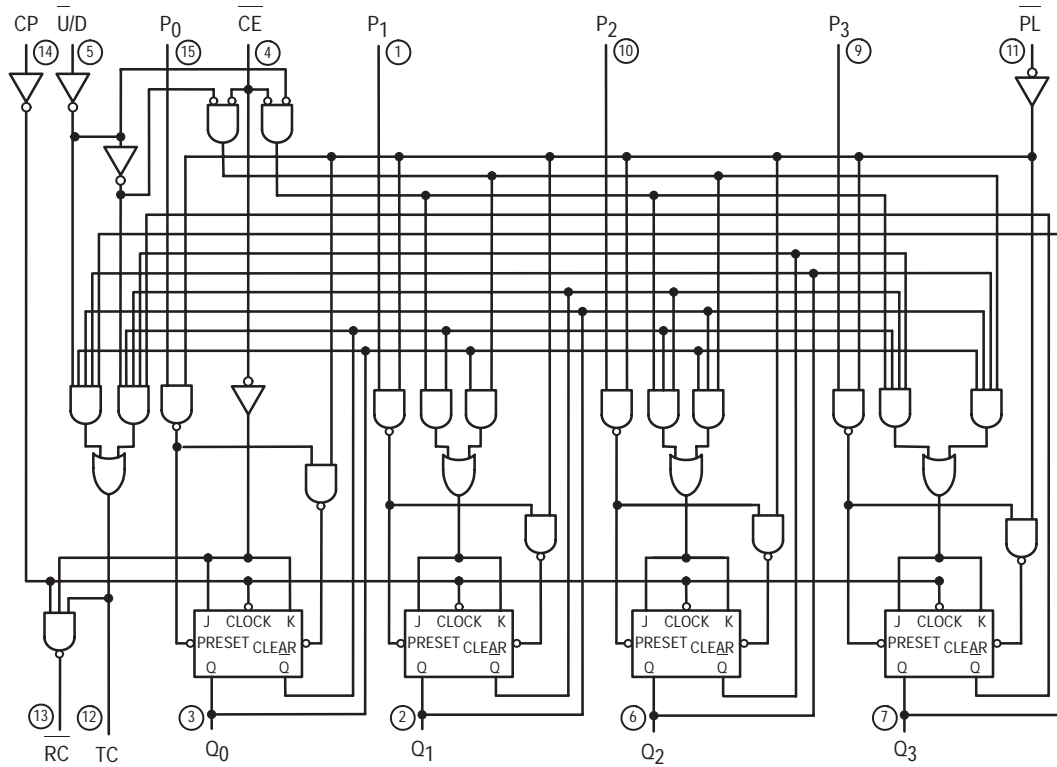


DECADE COUNTER
 LS190

V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

SN54/74LS190 • SN54/74LS191

LOGIC DIAGRAMS (continued)



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

**BINARY COUNTER
 LS191**

SN54/74LS190 • SN54/74LS191

FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Data inputs (P₀–P₃) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the CE input inhibits counting. When CE is LOW, internal state change are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the U/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the CE signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH CE transition must occur only while the clock is HIGH. Similarly, the U/D signal should only be changed when either CE or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.



The TC signal is also used internally to enable the Ripple

Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, the RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.



A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the RC outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stop before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The CE input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own CE.



MODE SELECT TABLE

INPUTS				MODE
PL	CE	U/D	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			RC OUTPUT
CE	TC*	CP	
L	H		
H	X	X	H
X	L	X	H

* TC is generated internally

- L = LOW Voltage Level
- H = HIGH Voltage Level
- X = Don't Care
-  = LOW-to-HIGH Clock Transition
-  = LOW Pulse

SN54/74LS190 • SN54/74LS191

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current Other Inputs CE			20 60	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Other Inputs CE			0.1 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Other Inputs CE			-0.4 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			35	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS190 • SN54/74LS191

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	20	25		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, PL to Output Q		22 33	33 50	ns	
t _{PLH} t _{PHL}	Data to Output Q		20 27	32 40	ns	
t _{PLH} t _{PHL}	Clock to $\overline{\text{RC}}$		13 16	20 24	ns	
t _{PLH} t _{PHL}	Clock to Output Q		16 24	24 36	ns	
t _{PLH} t _{PHL}	Clock to TC		28 37	42 52	ns	
t _{PLH} t _{PHL}	$\overline{\text{U/D}}$ to $\overline{\text{RC}}$		30 30	45 45	ns	
t _{PLH} t _{PHL}	$\overline{\text{U/D}}$ to TC		21 22	33 33	ns	
t _{PLH} t _{PHL}	$\overline{\text{CE}}$ to $\overline{\text{RC}}$		21 22	33 33	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	CP Pulse Width	25			ns	V _{CC} = 5.0 V
t _W	PL Pulse Width	35			ns	
t _S	Data Setup Time	20			ns	
t _H	Data Hold Time	5.0			ns	
t _{rec}	Recovery Time	40			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_S) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recogni-

tion. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

SN54/74LS190 • SN54/74LS191

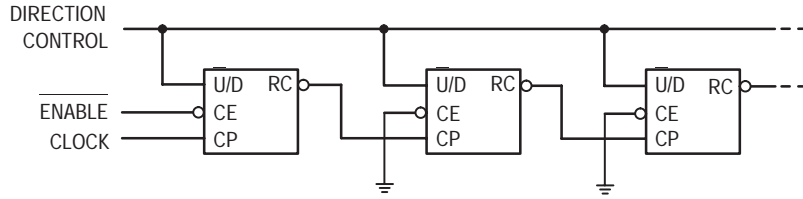


Figure a. n-Stage Counter Using Ripple Clock

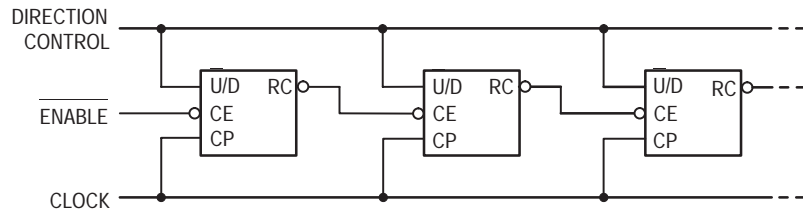


Figure b. Synchronous n-Stage Counter Using Ripple Carry/Borrow

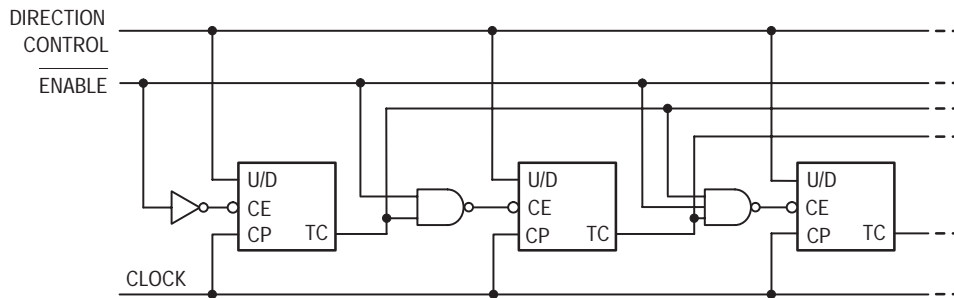


Figure c. Synchronous n-Stage Counter with Parallel Gated Carry/Borrow

SN54/74LS190 • SN54/74LS191

AC WAVEFORMS

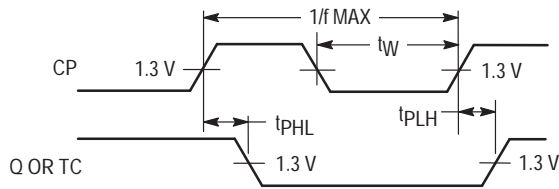


Figure 1

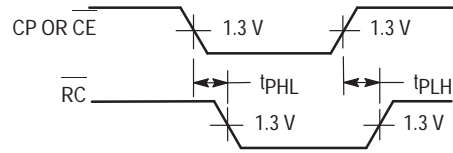
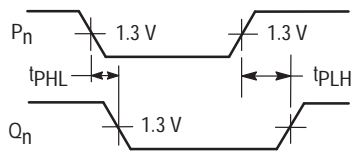


Figure 2



NOTE: PL = LOW

Figure 3

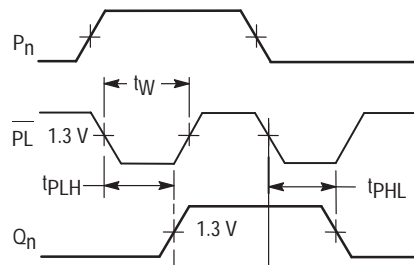


Figure 4

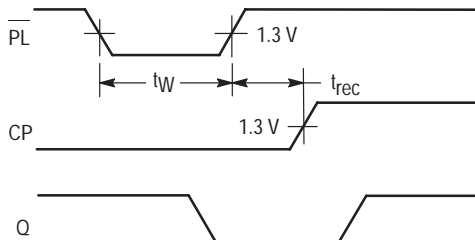
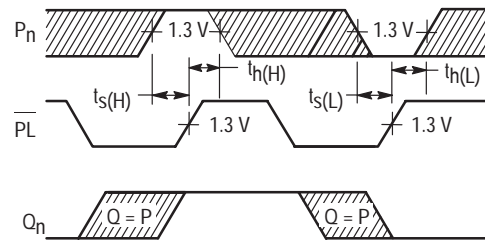


Figure 5



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6

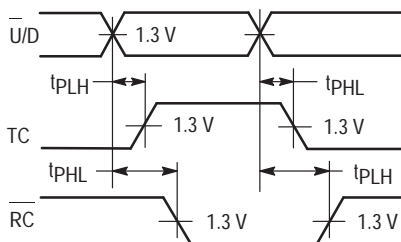


Figure 7

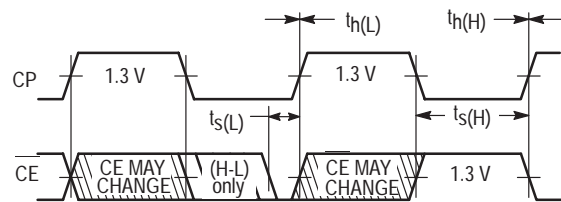


Figure 8



PRESETTABLE BCD/DECADE UP/DOWN COUNTER

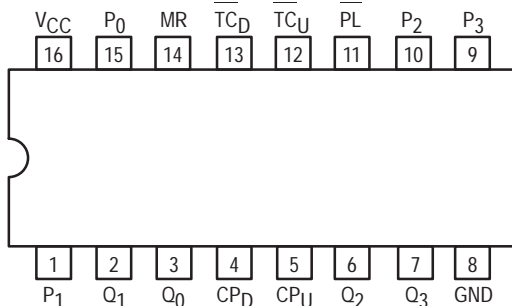
PRESETTABLE 4-BIT BINARY UP/DOWN COUNTER

The SN54/74LS192 is an UP/DOWN BCD Decade (8421) Counter and the SN54/74LS193 is an UP/DOWN MODULO-16 Binary Counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

- Low Power . . . 95 mW Typical Dissipation
- High Speed . . . 40 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Master Reset and Parallel Load
- Individual Preset Inputs
- Cascading Circuitry Internally Provided
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

CP _U	Count Up Clock Pulse Input
CP _D	Count Down Clock Pulse Input
MR	Asynchronous Master Reset (Clear) Input
PL	Asynchronous Parallel Load (Active LOW) Input
P _n	Parallel Data Inputs
Q _n	Flip-Flop Outputs (Note b)
TC _D	Terminal Count Down (Borrow) Output (Note b)
TC _U	Terminal Count Up (Carry) Output (Note b)

LOADING (Note a)

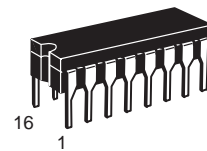
	HIGH	LOW
CP _U	0.5 U.L.	0.25 U.L.
CP _D	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
PL	0.5 U.L.	0.25 U.L.
P _n	0.5 U.L.	0.25 U.L.
Q _n	10 U.L.	5 (2.5) U.L.
TC _D	10 U.L.	5 (2.5) U.L.
TC _U	10 U.L.	5 (2.5) U.L.

NOTES:

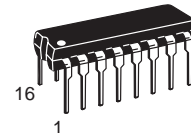
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS192 SN54/74LS193

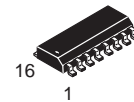
PRESETTABLE BCD/DECADE
UP/DOWN COUNTER
PRESETTABLE 4-BIT BINARY
UP/DOWN COUNTER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

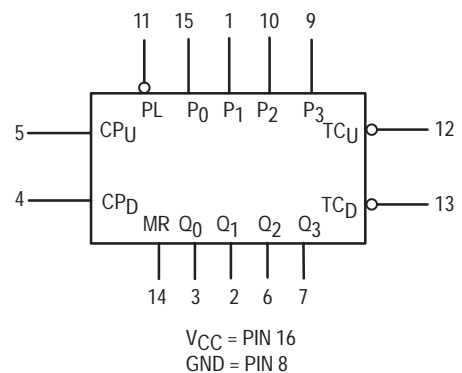


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

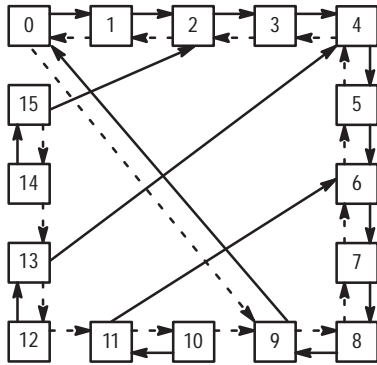
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS192 • SN54/74LS193

STATE DIAGRAMS



LS192

LS192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC_U} = Q_0 \cdot Q_3 \cdot \overline{CP_U}$$

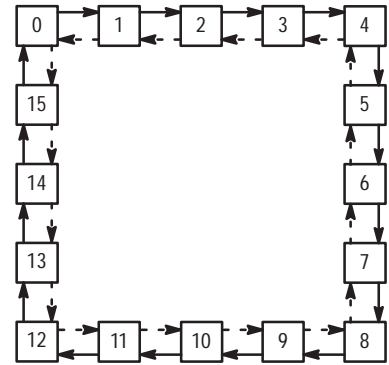
$$TC_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CP_D$$

LS193 LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC_U} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

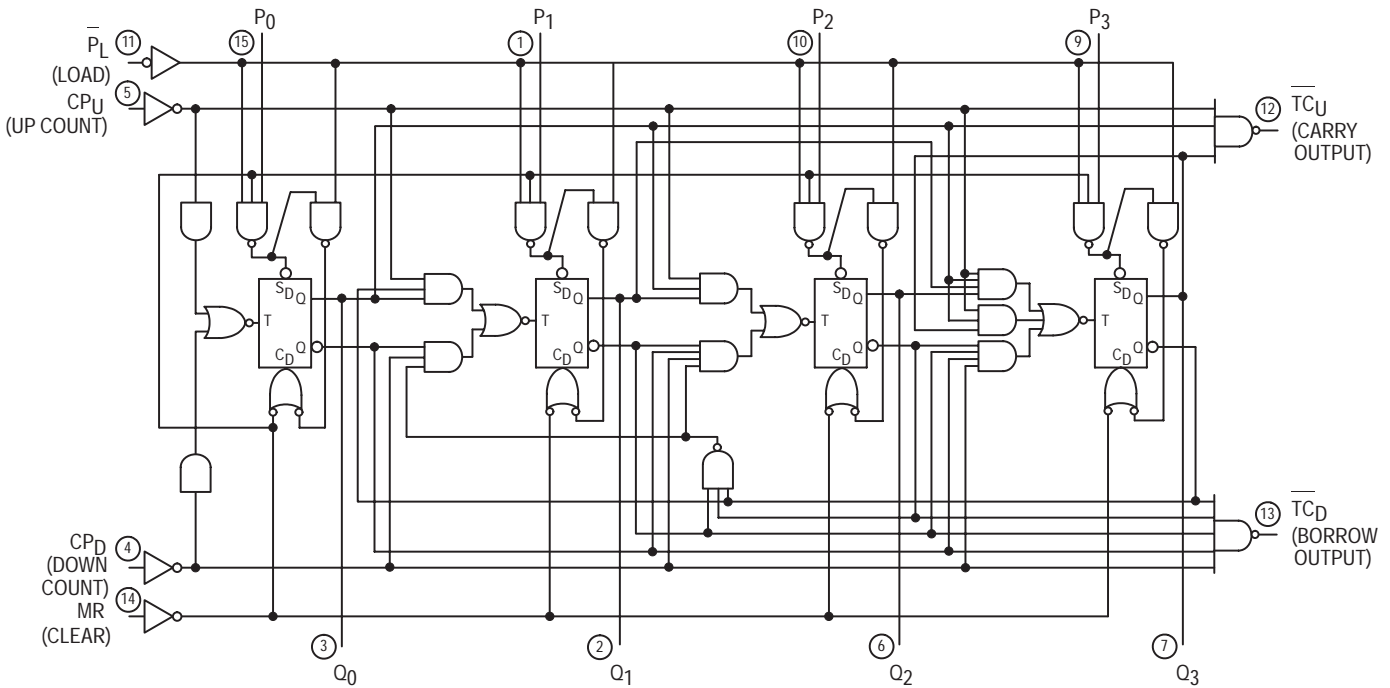
$$TC_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CP_D$$

COUNT UP ———
COUNT DOWN - - - - -



LS193

LOGIC DIAGRAMS

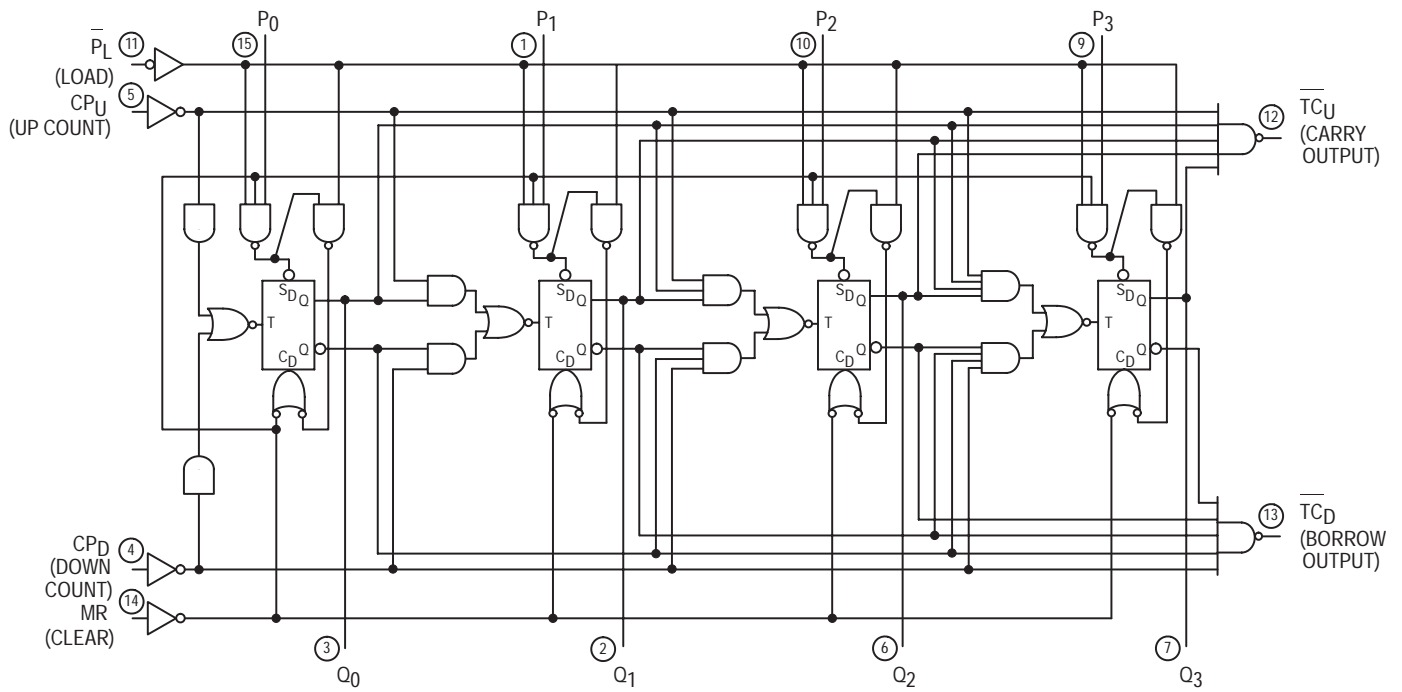


LS192

VCC = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS192 • SN54/74LS193

LOGIC DIAGRAMS (continued)



LS193

V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

SN54/74LS192 • SN54/74LS193

FUNCTIONAL DESCRIPTION

The LS192 and LS193 are Asynchronously Presettable Decade and 4-Bit Binary Synchronous UP/DOWN (Reversible) Counters. The operating modes of the LS192 decade counter and the LS193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC_U}$) and Terminal Count Down ($\overline{TC_D}$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the LS192, 15 for the LS193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC_U}$ to go LOW. $\overline{TC_U}$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC_D}$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the TC outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load (PL) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P_0, P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

MODE SELECT TABLE

MR	PL	CP _U	CP _D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌋	H	Count Up
L	H	H	⌋	Count Down

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

⌋ = LOW-to-HIGH Clock Transition

SN54/74LS192 • SN54/74LS193

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			34	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	32		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	$\overline{CP_U}$ Input to TC _U Output		17 18	26 24	ns	
t _{PLH} t _{PHL}	$\overline{CP_D}$ Input to TC _D Output		16 15	24 24	ns	
t _{PLH} t _{PHL}	Clock to Q		27 30	38 47	ns	
t _{PLH} t _{PHL}	\overline{PL} to Q		24 25	40 40	ns	
t _{PHL}	MR Input to Any Output		23	35	ns	

SN54/74LS192 • SN54/74LS193

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Any Pulse Width	20			ns	$V_{CC} = 5.0\text{ V}$
t_s	Data Setup Time	20			ns	
t_h	Data Hold Time	5.0			ns	
t_{rec}	Recovery Time	40			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the PL transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the PL transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recogni-

tion. A negative HOLD TIME indicates that the correct logic level may be released prior to the PL transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

SN54/74LS192 • SN54/74LS193

AC WAVEFORMS

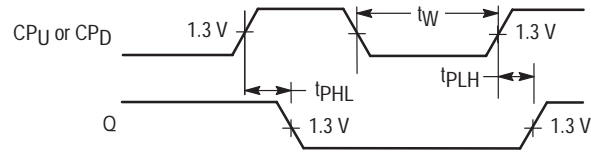


Figure 1

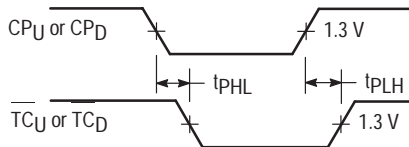
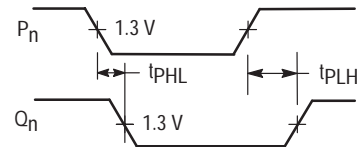


Figure 2



NOTE: PL = LOW

Figure 3

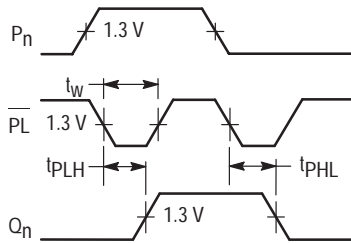


Figure 4

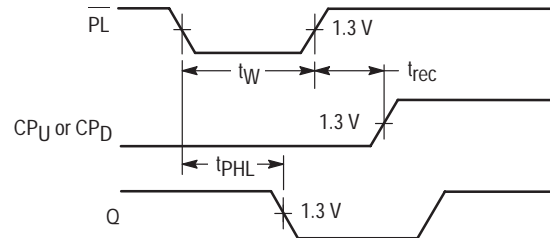
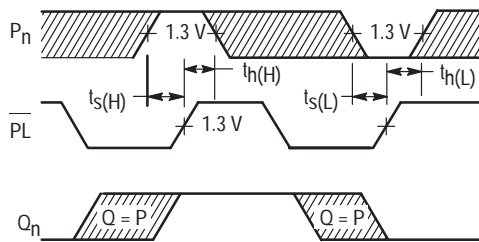


Figure 5



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 6

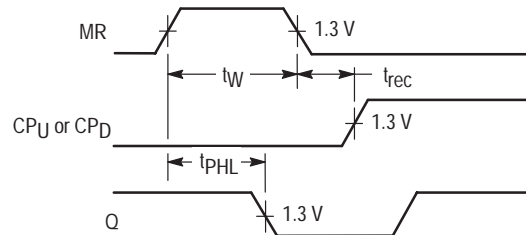


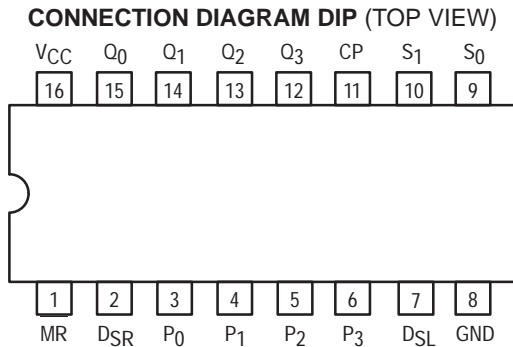
Figure 7



4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The SN54/74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL families.

- Typical Shift Frequency of 36 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects



PIN NAMES

S ₀ , S ₁	Mode Control Inputs
P ₀ –P ₃	Parallel Data Inputs
DSR	Serial (Shift Right) Data Input
DSL	Serial (Shift Left) Data Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ –Q ₃	Parallel Outputs (Note b)

LOADING (Note a)

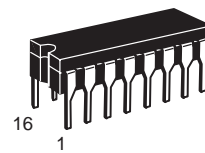
	HIGH	LOW
S ₀ , S ₁	0.5 U.L.	0.25 U.L.
P ₀ –P ₃	0.5 U.L.	0.25 U.L.
DSR	0.5 U.L.	0.25 U.L.
DSL	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ –Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

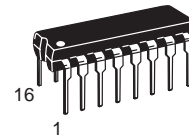
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS194A

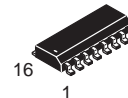
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



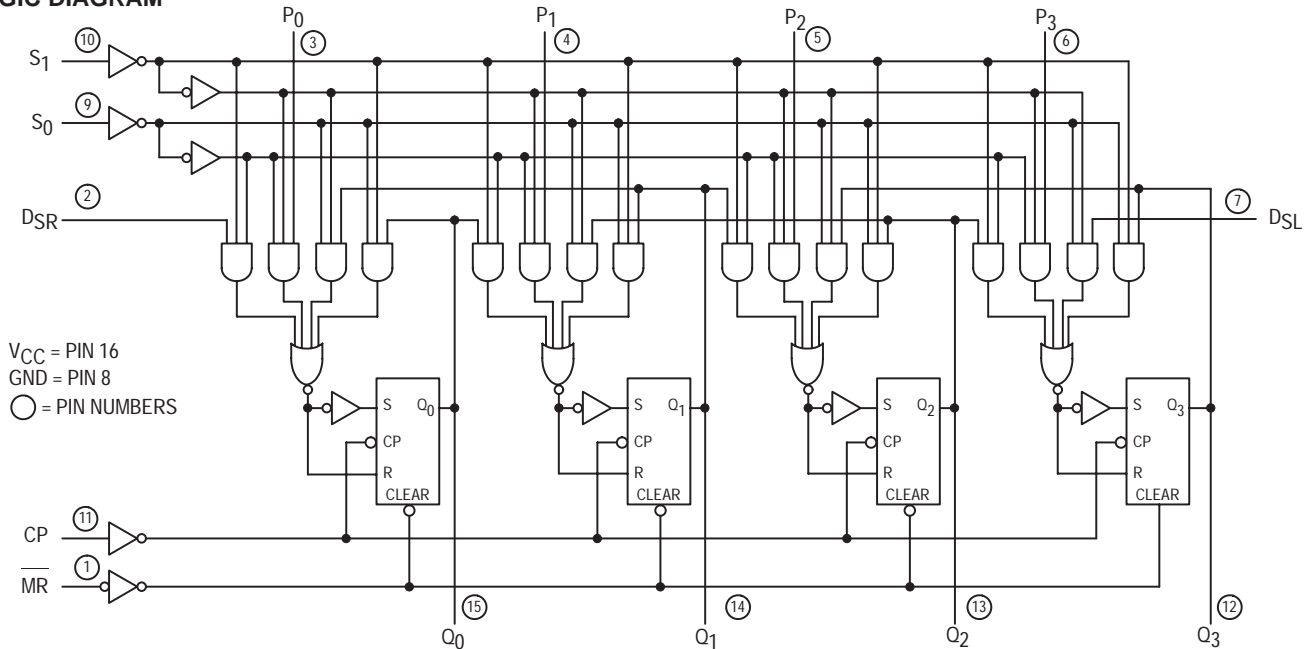
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS194A

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the Motorola LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

The four parallel data inputs (P_0 , P_1 , P_2 , P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0 , P_1 , P_2 , and P_3 inputs is transferred to the Q_0 , Q_1 , Q_2 , and

Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

The asynchronous Master Reset (\overline{MR}), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

Two mode control inputs (S_0 , S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

D-type serial data inputs (DSR , DSL) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	MR	S_1	S_0	DSR	DSL	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	P_n	P_0	P_1	P_2	P_3

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

P_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

SN54/74LS194A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			23	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	36		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		14 17	22 26	ns	
t _{PHL}	Propagation Delay, MR to Output		19	30	ns	

SN54/74LS194A

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock or MR Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	Mode Control Setup Time	30			ns	
t _S	Data Setup Time	20			ns	
t _H	Hold time, Any Input	0			ns	
t _{rec}	Recovery Time	25			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

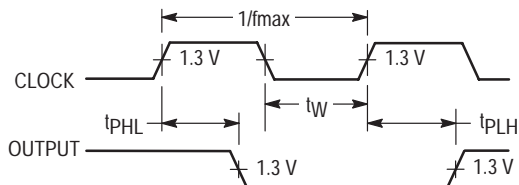
HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

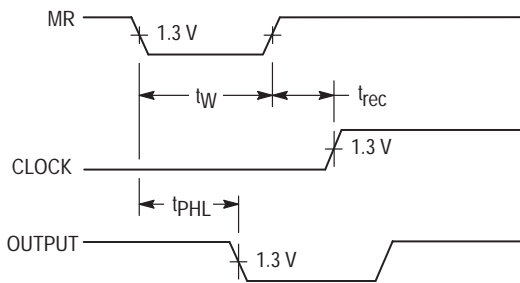
AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



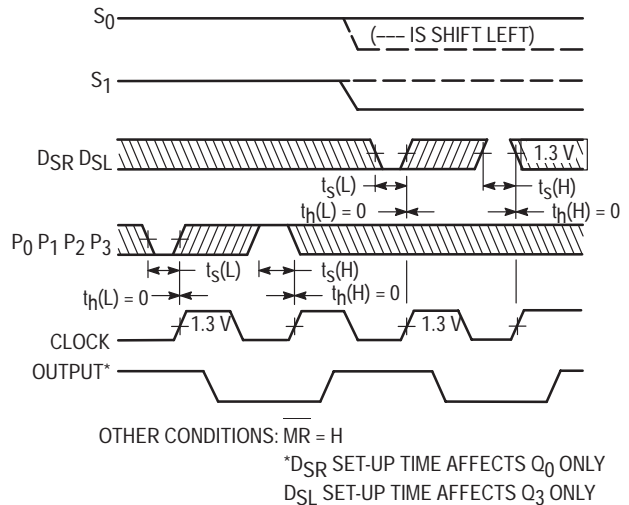
OTHER CONDITIONS: S₁ = L, MR = H, S₀ = H

Figure 1. Clock to Output Delays Clock Pulse Width and f_{max}



OTHER CONDITIONS: S₀, S₁ = H
P₀ = P₁ = P₂ = P₃ = H

Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

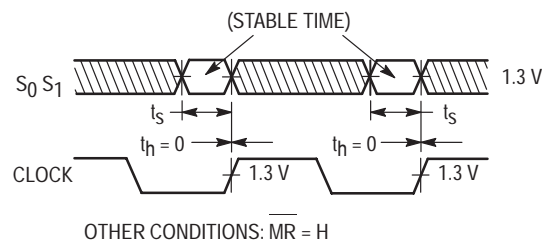


OTHER CONDITIONS: MR = H

*DSR SET-UP TIME AFFECTS Q₀ ONLY

DSL SET-UP TIME AFFECTS Q₃ ONLY

Figure 3. Setup (t_S) and Hold (t_H) Time for Serial Data (DSR, DSL) and Parallel Data (P₀, P₁, P₂, P₃)



OTHER CONDITIONS: MR = H

Figure 4. Setup (t_S) and Hold (t_H) Time for S Input

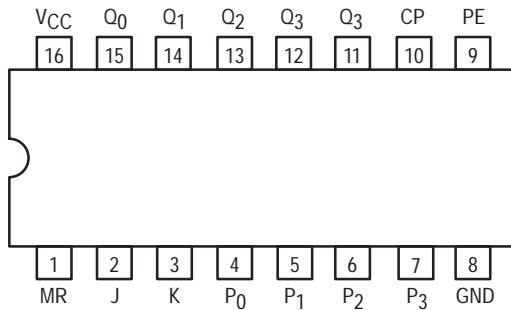


UNIVERSAL 4-BIT SHIFT REGISTER

The SN54/74LS195A is a high speed 4-Bit Shift Register offering typical shift frequencies of 39 MHz. It is useful for a wide variety of register and counting applications. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all Motorola TTL products.

- Typical Shift Right Frequency of 39 MHz
- Asynchronous Master Reset
- J, K Inputs to First Stage
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

PE	Parallel Enable (Active LOW) Input
P ₀ – P ₃	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
K	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
Q ₀ – Q ₃	Parallel Outputs (Note b)
Q ₃	Complementary Last Stage Output (Note b)

LOADING (Note a)

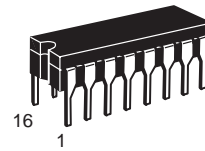
	HIGH	LOW
PE	0.5 U.L.	0.25 U.L.
P ₀ – P ₃	0.5 U.L.	0.25 U.L.
J	0.5 U.L.	0.25 U.L.
K	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ – Q ₃	10 U.L.	5 (2.5) U.L.
Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

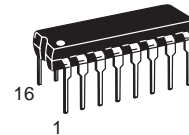
- a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS195A

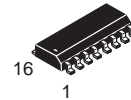
UNIVERSAL 4-BIT
SHIFT REGISTER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

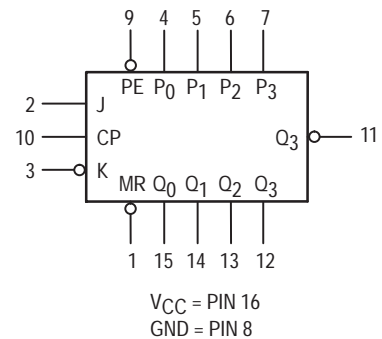


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

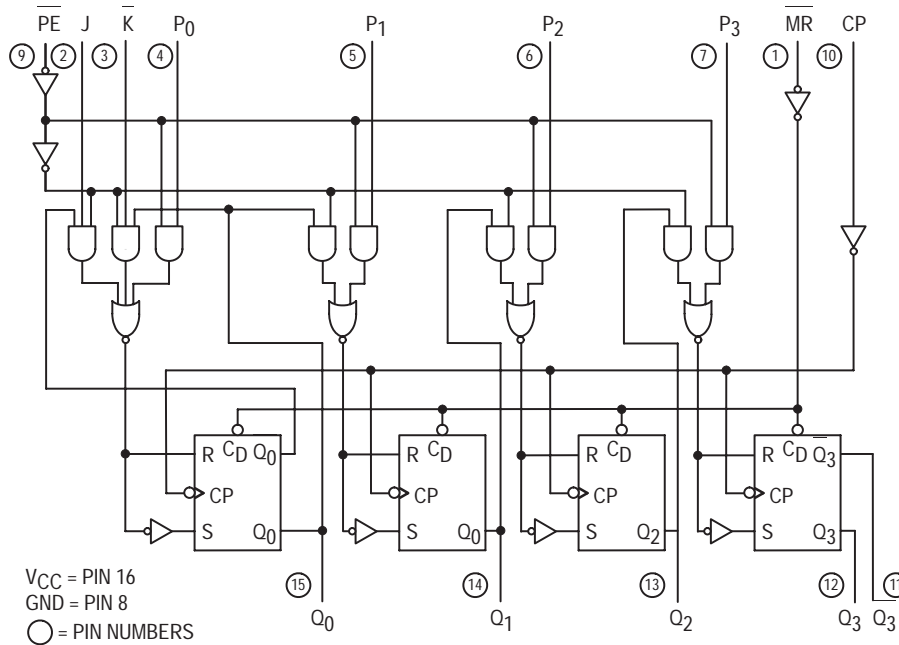
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS195A

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A 4-Bit Shift Register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load which are controlled by the state of the Parallel Enable (PE) input. When the PE input is HIGH, serial data enters the first flip-flop Q_0 via the J and K inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \Rightarrow Q_2 \rightarrow Q_3$ following each LOW to HIGH clock transition. The JK inputs provide the flexibility of the JK type input for special applications, and the simple D type input for general applications by tying the two

pins together. When the \overline{MR} input is LOW, the LS195A appears as four common clocked D flip-flops. The data on the parallel inputs P_0, P_1, P_2, P_3 is transferred to the respective Q_0, Q_1, Q_2, Q_3 outputs following the LOW to HIGH clock transition. Shift left operations ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n Outputs to the P_{n-1} inputs and holding the PE input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K, P_n and PE inputs for logic operation — except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset (MR) input sets all Q outputs LOW, independent of any other input condition.

MODE SELECT — TRUTH TABLE

OPERATING MODES	INPUTS					OUTPUTS				
	MR	PE	J	K	P_n	Q_0	Q_1	Q_2	Q_3	Q_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q_0	q_1	q_2	q_2
Shift, Reset First	H	h	l	l	X	\underline{L}	q_0	q_1	q_2	q_2
Shift, Toggle First Stage	H	h	h	l	X	q_0	q_0	q_1	q_2	q_2
Shift, Retain First Stage	H	h	l	h	X	q_0	q_0	q_1	q_2	q_2
Parallel Load	H	l	X	X	p_n	p_0	p_1	p_2	p_3	p_3

L = LOW voltage levels

H = HIGH voltage levels

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition.

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition.

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

SN54/74LS195A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			21	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	39		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output		14 17	22 26	ns	
t _{PHL}	Propagation Delay, MR to Output		19	30	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	CP Clock Pulse Width	16			ns	V _{CC} = 5.0 V
t _W	MR Pulse Width	12			ns	
t _S	PE Setup Time	25			ns	
t _S	Data Setup Time	15			ns	
t _{rec}	Recovery Time	25			ns	
t _{rel}	PE Release Time			10	ns	
t _H	Data Hold Time	0			ns	

SN54/74LS195A

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

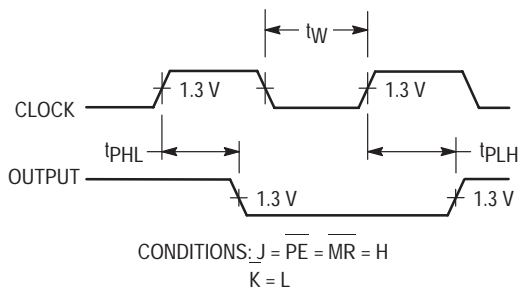


Figure 1. Clock to Output Delays and Clock Pulse Width

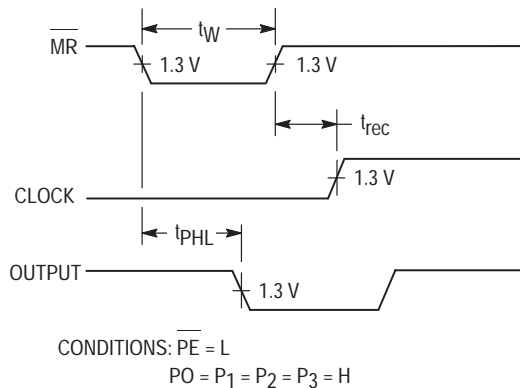


Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

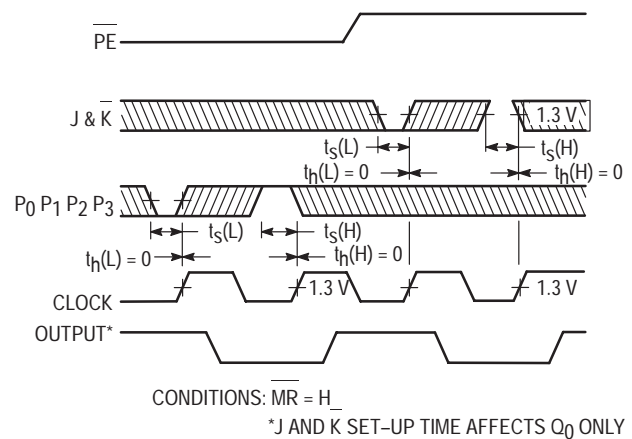


Figure 3. Setup (t_s) and Hold (t_h) Time for Serial Data (J & K) and Parallel Data (P_0 , P_1 , P_2 , P_3)

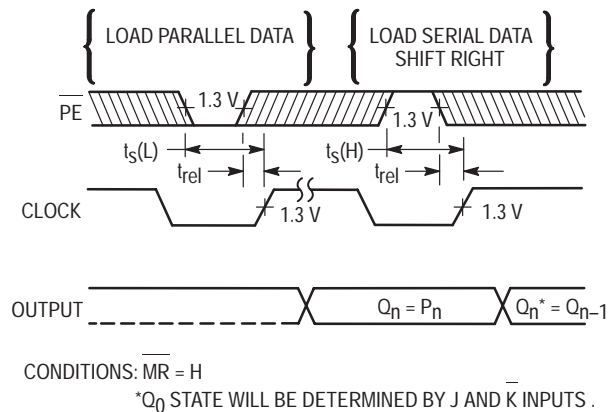


Figure 4. Setup (t_s) and Hold (t_h) Time for PE Input



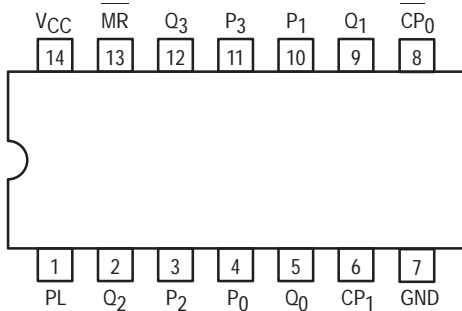
4-STAGE PRESETTABLE RIPPLE COUNTERS

The SN54/74LS196 decade counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8, 4, 2, 1) sequence or in a bi-quinary mode producing a 50% duty cycle output. The SN54/74LS197 contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. Low Power Schottky technology is used to achieve typical count rates of 70 MHz and power dissipation of only 80 mW.

Both circuit types have a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (PL) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when PL is LOW and storing the data when PL is HIGH.

- Low Power Consumption — Typically 80 mW
- High Counting Rates — Typically 70 MHz
- Choice of Counting Modes — BCD, Bi-Quinary, Binary
- Asynchronous Presettable
- Asynchronous Master Reset
- Easy Multistage Cascading
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

$\overline{CP_0}$	Clock (Active LOW Going Edge)
$\overline{CP_1}$ (LS196)	Input to Divide-by-Two Section
$\overline{CP_1}$ (LS197)	Input to Divide-by-Five Section
\overline{MR}	Master Reset (Active LOW) Input
PL	Parallel Load (Active LOW) Input
P_0 – P_3	Data Inputs
Q_0 – Q_3	Outputs (Notes b, c)

LOADING (Note a)

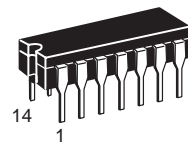
	HIGH	LOW
$\overline{CP_0}$	1.0 U.L.	1.5 U.L.
$\overline{CP_1}$ (LS196)	2.0 U.L.	1.75 U.L.
$\overline{CP_1}$ (LS197)	1.0 U.L.	0.8 U.L.
\overline{MR}	1.0 U.L.	0.5 U.L.
PL	0.5 U.L.	0.25 U.L.
P_0 – P_3	0.5 U.L.	0.25 U.L.
Q_0 – Q_3	10 U.L.	5 (2.5) U.L.

NOTES:

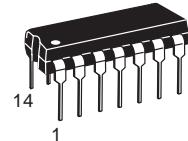
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
 c. In addition to loading shown, Q_0 can also drive $\overline{CP_1}$.

SN54/74LS196 SN54/74LS197

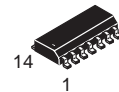
4-STAGE PRESETTABLE RIPPLE COUNTERS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

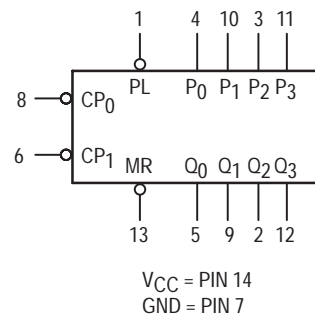


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

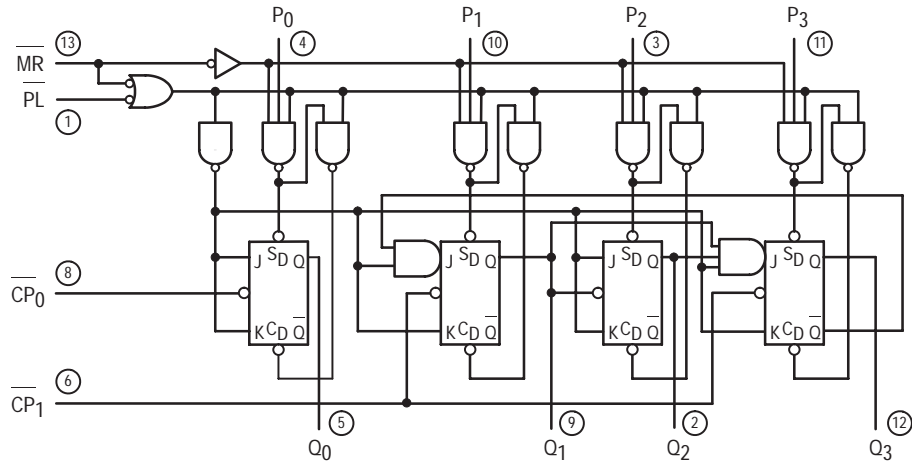
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL

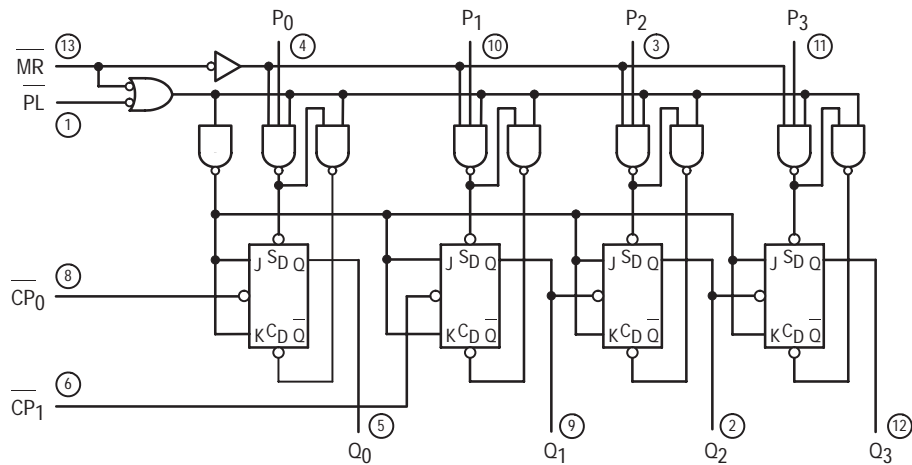


SN54/74LS196 • SN54/74LS197

LOGIC DIAGRAM



LS196



LS197

V_{CC} = PIN 14
 GND = PIN 7
 ○ = PIN NUMBERS

SN54/74LS196 • SN54/74LS197

FUNCTIONAL DESCRIPTION

The LS196 and LS197 are asynchronously presettable decade and binary ripple counters. The LS196 Decade Counter is partitioned into divide-by-two and divide-by-five sections while the LS197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH to LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The CP_0 input serves the Q_0 flip-flop in both circuit types while the CP_1 input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the CP_1 input. With the input frequency connected to CP_0 and Q_0 driving CP_1 , the LS197 forms a straightforward module-16 counter, with Q_0 the least significant output and Q_3 the most

significant output.

The LS196 Decade Counter can be connected up to operate in two different count sequences, as indicated in the tables of Figure 2. With the input frequency connected to CP_0 and with Q_0 driving CP_1 , the circuit counts in the BCD (8, 4, 2, 1) sequence. With the input frequency connected to CP_1 and Q_3 driving CP_0 , Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The LS196 and LS197 have an asynchronous active LOW Master Reset input (MR) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (PL) overrides the clock inputs and loads the data from Parallel Data (P_0-P_3) inputs into the flip-flops. While PL is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs.

Figure 2. LS196 COUNT SEQUENCES

DECADE (NOTE 1)					BI-QUINARY (NOTE 2)				
COUNT	Q_3	Q_2	Q_1	Q_0	COUNT	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L	0	L	L	L	L
1	L	L	L	H	1	L	L	L	H
2	L	L	H	L	2	L	L	H	L
3	L	L	H	H	3	L	L	H	H
4	L	H	L	L	4	L	H	L	L
5	L	H	L	H	5	H	L	L	L
6	L	H	H	L	6	H	L	L	H
7	L	H	H	H	7	H	L	H	L
8	H	L	L	L	8	H	L	H	H
9	H	L	L	H	9	H	H	L	L

NOTES:

- Signal applied to CP_0 , Q_0 connected to CP_1 .
- Signal applied to CP_1 , Q_3 connected to CP_0 .

MODE SELECT TABLE

INPUTS			RESPONSE
MR	PL	CP	
L	X	X	Reset (Clear)
H	L	X	Parallel Load
H	H	\downarrow	Count

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 \downarrow = HIGH to Low Clock Transition

SN54/74LS196 • SN54/74LS197

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current Data, PL MR, CP ₀ (LS196) MR, CP ₀ , CP ₁ (LS197) CP ₁ (LS196)			20 40 40 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Data, PL MR, CP ₀ (LS196) MR, CP ₀ , CP ₁ (LS197) CP ₁ (LS196)			0.1 0.2 0.2 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Data, PL MR CP ₀ CP ₁ (LS196) CP ₁ (LS197)			-0.4 -0.8 -2.4 -2.8 -1.3	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			27	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS196 • SN54/74LS197

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	30	40		30	40		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	CP ₀ Input to Q ₀ Output		8.0 13	15 20		8.0 14	15 21	ns	
t _{PLH} t _{PHL}	CP ₁ Input to Q ₁ Output		16 22	24 33		12 23	19 35	ns	
t _{PLH} t _{PHL}	CP ₁ Input to Q ₂ Output		38 41	57 62		34 42	51 63	ns	
t _{PLH} t _{PHL}	CP ₁ Input to Q ₃ Output		12 30	18 45		55 63	78 95	ns	
t _{PLH} t _{PHL}	Data to Output		20 29	30 44		18 29	27 44	ns	
t _{PLH} t _{PHL}	PL Input to Any Output		27 30	41 45		26 30	39 45	ns	
t _{PHL}	MR Input to Any Output		34	51		34	51	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS196			LS197				
		Min	Typ	Max	Min	Typ	Max		
t _W	CP ₀ Pulse Width	20			20			ns	V _{CC} = 5.0 V
t _W	CP ₁ Pulse Width	30			30			ns	
t _W	PL Pulse Width	20			20			ns	
t _W	MR Pulse Width	15			15			ns	
t _s	Data Input Setup Time — HIGH	10			10			ns	
t _s	Data Input Setup Time — LOW	15			15			ns	
t _h	Data Hold Time — HIGH	10			10			ns	
t _h	Data Hold Time — LOW	10			10			ns	
t _{rec}	Recovery Time	30			30			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recog-

nition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer LOW Data to the Q outputs.

SN54/74LS196 • SN54/74LS197

AC WAVEFORMS

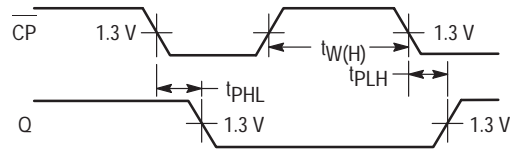
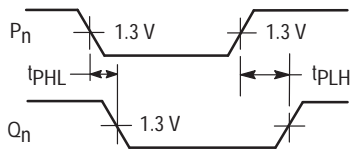


Figure 1



NOTE: $\bar{P}L = \text{LOW}$

Figure 2

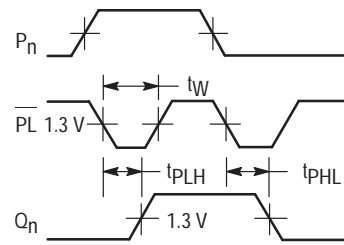


Figure 3

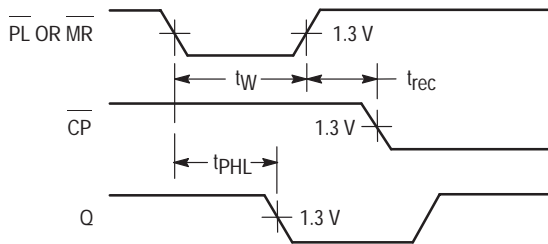
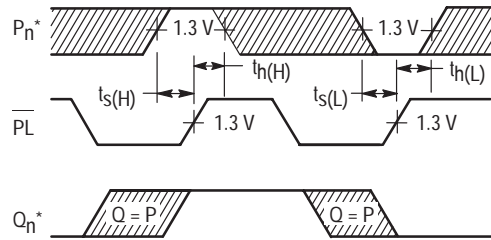


Figure 4



* The shaded areas indicate when the input is permitted to change for predictable output performance

Figure 5



DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

Each multivibrator of the LS221 features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1 volt/second, providing the circuit with excellent noise immunity. A high immunity to V_{CC} noise is also provided by internal latching circuitry.

Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With $R_{ext} = 2.0 \text{ k}\Omega$ and $C_{ext} = 0$, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

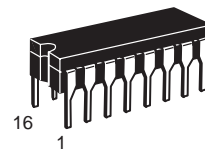
Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10 pF to 10 μF), and greater than one decade of timing resistance (2.0 to 70 k Ω for the SN54LS221, and 2.0 to 100 k Ω for the SN74LS221). Pulse width is defined by the relationship: $t_w(\text{out}) = C_{ext}R_{ext} \ln 2.0 \approx 0.7 C_{ext} R_{ext}$; where t_w is in ns if C_{ext} is in pF and R_{ext} is in k Ω . If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 k Ω may be used. The range of jitter-free pulse widths is extended if V_{CC} is 5.0 V and 25°C temperature.

- SN54LS221 and SN74LS221 is a Dual Highly Stable One-Shot
- Overriding Clear Terminates Output Pulse
- Pin Out is Identical to SN54/74LS123

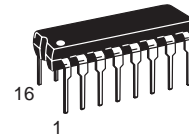
SN54/74LS221

DUAL MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

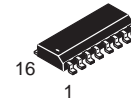
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

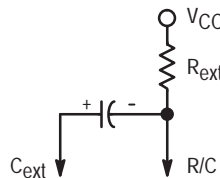
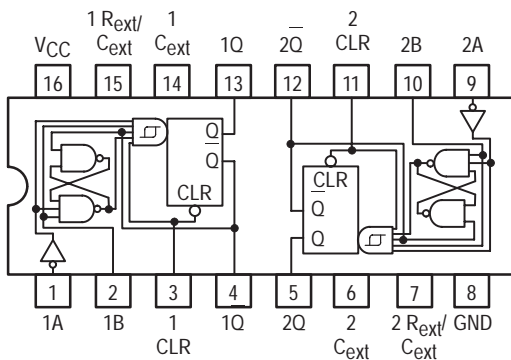


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

(TOP VIEW)



positive logic: \bar{L} input to clear resets Q low and Q high regardless of dc levels at A or B inputs.

FUNCTION TABLE (EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow		
H	\downarrow	H		
\uparrow	L	H		

*See operational notes — Pulse Trigger Modes

TYPE	TYPICAL	MAXIMUM
	POWER DISSIPATION	OUTPUT PULSE LENGTH
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54/74LS221

OPERATIONAL NOTES

Once in the pulse trigger mode, the output pulse width is determined by $t_W = R_{ext}C_{ext}\ln 2$, as long as R_{ext} and C_{ext} are within their minimum and maximum values and the duty cycle is less than 50%. This pulse width is essentially independent of V_{CC} and temperature variations. Output pulse widths varies typically no more than $\pm 0.5\%$ from device to device.

If the duty cycle, defined as being $100 \cdot \frac{t_W}{T}$ where T is the period of the input pulse, rises above 50%, the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum, R_{ext} should be as large as possible. (Jitter is independent of C_{ext}). With $R_{ext} = 100K$, jitter is not appreciable until the duty cycle approaches 90%.

Although the LS221 is pin-for-pin compatible with the LS123, it should be remembered that they are not functionally identical. The LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the LS221. Also note that it is recommended to externally ground the LS123 C_{ext} pin. However, this cannot be done on the LS221.

The SN54LS/74LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width, t_W can be varied over 9 decades of timing by proper selection of the external timing components, R_{ext} and C_{ext} .

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers ($\geq 1.0 \mu V/s$). High immunity to V_{CC} noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard V_{CC} bypassing is strongly recommended.

The LS221 has four basic modes of operation.

Clear Mode: If the clear input is held low, irregardless of the previous output state and other input states, the Q output is low.

Inhibit Mode: If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other inputs.

Pulse Trigger Mode: A transition of the A or B inputs as indicated in the functional truth table will trigger the Q output to go high for a duration determined by the t_W equation described above; Q will go low for a corresponding length of time.

The Clear input may also be used to trigger an output pulse, but special logic preconditioning on the A or B inputs must be done as follows:

Following any output triggering action using the A or B inputs, the A input must be set high OR the B input must be set low to allow Clear to be used as a trigger. Inputs should then be set up per the truth table (without triggering the output) to allow Clear to be used a trigger for the output pulse.

If the Clear pin is routinely being used to trigger the output pulse, the A or B inputs must be toggled as described above before and between each Clear trigger event.

Once triggered, as long as the output remains high, all input transitions (except overriding Clear) are ignored.

Overriding Clear Mode: If the Q output is high, it may be forced low by bringing the clear input low.

SN54/74LS221

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{T+}	Positive-Going Threshold Voltage at C Input		1.0	2.0	V	V _{CC} = MIN
V _{T-}	Negative-Going Threshold Voltage at C Input	54	0.7	0.8	V	V _{CC} = MIN
		74	0.7	0.8	V	
V _{T+}	Positive-Going Threshold Voltage at B Input		1.0	2.0	V	V _{CC} = MIN
V _{T-}	Negative-Going Threshold Voltage at B Input	54	0.7	0.9	V	V _{CC} = MIN
		74	0.8	0.9	V	
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for A Input
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for A Input
		74		0.8	V	
V _{IK}	Input Clamp Voltage			-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.4	V	V _{CC} = MIN, I _{OH} = MAX
		74	2.7	3.4	V	
V _{OL}	Output LOW Voltage	54	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Input A Input B Clear			-0.4 -0.8 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Quiescent		4.7	11	mA	V _{CC} = MAX
	Triggered		19	27	mA	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS221

AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Symbol	From (Input)	To (Output)	Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH}	A	Q		45	70	ns	C _L = 15 pF, See Figure 1	
	B	Q		35	55			
t _{PHL}	A	Q		50	80	ns		C _{ext} = 80 pF, R _{ext} = 2.0 Ω
	B	Q		40	65			
t _{PHL}	Clear	Q		35	55	ns		
t _{PLH}	Clear	Q		44	65	ns		
t _{W(out)}	A or B	Q or \bar{Q}	70	120	150	ns	C _{ext} = 80 pF, R _{ext} = 2.0 Ω	
			20	47	70		C _{ext} = 0, R _{ext} = 2.0 kΩ	
			600	670	750		C _{ext} = 100 pF, R _{ext} = 10 kΩ	
			6.0	6.9	7.5		ms	C _{ext} = 1.0 μF, R _{ext} = 10 kΩ

AC SETUP REQUIREMENTS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
dv/dt	Rate of Rise or Fall of Input Pulse	Schmitt, B	1.0		V/s
		Logic Input, A	1.0		V/μs
t _W	Input Pulse Width	A or B, t _{W(in)}	40		ns
		Clear, t _W (clear)	40		
t _s	Clear-Inactive-State Setup Time	15		ns	
R _{ext}	External Timing Resistance	54	1.4	70	kΩ
		74	1.4	100	
C _{ext}	External Timing Capacitance	0		1000	μF
	Output Duty Cycle	RT = 2.0 kΩ		50	%
		RT = MAX R _{ext}		90	

SN54/74LS221

AC WAVEFORMS

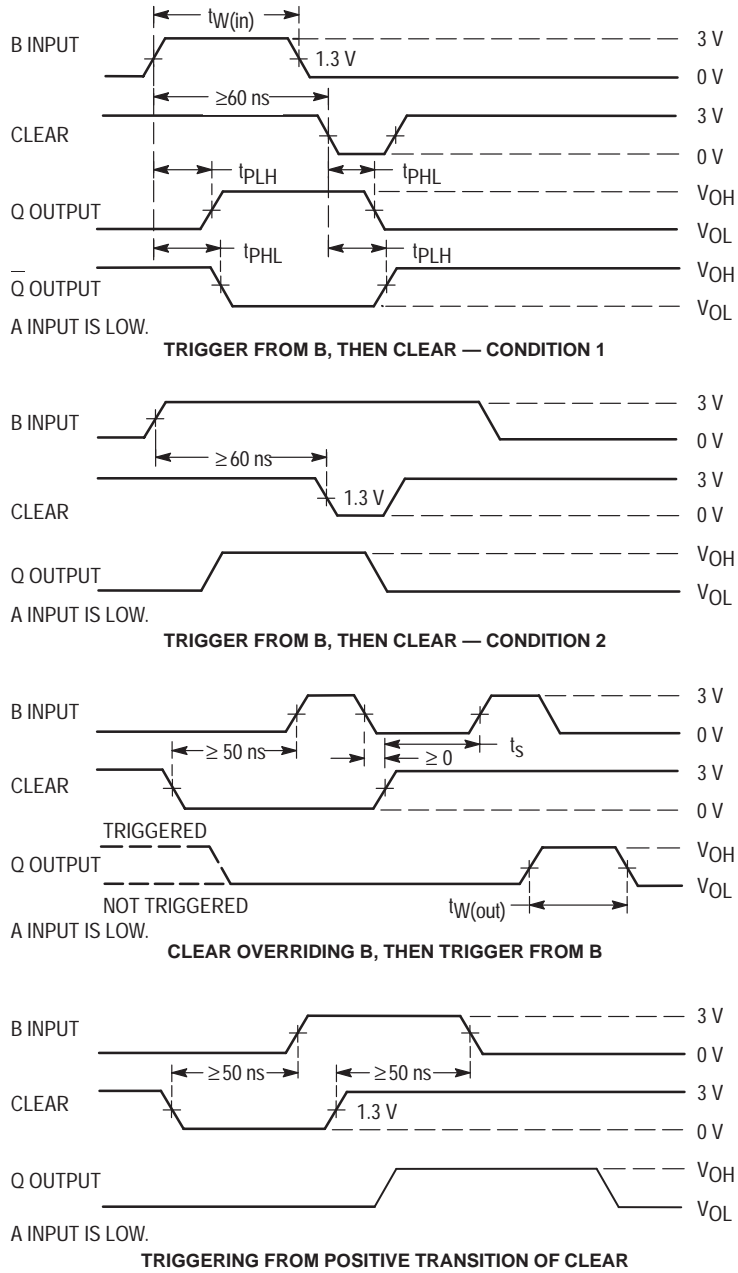


Figure 1

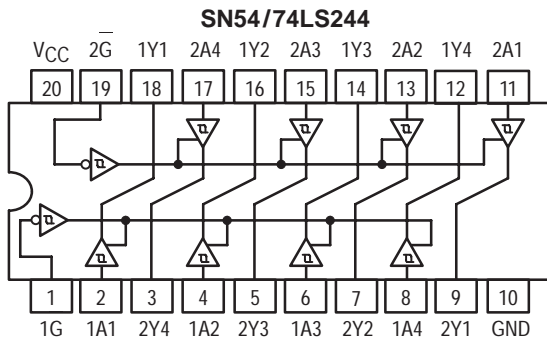
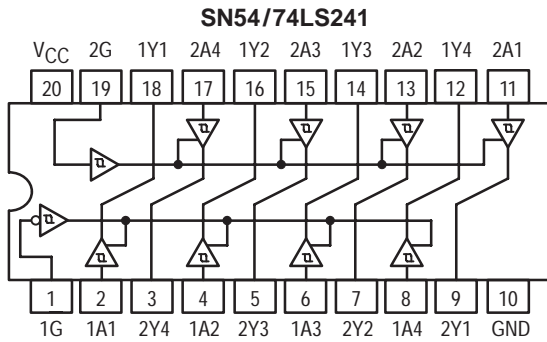
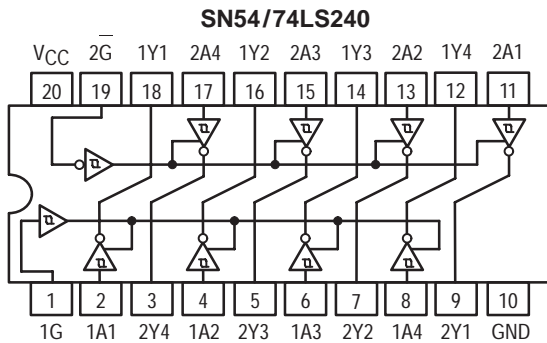


OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The SN54/74LS240, 241 and 244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

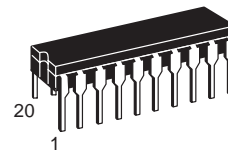
- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

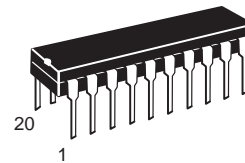


**SN54/74LS240
SN54/74LS241
SN54/74LS244**

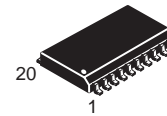
**OCTAL BUFFER/LINE DRIVER
WITH 3-STATE OUTPUTS
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 732-03**



**N SUFFIX
PLASTIC
CASE 738-03**



**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

SN54/74LS240 • SN54/74LS241 • SN54/74LS244

TRUTH TABLES

SN54/74LS240

INPUTS		OUTPUT
1G, 2G	D	
L	L	H
L	H	L
H	X	(Z)

SN54/74LS244

INPUTS		OUTPUT
1G, 2G	D	
L	L	L
L	H	H
H	X	(Z)

SN54/74LS241

INPUTS		OUTPUT	INPUTS		OUTPUT
1G	D		2G	D	
L	L	L	H	L	L
L	H	H	H	H	H
H	X	(Z)	L	X	(Z)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
		54 74			-12 -15	mA
I _{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS240 • SN54/74LS241 • SN54/74LS244

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{T+} -V _{T-}	Hysteresis		0.2	0.4		V	V _{CC} = MIN
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	V _{CC} = MIN, I _{OH} = -3.0 mA
		54, 74	2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1)		-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH				27	mA	V _{CC} = MAX
	Total, Output LOW	LS240			44		
		LS241/244			46		
	Total at HIGH Z	LS240			50		
LS241/244				54			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Output LS240			9.0 12	14 18	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Data to Output LS241/244			12 12	18 18	ns	
t _{PZH}	Output Enable Time to HIGH Level			15	23	ns	
t _{PZL}	Output Enable Time to LOW Level			20	30	ns	
t _{PLZ} t _{PHZ}	Output Disable Time from LOW Level Output Disable Time from HIGH Level			15 10	25 18	ns	

SN54/74LS240 • SN54/74LS241 • SN54/74LS244

AC WAVEFORMS

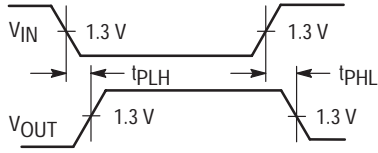


Figure 1

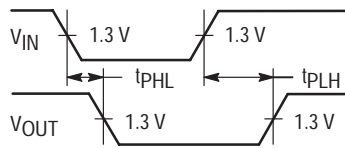


Figure 2

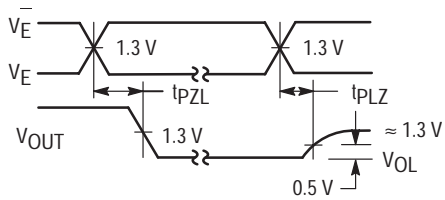


Figure 3

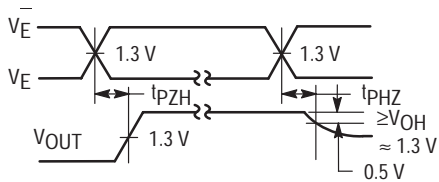
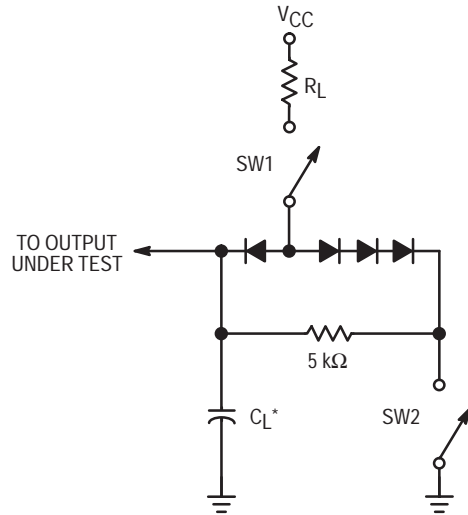


Figure 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 5



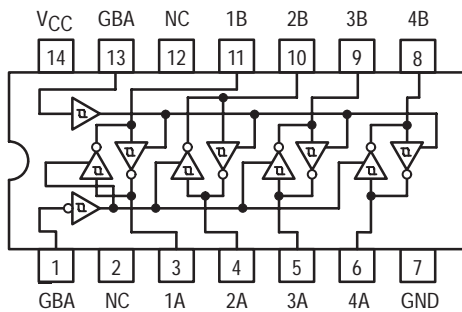
QUAD BUS TRANSCEIVER

The SN54/74LS242 and SN54/74LS243 are Quad Bus Transmitters/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

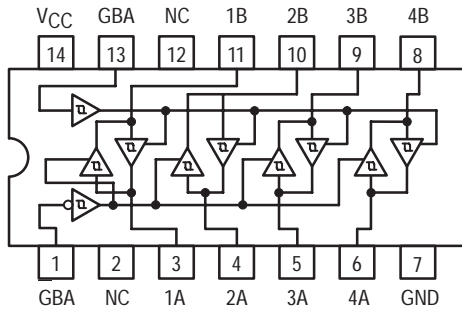
- Hysteresis at Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

SN54/74LS242



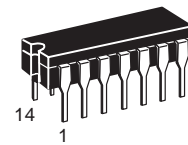
SN54/74LS243



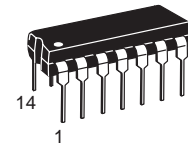
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS242
SN54/74LS243

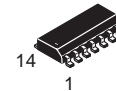
QUAD BUS TRANSCEIVER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

TRUTH TABLES

SN54/74LS242

INPUTS		OUTPUT	INPUTS		OUTPUT
GAB	D		GAB	D	
L	L	H	L	X	(Z)
L	H	L	H	L	H
H	X	(Z)	H	H	L

SN54/74LS243

INPUTS		OUTPUT	INPUTS		OUTPUT
GAB	D		GAB	D	
L	L	L	L	X	(Z)
L	H	H	H	L	H
H	X	(Z)	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

SN54/74LS242 • SN54/74LS243

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-3.0	mA
		54 74			-12 -15	mA
I _{OL}	Output Current — Low	54			12	mA
		74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{T+} -V _{T-}	Hysteresis		0.2	0.4		V	V _{CC} = MIN
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	V _{CC} = MIN, I _{OH} = -3.0 mA
		54, 74	2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-200	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current	D, E ₁ , E ₂			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		E ₁ , E ₂			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		D Input			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
I _{IL}	Input LOW Current				-0.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1)		-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH				38	mA	V _{CC} = MAX
					50		
	Total at HIGH Z	LS242			50		
		LS243			54		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS242 • SN54/74LS243

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS242			LS243				
		Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		9.0 12	14 18		12 12	18 18	ns	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$
t_{PZH}	Output Enable Time to HIGH Level		15	23		15	23	ns	
t_{PZL}	Output Enable Time to LOW Level		20	30		20	30	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25		15	25	ns	$C_L = 5.0\text{ pF}$, $R_L = 667\ \Omega$
t_{PHZ}	Output Disable Time from HIGH Level		10	18		10	18	ns	

AC WAVEFORMS

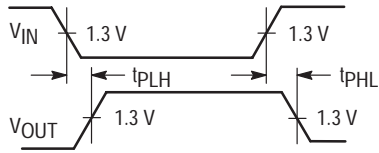


Figure 1

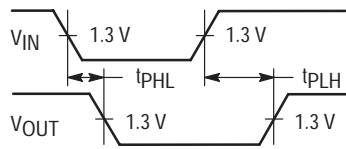


Figure 2

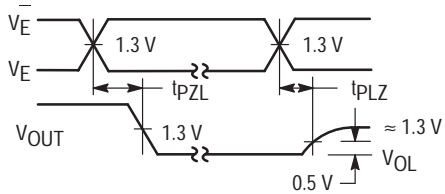


Figure 3

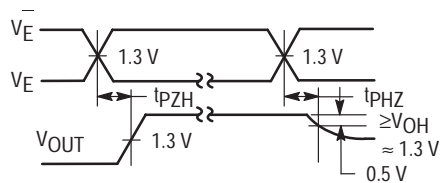
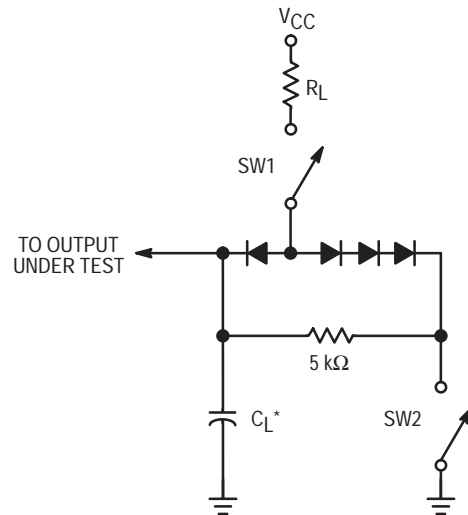


Figure 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5

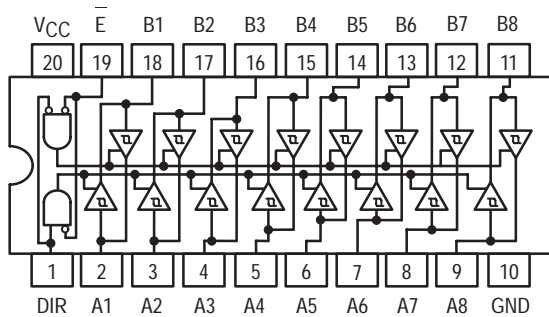


OCTAL BUS TRANSCEIVER

The SN54/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input (E) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



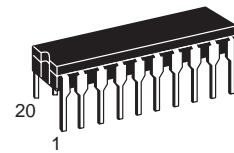
TRUTH TABLE

INPUTS		OUTPUT
E	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

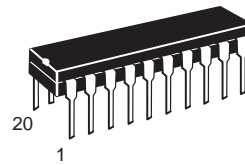
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN54/74LS245

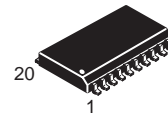
OCTAL BUS TRANSCEIVER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
		54 74			-12 -15	mA
I _{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS245

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{T+} -V _{T-}	Hysteresis		0.2	0.4		V	V _{CC} = MIN
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	V _{CC} = MIN, I _{OH} = -3.0 mA
		54, 74	2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-200	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current	A or B, DR or E			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		DR or E			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		A or B			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
I _{IL}	Input LOW Current				-0.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Output Short Circuit Current (Note 1)		-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH				70	mA	V _{CC} = MAX
	Total, Output LOW				90		
	Total at HIGH Z				95		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, T_{RISE}/T_{FALL} ≤ 6.0 ns)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			8.0 8.0	12 12	ns	C _L = 45 pF, R _L = 667 Ω
t _{PZH}	Output Enable Time to HIGH Level			25	40	ns	
t _{PZL}	Output Enable Time to LOW Level			27	40	ns	
t _{PLZ}	Output Disable Time from LOW Level			15	25	ns	C _L = 5.0 pF, R _L = 667 Ω
t _{PHZ}	Output Disable Time from HIGH Level			15	25	ns	



BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

The SN54/74LS247 thru SN54/74LS249 are BCD-to-Seven-Segment Decoder/Drivers.

The LS247 and LS248 are functionally and electrically identical to the LS47 and LS48 with the same pinout configuration. The LS249 is a 16-pin version of the 14-pin LS49 and includes full functional capability for lamp test and ripple blanking which was not available in the LS49.

The composition of all characters, except the 6 and 9 are identical between the LS247, 248, 249 and the LS47, 48 and 49. The LS47 thru 49 compose the and without tails, the LS247 thru 249 compose the and with the tails. The LS247 has active-low outputs for direct drive of indicators. The LS248 and 249 have active-high outputs for driving lamp buffers.

All types feature a lamp test input and have full ripple-blanking input/output controls. On all types an automatic leading and/or trailing-edge zero-blanking control (RBI and RBO) is incorporated and an overriding blanking input (BI) is contained which may be used to control the lamp intensity by pulsing or to inhibit the output's lamp test may be performed at any time when the BI/RBO node is at high level. Segment identification and resultant displays are shown below. Display pattern for BCD input counts above 9 are unique symbols to authenticate input conditions.

LS247

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS248

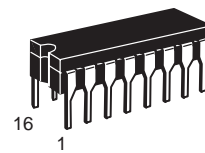
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

LS249

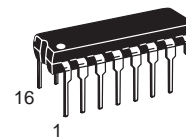
- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

SN54/74LS247
SN54/74LS248
SN54/74LS249

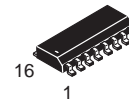
**BCD-TO-SEVEN-SEGMENT
DECODERS/DRIVERS**
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



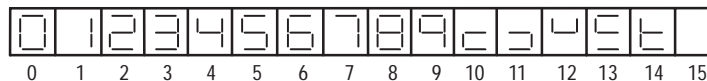
N SUFFIX
PLASTIC
CASE 648-08



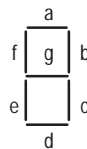
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC



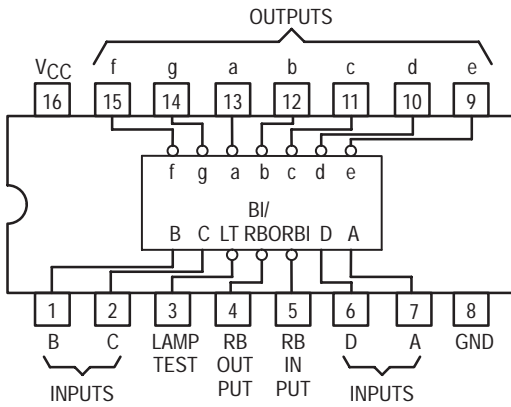
NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS



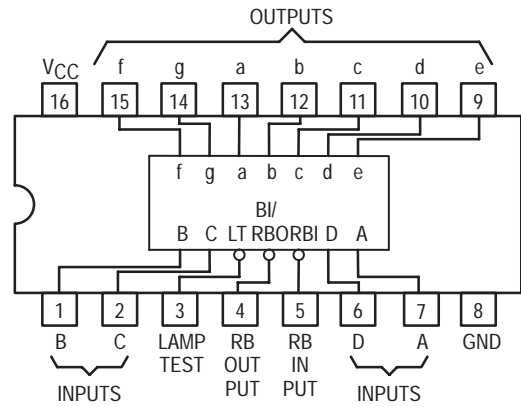
**SEGMENT
IDENTIFICATION**

SN54/74LS247 • SN54/74LS248 • SN54/74LS249

SN54/74LS247
(TOP VIEW)



SN54/74LS248
SN54/74LS259
(TOP VIEW)

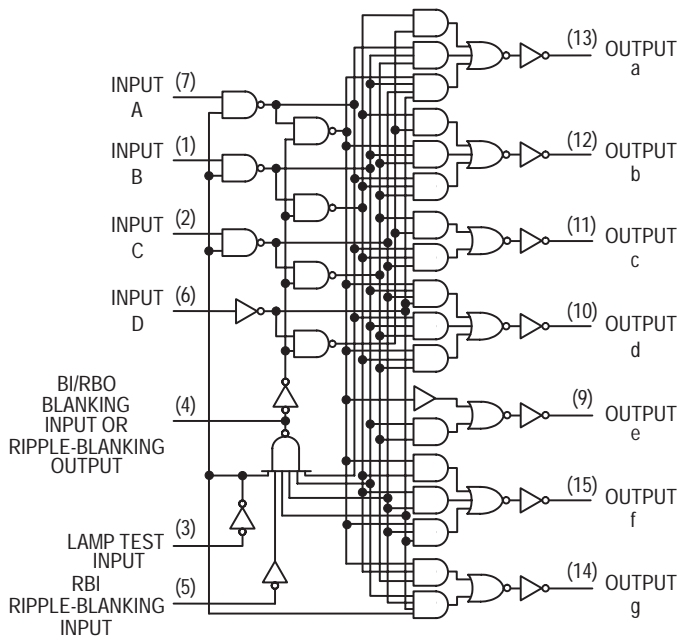


ALL CIRCUIT TYPES FEATURE LAMP INTENSITY MODULATION CAPABILITY

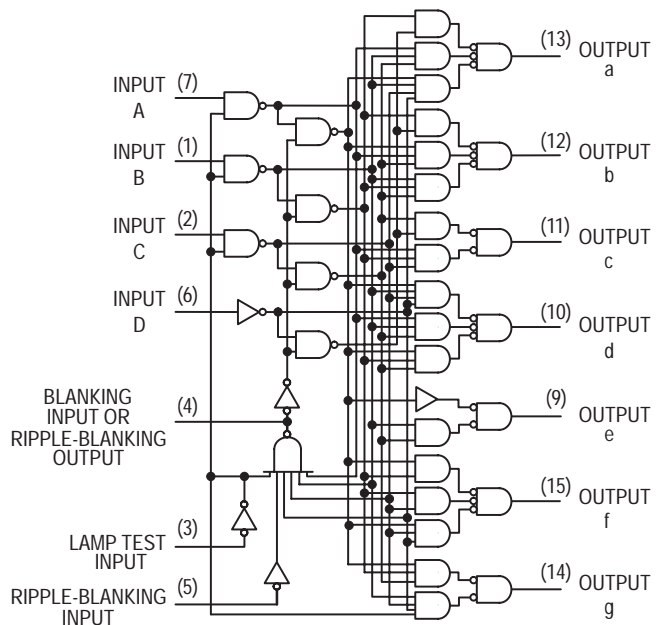
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE	
SN54LS247	low	open-collector	12 mA	15 V	35 mW
SN54LS248	high	2.0 kΩ pull-up	2.0 mA	5.5 V	125 mW
SN54LS249	high	open-collector	4.0 mA	5.5 V	40 mW
SN74LS247	low	open-collector	24 mA	15 V	35 mW
SN74LS248	high	2.0 kΩ pull-up	6.0 mA	5.5 V	125 mW
SN74LS249	high	open-collector	8.0 mA	5.5 V	40 mW

LOGIC DIAGRAM

LS247



LS248, LS249



SN54/74LS247 • SN54/74LS248 • SN54/74LS249

LS247 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

LS248, LS249 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO [†]	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	L	H	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = HIGH Level, L = LOW Level, X = Irrelevant

- NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

[†] BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

SN54/74LS247

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High BI/RBO	54, 74			-50	μA
I _{OL}	Output Current — Low BI/RBO	54			1.6	mA
		74			3.2	
V _{O(off)}	Off-State Output Voltage a-g	54, 74			15	V
I _{O(on)}	On-State Output Current a-g	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage BI/RBO	54	2.4	4.2	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	4.2	V		
V _{OL}	Output LOW Voltage BI/RBO	54, 74		0.25	0.4	V	I _{OL} = 1.6 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{O(off)}	Off-State Output Current a-g	54, 74			250	μA	V _{CC} = MAX, V _{IH} = 2.0 V, V _{O(off)} = 15 V, V _{IL} = MAX
V _{O(on)}	On-State Output Voltage a-g	54, 74		0.25	0.4	V	I _{O(on)} = 12 mA V _{CC} = MIN, V _{IH} = 2.0 V, V _{IL} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current Any Input, except BI/RBO BI/RBO				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
					-1.2		
I _{OS}	Short Circuit Current BI/RBO (Note 1)	-0.3			-2.0	mA	V _{CC} = MAX
I _{CC}	Power Supply Current		7.0		13	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH}	Turn-Off Time from A Input			100	ns	C _L = 15 pF, R _L = 665 Ω
t _{PHL}	Turn-On Time from A Input			100		
t _{PHL}	Turn-Off Time from RBI Input			100	ns	
t _{PLH}	Turn-On Time from RBI Input			100		

SN54/74LS248

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High BI/RBO a-g	54, 74 54, 74			-50 -100	μA
I _{OL}	Output Current — Low BI/RBO BI/RBO a-g a-g	54 74 54 74			1.6 3.2 2.0 6.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage a-g and BI/RBO	54	2.4	4.2	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	4.2	V		
I _{OH}	Output Current a-g	54, 74	-1.3	-2.0	mA	V _{CC} = MIN, V _O = 0.85 V, Input Conditions as for V _{OH}	
V _{OL}	Output LOW Voltage a-g	54, 74		0.25	0.4	V	V _{CC} = MIN, V _{IH} = 2.0 V, V _{IL} = per Truth Table
		74		0.35	0.5	V	
	BI/RBO	54, 74		0.25	0.4	V	
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current Any Input, except BI/RBO			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Any Input, except BI/RBO BI/RBO			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
				-1.2	mA		
I _{OS}	Short Circuit Current BI/RBO (Note 1)	-0.3		-2.0	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current		25	38	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	C _L = 15 pF R _L = 4.0 kΩ
t _{PHL} t _{PLH}	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	C _L = 15 pF R _L = 6.0 kΩ

SN54/74LS249

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High BI/RBO	54, 74			-50	μA
I _{OL}	Output Current — Low BI/RBO BI/RBO	54 74			1.6 3.2	mA
V _{OH}	Output Voltage — High a-g	54, 74			5.5	V
I _{OL}	Output Current — Low a-g a-g	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage BI/RBO	54	2.4	4.2	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	4.2	V		
I _{OH}	Output HIGH Current a-g	54, 74		250	μA	V _{CC} = MIN, V _{IH} = 2.0 V, V _{OH} = 5.5 V, V _{IL} = MAX	
V _{OL}	Output LOW Voltage BI/RBO	54, 74		0.25	0.4	V	V _{CC} = MIN, V _{IH} = 2.0 V, V _{IL} = per Truth Table
		74		0.35	0.5	V	
	a-g	54, 74		0.25	0.4	V	
		74		0.35	0.5		
I _{IH}	Input HIGH Current Any Input, except BI/RBO			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Any Input, except BI/RBO BI/RBO			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
				-1.2			
I _{OS}	Short Circuit Current BI/RBO (Note 1)	-0.3		-2.0	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current		8.0	15	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PHL} t _{PLH}	Propagation Delay Time, High-to-Low-Level Output from A Input Propagation Delay Time, Low-to-High-Level Output from A Input			100 100	ns	C _L = 15 pF, R _L = 2.0 Ω
t _{PHL} t _{PLH}	Propagation Delay Time, High-to-Low-Level Output from RBI Input Propagation Delay Time, Low-to-High-Level Output from RBI Input			100 100	ns	C _L = 15 pF, R _L = 6.0 Ω

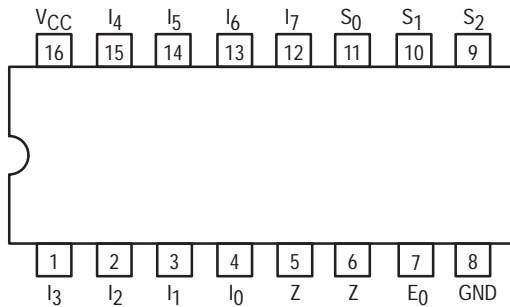


8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The TTL/MSI SN74LS251 is a high speed 8-Input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Inverting and Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

S_0 - S_2	Select Inputs
E_0	Output Enable (Active LOW) Inputs
I_0 - I_7	Multiplexer Inputs
Z	Multiplexer Output
\bar{Z}	Complementary Multiplexer Output

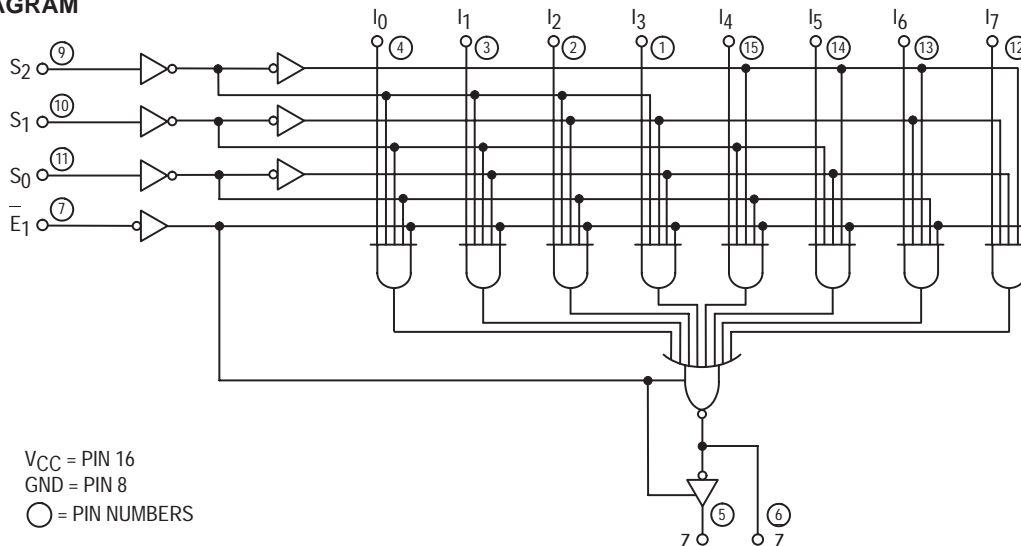
LOADING (Note a)

	HIGH	LOW
S_0 - S_2	0.5 U.L.	0.25 U.L.
E_0	0.5 U.L.	0.25 U.L.
I_0 - I_7	0.5 U.L.	0.25 U.L.
Z	65 U.L.	15 U.L.
\bar{Z}	65 U.L.	15 U.L.

NOTES:

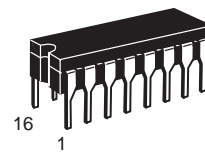
a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

LOGIC DIAGRAM

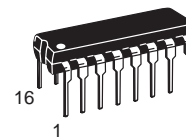


SN54/74LS251

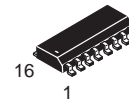
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

SN54/74LS251

FUNCTIONAL DESCRIPTION

The LS251 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both assertion and negation outputs are provided. The Output Enable input (E_0) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{E_0} \cdot (I_0 \cdot S_0 \cdot S_1 \cdot S_2 + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_3 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_4 \cdot S_0 \cdot S_1 \cdot S_2 + I_5 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_6 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltage.

TRUTH TABLE

E_0	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 (Z) = High impedance (Off)

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			-2.6	mA
I_{OL}	Output Current — Low			24	mA

SN54/74LS251

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
			0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current			10	mA	V _{CC} = MAX, V _E = 0 V
				12	mA	V _{CC} = MAX, V _E = 4.5 V

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Select to Z Output		20 21	33 33	ns	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, Select to Z Output		29 28	45 45	ns	Figure 2
t _{PLH} t _{PHL}	Propagation Delay, Data to Z Output		10 9.0	15 15	ns	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, Data to Z Output		17 18	28 28	ns	Figures 2
t _{PZH} t _{PZL}	Output Enable Time to Z Output		17 24	27 40	ns	Figures 4, 5
t _{PZH} t _{PZL}	Output Enable Time to Z Output		30 26	45 40	ns	Figures 3, 5
t _{PHZ} t _{PLZ}	Output Disable Time to Z Output		37 15	55 25	ns	Figures 3, 5
t _{PHZ} t _{PLZ}	Output Disable Time to Z Output		30 15	45 25	ns	Figures 4, 5

C_L = 15 pF,
R_L = 2.0 kΩ

C_L = 5.0 pF,
R_L = 667 kΩ

SN54/74LS251

3-STATE AC WAVEFORMS

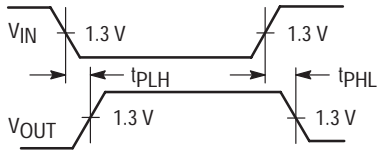


Figure 1

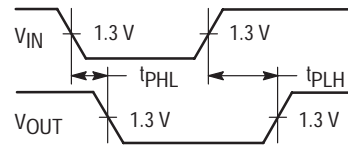


Figure 2

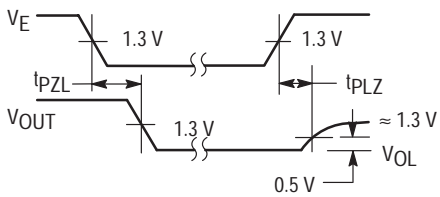


Figure 3

0.5 V

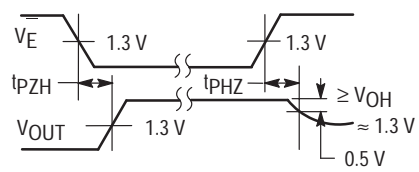
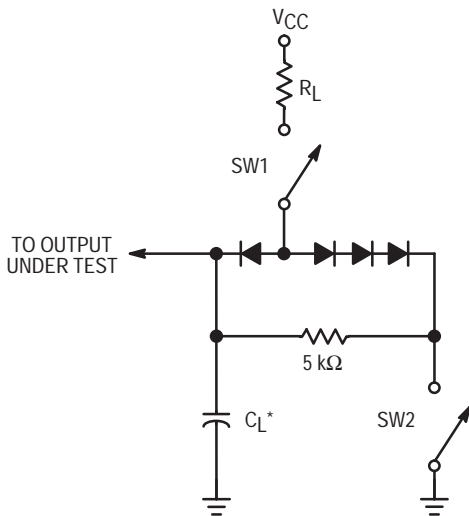


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

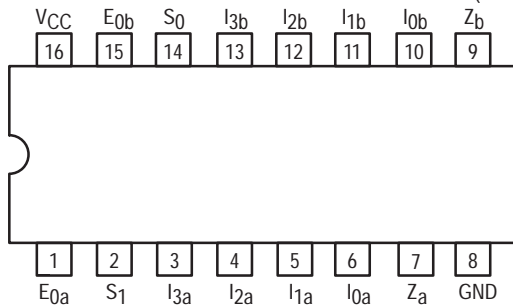


DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

- S_0, S_1 Common Select Inputs
- Multiplexer A**
- E_{0a} Output Enable (Active LOW) Input
- $I_{0a}-I_{3a}$ Multiplexer Inputs
- Z_a Multiplexer Output (Note b)
- Multiplexer B**
- E_{0b} Output Enable (Active LOW) Input
- $I_{0b}-I_{3b}$ Multiplexer Inputs
- Z_b Multiplexer Output (Note b)

LOADING (Note a)

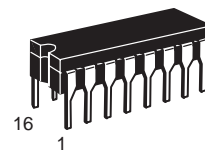
	HIGH	LOW
S_0, S_1	0.5 U.L.	0.25 U.L.
E_{0a}	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{3a}$	0.5 U.L.	0.25 U.L.
Z_a	65 (25) U.L.	15 (7.5) U.L.
E_{0b}	0.5 U.L.	0.25 U.L.
$I_{0b}-I_{3b}$	0.5 U.L.	0.25 U.L.
Z_b	65 (25) U.L.	15 (7.5) U.L.

NOTES:

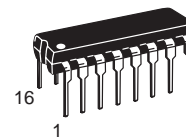
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS253

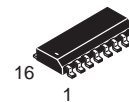
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

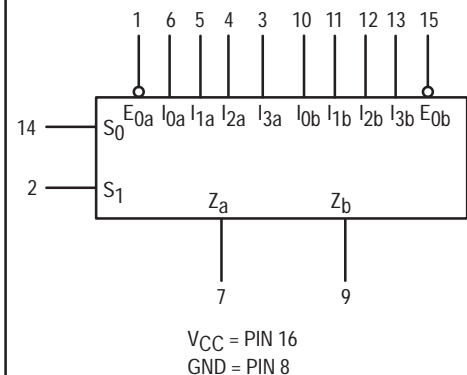


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

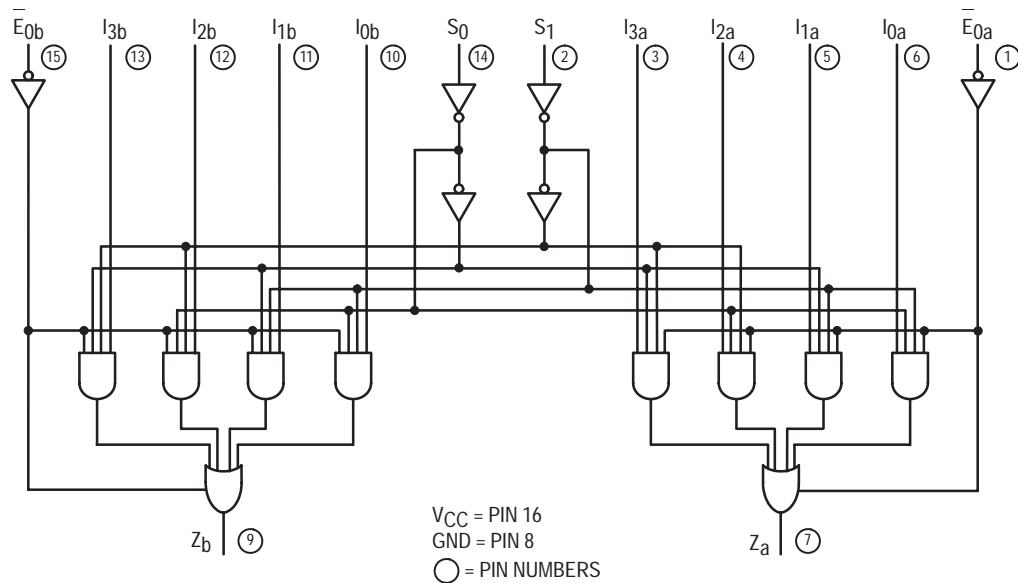
- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

LOGIC SYMBOL



SN54/74LS253

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable (E_{0a} , E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	E_0	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level

L = LOW Level

X = Irrelevant

(Z) = High Impedance (off)

Address inputs S_0 and S_1 are common to both sections.

SN54/74LS253

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			12	mA	V _{CC} = MAX, V _E = 0 V	
				14	mA	V _{CC} = MAX, V _E = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V) See SN54LS251 for Waveforms

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Output		17 13	25 20	ns	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, Select to Output		30 21	45 32	ns	Figure 1
t _{PZH} t _{PZL}	Output Enable Time		15 15	28 23	ns	Figures 4, 5
t _{PHZ} t _{PLZ}	Output Disable Time		27 18	41 27	ns	Figures 3, 5

C_L = 45 pF,
R_L = 667 Ω

C_L = 5.0 pF,
R_L = 667 Ω



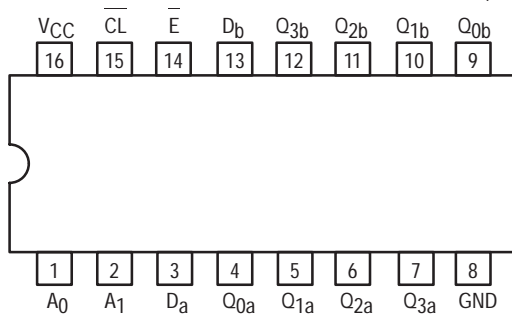
DUAL 4-BIT ADDRESSABLE LATCH

The SN54/74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input (\bar{E}) and an active LOW Clear input (\bar{CL}). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

When the Enable (\bar{E}) is HIGH and the Clear input (\bar{CL}) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the (\bar{CL}) and \bar{E} are both LOW. When \bar{CL} is HIGH and \bar{E} is LOW, the selected output (Q_0-Q_3), determined by the Address inputs, follows D . When the \bar{E} goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\bar{E}=\text{LOW}, \bar{CL}=\text{HIGH}$), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\bar{E}=\bar{CL}=\text{HIGH}$).

- Serial-to-Parallel Capability
- Output From Each Storage Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Active Low Common Clear
- Input Clamp Diodes Limit High Speed Termination Effects

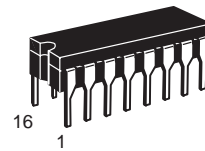
CONNECTION DIAGRAM DIP (TOP VIEW)



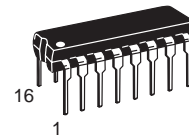
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS256

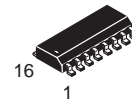
DUAL 4-BIT ADDRESSABLE LATCH LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

PIN NAMES

A_0, A_1 Address Inputs
 D_a, D_b Data Inputs
 \bar{E} Enable Input (Active LOW)
 \bar{CL} Clear Input (Active LOW)
 $Q_{0a}-Q_{3a}$
 $Q_{0b}-Q_{3b}$ Parallel Latch Outputs (Note b)

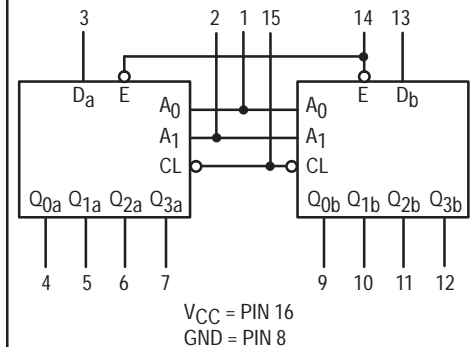
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)

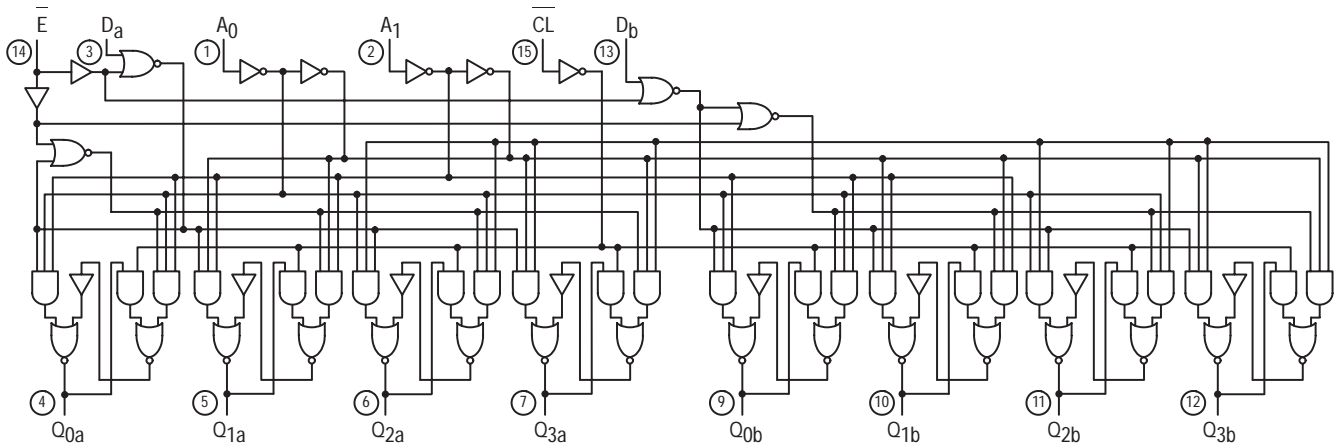
	HIGH	LOW
A_0, A_1	0.5 U.L.	0.25 U.L.
D_a, D_b	0.5 U.L.	0.25 U.L.
\bar{E}	1.0 U.L.	0.5 U.L.
\bar{CL}	0.5 U.L.	0.25 U.L.
$Q_{0a}-Q_{3a}$ $Q_{0b}-Q_{3b}$	10 U.L.	5 (2.5) U.L.

LOGIC SYMBOL



SN54/74LS256

LOGIC DIAGRAM



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

TRUTH TABLE

CL	E	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q _{N-1}	Q _{N-1}	Q _{N-1}	Q _{N-1}	Memory
H	L	L	L	L	L	Q _{N-1}	Q _{N-1}	Q _{N-1}	Addressable Latch
H	L	H	L	L	H	Q _{N-1}	Q _{N-1}	Q _{N-1}	
H	L	L	H	L	Q _{N-1}	L	Q _{N-1}	Q _{N-1}	
H	L	H	H	L	Q _{N-1}	H	Q _{N-1}	Q _{N-1}	
H	L	L	L	H	Q _{N-1}	Q _{N-1}	L	Q _{N-1}	
H	L	H	L	H	Q _{N-1}	Q _{N-1}	H	Q _{N-1}	
H	L	L	H	H	Q _{N-1}	Q _{N-1}	Q _{N-1}	L	
H	L	H	H	H	Q _{N-1}	Q _{N-1}	Q _{N-1}	H	

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

MODE SELECTION

E	CL	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

SN54/74LS256

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current Others E Input			20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Others E Input			0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current Others E Input			-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			30	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Turn-Off Delay, Enable to Output Turn-On Delay, Enable to Output		20 16	27 24	ns ns	V _{CC} = 5.0 V, C _L = 15 pF
t _{PLH} t _{PHL}	Turn-Off Delay, Data to Output Turn-On Delay, Data to Output		20 13	30 20	ns ns	
t _{PLH} t _{PHL}	Turn-Off Delay, Address to Output Turn-On Delay, Address to Output		20 14	30 24	ns ns	
t _{PHL}	Turn-On Delay, Clear to Output		12	23	ns	

SN54/74LS256

AC SET-UP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_s	Data Setup Time	20			ns	Figures 4 & 6 $V_{CC} = 5.0\text{ V}$
t_s	Address Setup Time	0			ns	
t_h	Data Hold Time	0			ns	
t_h	Address Hold Time	15			ns	
t_W	Enable Pulse Width	15			ns	

AC WAVEFORMS

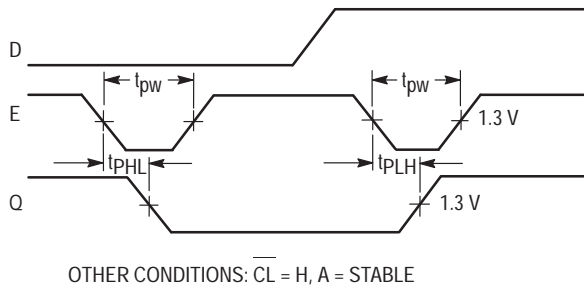


Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width

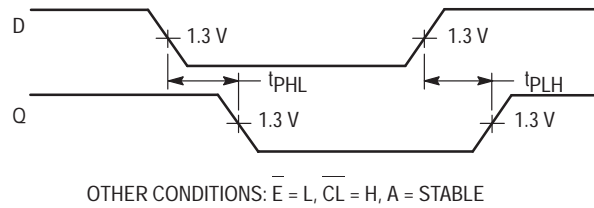


Figure 2. Turn-on and Turn-off Delays, Data to Output

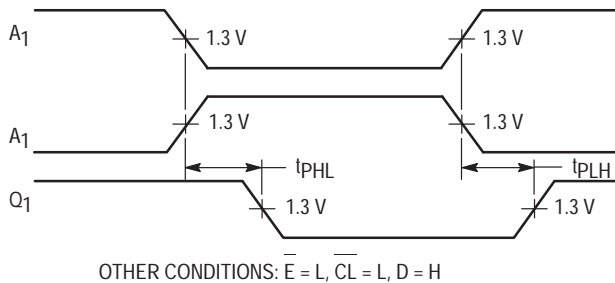


Figure 3. Turn-on and Turn-off Delays, Address to Output

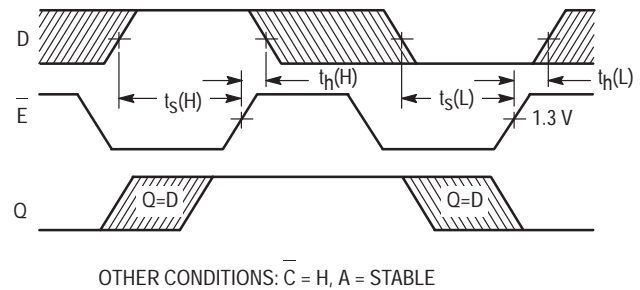


Figure 4. Setup and Hold Time, Data to Enable

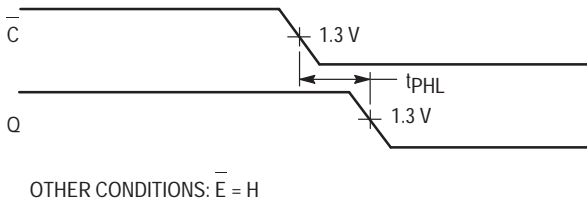


Figure 5. Turn-on Delay, Clear to Output

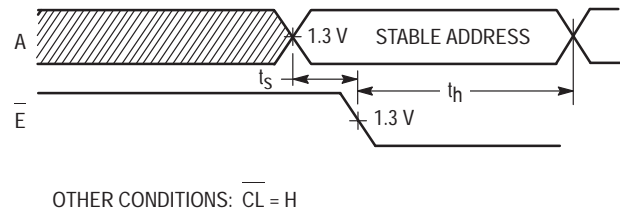


Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

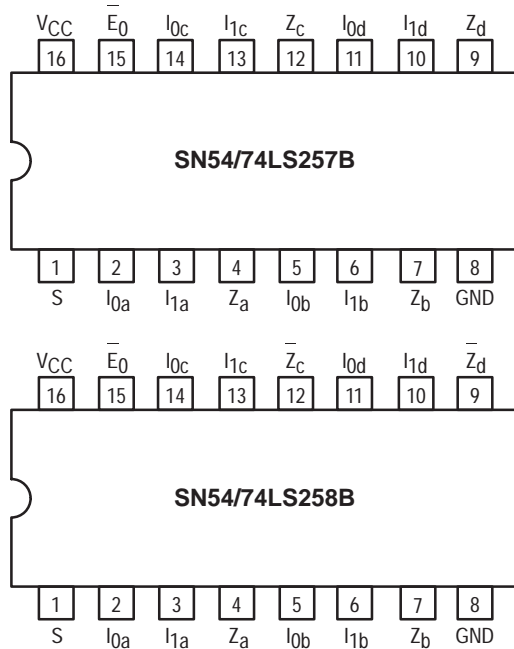


QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS257B and the SN54/74LS258B are Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\bar{E}_O) Input, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process For High Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

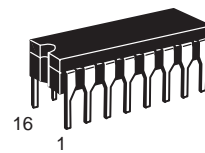


VCC = PIN 16
GND = PIN 8

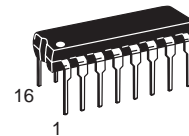
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS257B
SN54/74LS258B

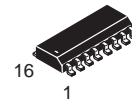
QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

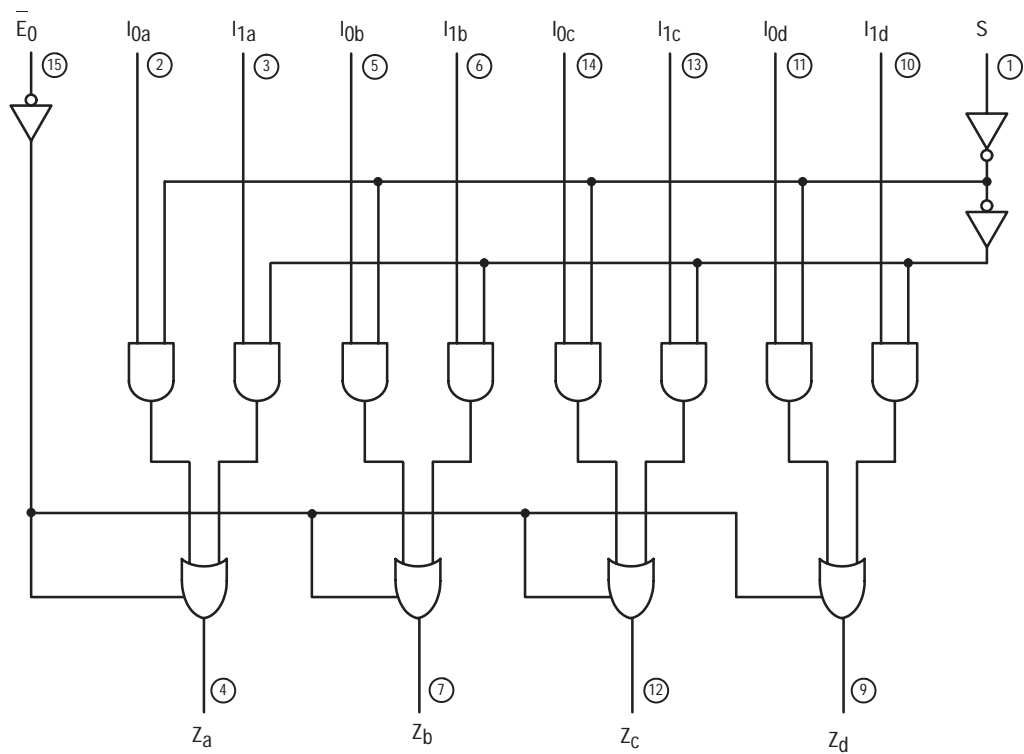
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

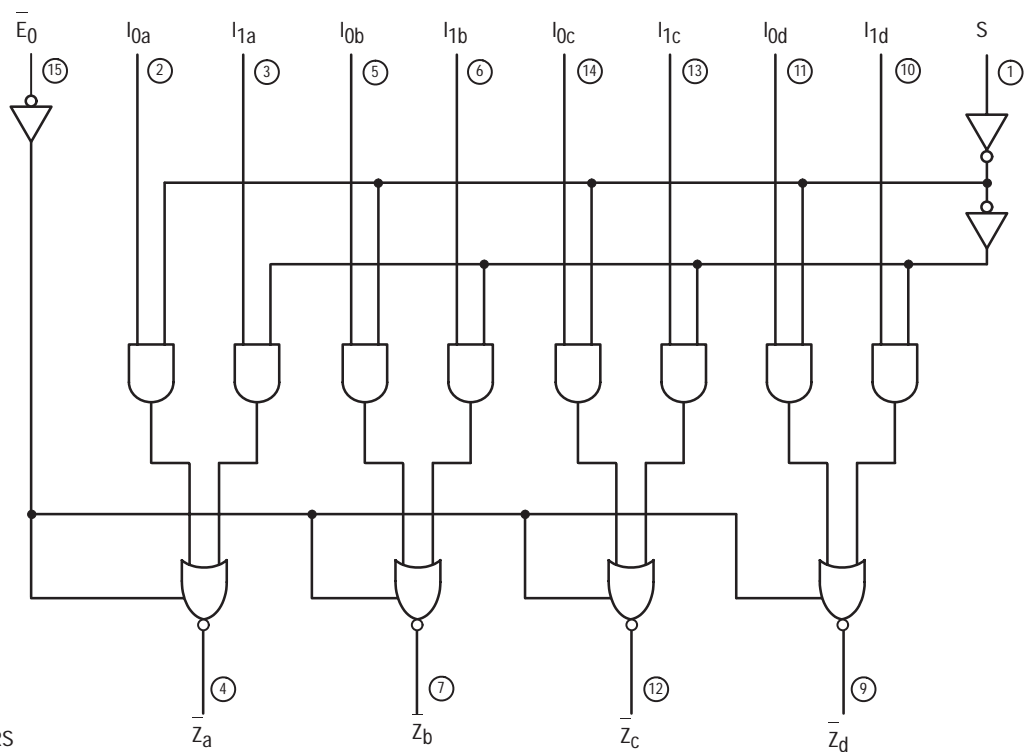
SN54/74LS257B • SN54/74LS258B

LOGIC DIAGRAMS

SN54/74LS257B



SN54/74LS258B



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

SN54/74LS257B • SN54/74LS258B

FUNCTIONAL DESCRIPTION

The LS257B and LS258B are Quad 2-Input Multiplexers with 3-state outputs. They select four bits of data from two sources each under control of a Common Data Select Input. When the Select Input is LOW, the I₀ inputs are selected and when Select is HIGH, the I₁ inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form for the LS257B and in the inverted form for the LS258B.

The LS257B and LS258B are the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are shown below:

When the Output Enable Input ($\overline{E_0}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LS257B

$$Z_a = \overline{E_0} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad Z_b = \overline{E_0} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad Z_d = E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

LS258B

$$Z_a = \overline{E_0} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad \overline{Z_b} = \overline{E_0} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = E_0 \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad \overline{Z_d} = E_0 \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS LS257B	OUTPUTS LS258B
$\overline{E_0}$	S	I ₀	I ₁	Z	\overline{Z}
H	X	X	X	(Z)	(Z)
L	H	X	L	L	H
L	H	X	H	H	L
L	L	L	X	L	H
L	L	H	X	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 (Z) = High Impedance (off)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS257B • SN54/74LS258B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current — HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current — LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current Other Inputs S Inputs				20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	Other Inputs S Inputs				0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current All Inputs				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH	LS257B			10	mA	V _{CC} = MAX	
		LS258B			9.0			
	Total, Output LOW	LS257B			16	mA		
	LS258B			14				
	Total, Output 3-State	LS257B			19	mA		
		LS258B			16			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V) See SN54LS251 for Waveforms

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			10 12	13 15	ns	Figures 1 & 2	C _L = 45 pF
t _{PLH} t _{PHL}	Propagation Delay, Select to Output			14 14	21 21			
t _{PZH}	Output Enable Time to HIGH Level			20	25	ns	Figures 4 & 5	C _L = 45 pF R _L = 667 Ω
t _{PZL}	Output Enable Time to LOW Level			20	25			
t _{PLZ}	Output Disable Time to LOW Level			16	25	ns	Figures 3 & 5	C _L = 5.0 pF R _L = 667 Ω
t _{PHZ}	Output Disable Time from HIGH Level			18	25			

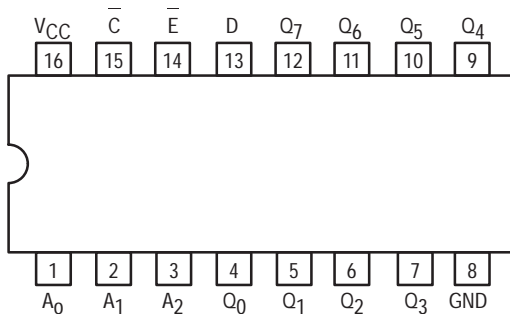


8-BIT ADDRESSABLE LATCH

The SN54/74LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

- Serial-to-Parallel Conversion
- Eight Bits of Storage With Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

A ₀ , A ₁ , A ₂	Address Inputs
D	Data Input
E	Enable (Active LOW) Input
C	Clear (Active LOW) input
Q ₀ to Q ₇	Parallel Latch Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
A ₀ , A ₁ , A ₂	0.5 U.L.	0.25 U.L.
D	0.5 U.L.	0.25 U.L.
E	1.0 U.L.	0.5 U.L.
C	0.5 U.L.	0.25 U.L.
Q ₀ to Q ₇	10 U.L.	5 (2.5) U.L.

NOTES:

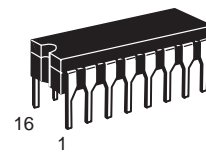
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

GUARANTEED OPERATING RANGES

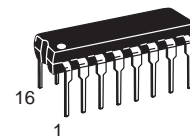
Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS259

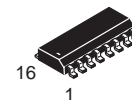
8-BIT ADDRESSABLE LATCH LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS259

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				36	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH}	Turn-Off Delay, Enable to Output			22	35	ns	C _L = 15 pF
t _{PHL}	Turn-On Delay, Enable to Output			15	24	ns	
t _{PLH}	Turn-Off Delay, Data to Output			20	32	ns	
t _{PHL}	Turn-On Delay, Data to Output			13	21	ns	
t _{PLH}	Turn-Off Delay, Address to Output			24	38	ns	
t _{PHL}	Turn-On Delay, Address to Output			18	29	ns	
t _{PHL}	Turn-On Delay, Clear to Output			17	27	ns	

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
t _s	Input Setup Time		20			ns
t _w	Pulse Width, Clear or Enable		15			ns
t _h	Hold Time, Data		5.0			ns
t _h	Hold Time, Address		20			ns

SN54/74LS259

AC WAVEFORMS

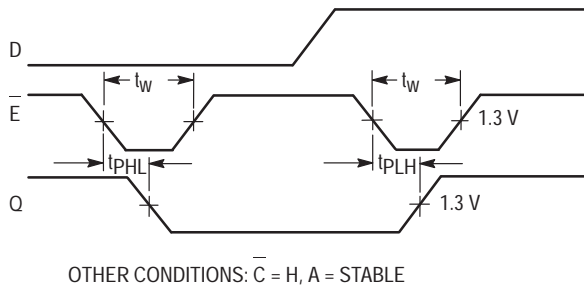


Figure 1. Turn-on and Turn-off Delays, Enable To Output and Enable Pulse Width

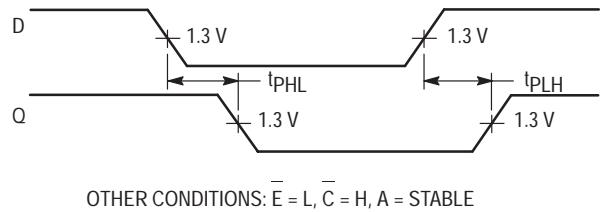


Figure 2. Turn-on and Turn-off Delays, Data to Output

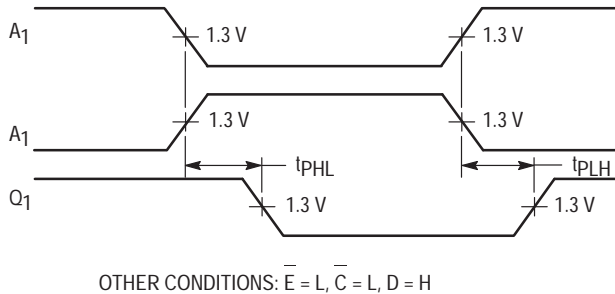


Figure 3. Turn-on and Turn-off Delays, Address to Output

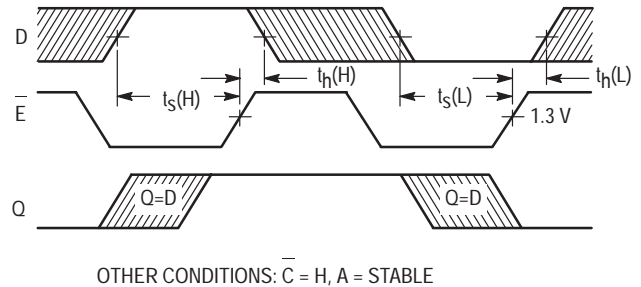


Figure 4. Setup and Hold Time, Data to Enable

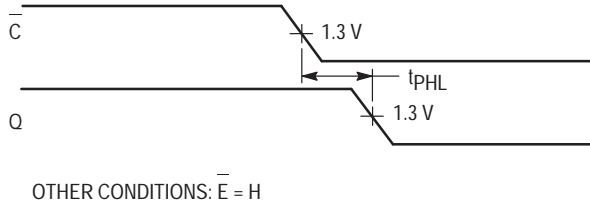


Figure 5. Turn-on Delay, Clear to Output

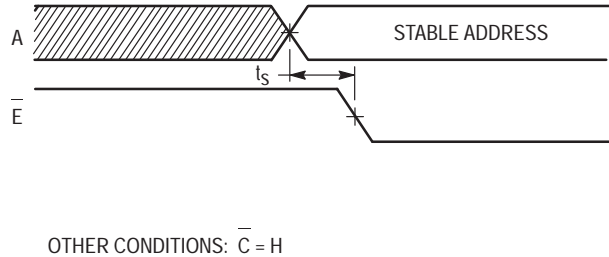


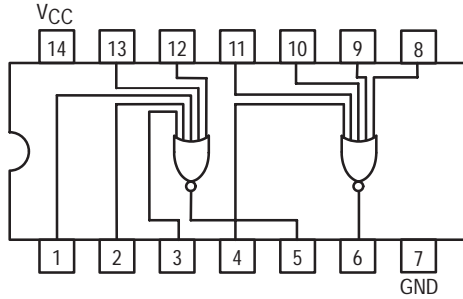
Figure 6. Setup Time, Address to Enable (See Notes 1 and 2)

NOTES:

1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

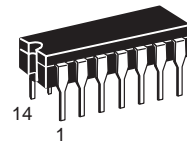


DUAL 5-INPUT NOR GATE

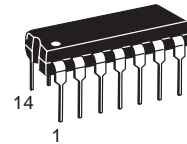


SN54/74LS260

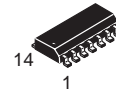
DUAL 5-INPUT NOR GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS260

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW			4.0	mA	$V_{CC} = \text{MAX}$	
				5.5			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

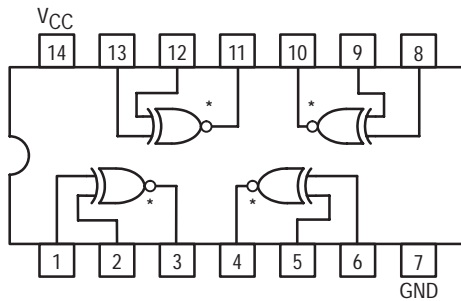
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		5.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PHL}	Turn-On Delay, Input to Output		6.0	15	ns	



QUAD 2-INPUT EXCLUSIVE NOR GATE

SN54/74LS266

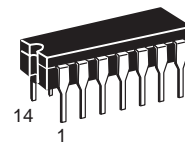
QUAD 2-INPUT EXCLUSIVE NOR GATE
LOW POWER SCHOTTKY



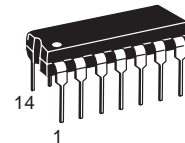
* OPEN COLLECTOR OUTPUTS

TRUTH TABLE

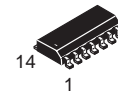
IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS266

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs		
		74		0.8				
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74			100	μA	V _{CC} = MIN, V _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current				40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{CC}	Power Supply Current				13	mA	V _{CC} = MAX	

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay, Other Input LOW			18 18	30 30	ns	V _{CC} = 5.0 V C _L = 15 pF, R _L = 2.0 kΩ	
t _{PLH} t _{PHL}	Propagation Delay, Other Input HIGH			18 18	30 30	ns		

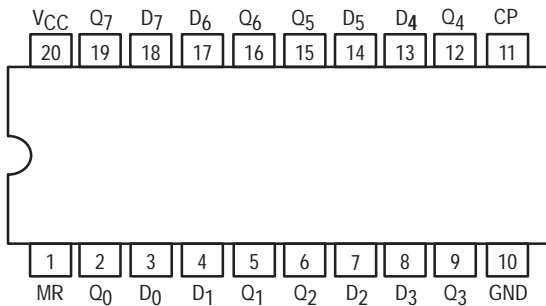


OCTAL D FLIP-FLOP WITH CLEAR

The SN54/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

CP Clock (Active HIGH Going Edge) Input
 D₀-D₇ Data Inputs
 MR Master Reset (Active LOW) Input
 Q₀-Q₇ Register Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
CP	0.5 U.L.	0.25 U.L.
D ₀ -D ₇	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q ₀ -Q ₇	10 U.L.	5 (2.5) U.L.

NOTES:

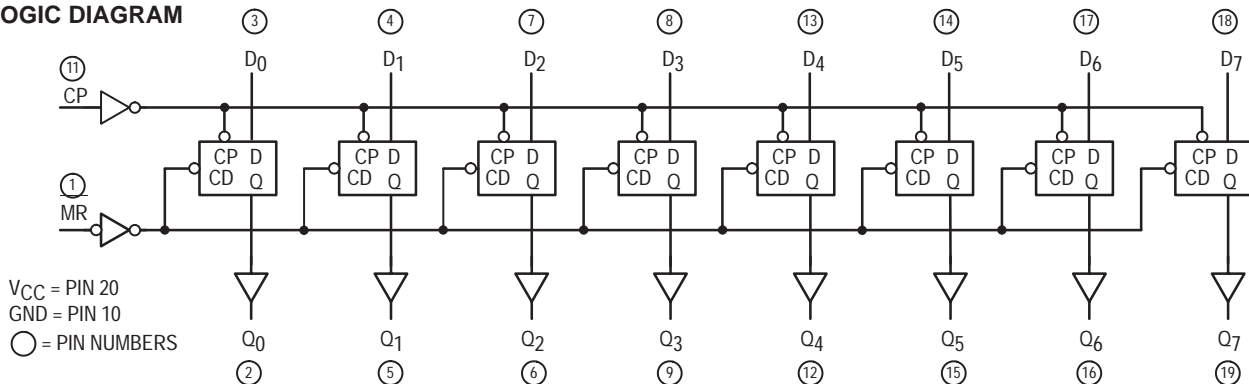
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

MR	CP	D _x	Q _x
L	X	X	L
H	⏏	H	H
H	⏏	L	L

H = HIGH Logic Level
 L = LOW Logic Level
 X = Immaterial

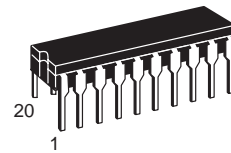
LOGIC DIAGRAM



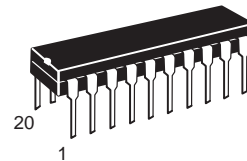
V_{CC} = PIN 20
 GND = PIN 10
 ○ = PIN NUMBERS

SN54/74LS273

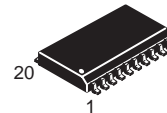
OCTAL D FLIP-FLOP WITH CLEAR
 LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03



DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

SN54/74LS273

FUNCTIONAL DESCRIPTION

The SN54/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the MR input is LOW, the Q outputs are LOW,

independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				27	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

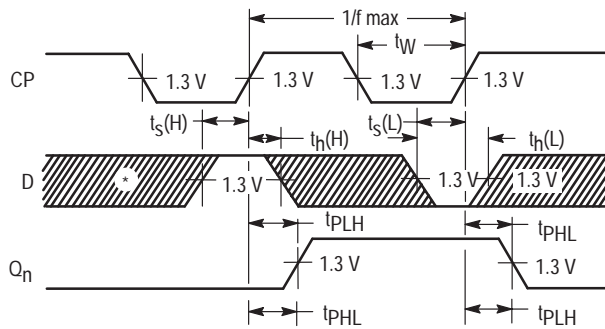
Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency		30	40		MHz	Figure 1
t _{PHL}	Propagation Delay, MR to Q Output			18	27	ns	Figure 2
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output			17	27	ns	Figure 1
				18	27		

SN54/74LS273

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_w	Pulse Width, Clock or Clear	20			ns	Figure 1
t_s	Data Setup Time	20			ns	Figure 1
t_h	Hold Time	5.0			ns	Figure 1
t_{rec}	Recovery Time	25			ns	Figure 2

AC WAVEFORMS



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock

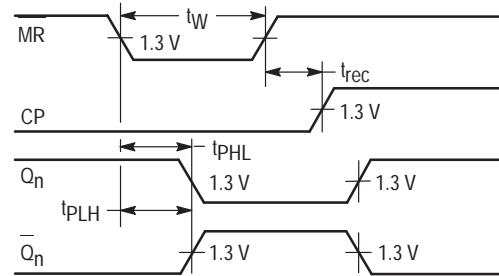


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

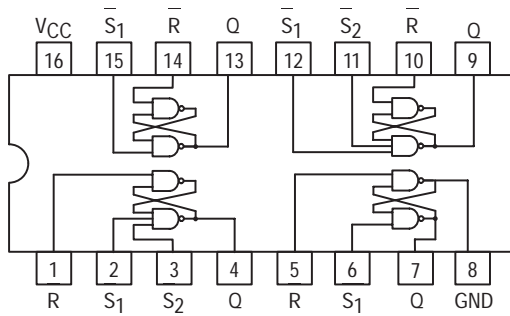
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.



QUAD SET-RESET LATCH



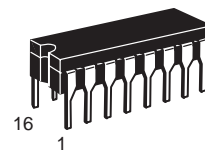
TRUTH TABLE

INPUT			OUTPUT (Q)
S ₁	S ₂	R	
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

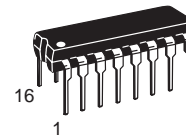
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S₁ or S₂ is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table

SN54/74LS279

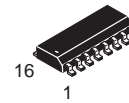
QUAD SET-RESET LATCH
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS279

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			7.0	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, \bar{S} to Output			22 21*	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Propagation Delay, R to Output			27	ns	

* Add 0.6 ns to spec limit for each 1.0 ns input rise time less than 15 ns.

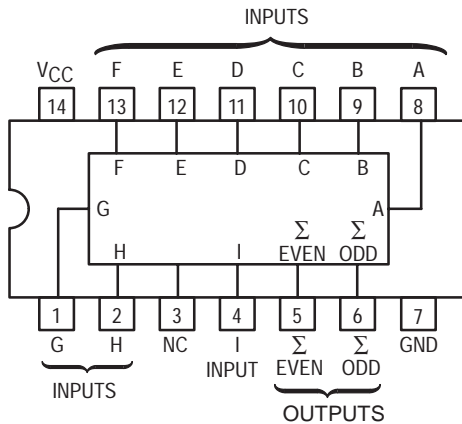


9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

The SN54/74LS280 is a Universal 9-Bit Parity Generator/Checker. It features odd/even outputs to facilitate either odd or even parity. By cascading, the word length is easily expanded.

The LS280 is designed without the expander input implementation, but the corresponding function is provided by an input at Pin 4 and the absence of any connection at Pin 3. This design permits the LS280 to be substituted for the LS180 which results in improved performance. The LS280 has buffered inputs to lower the drive requirements to one LS unit load.

- Generates Either Odd or Even Parity for Nine Data Lines
- Typical Data-to-Output Delay of only 33 ns
- Cascadable for n-Bits
- Can Be Used To Upgrade Systems Using MSI Parity Circuits
- Typical Power Dissipation = 80 mW



FUNCTION TABLE

NUMBER OF INPUTS A THRU 1 THAT ARE HIGH	OUTPUTS	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Level, L = LOW Level

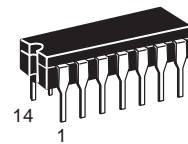
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

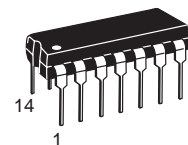
SN54/74LS280

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

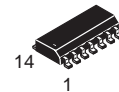
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



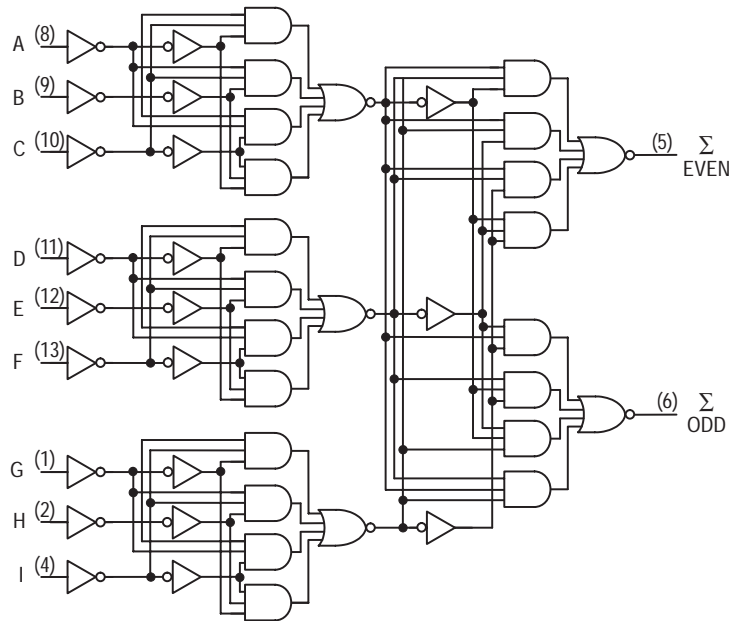
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

SN54/74LS280

FUNCTIONAL BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74	0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			27	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

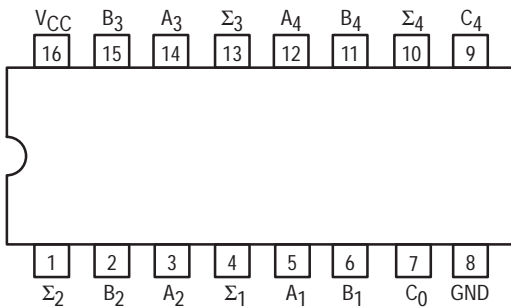
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Data to Output ΣEVEN		33 29	50 45	ns	$C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, Data to Output ΣODD		23 31	35 50	ns	



4-BIT BINARY FULL ADDER WITH FAST CARRY

The SN54/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4 , B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

- A_1-A_4 Operand A Inputs
- B_1-B_4 Operand B Inputs
- C_0 Carry Input
- $\Sigma_1-\Sigma_4$ Sum Outputs (Note b)
- C_4 Carry Output (Note b)

LOADING (Note a)

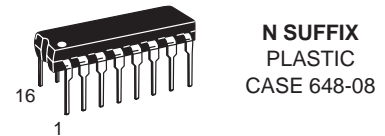
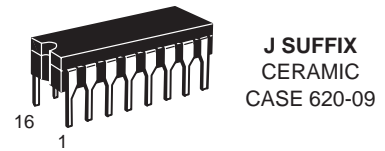
	HIGH	LOW
A_1-A_4	1.0 U.L.	0.5 U.L.
B_1-B_4	1.0 U.L.	0.5 U.L.
C_0	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	10 U.L.	5 (2.5) U.L.
C_4	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS283

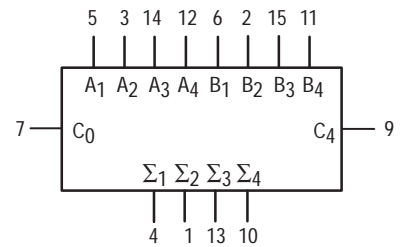
4-BIT BINARY FULL ADDER WITH FAST CARRY
LOW POWER SCHOTTKY



ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

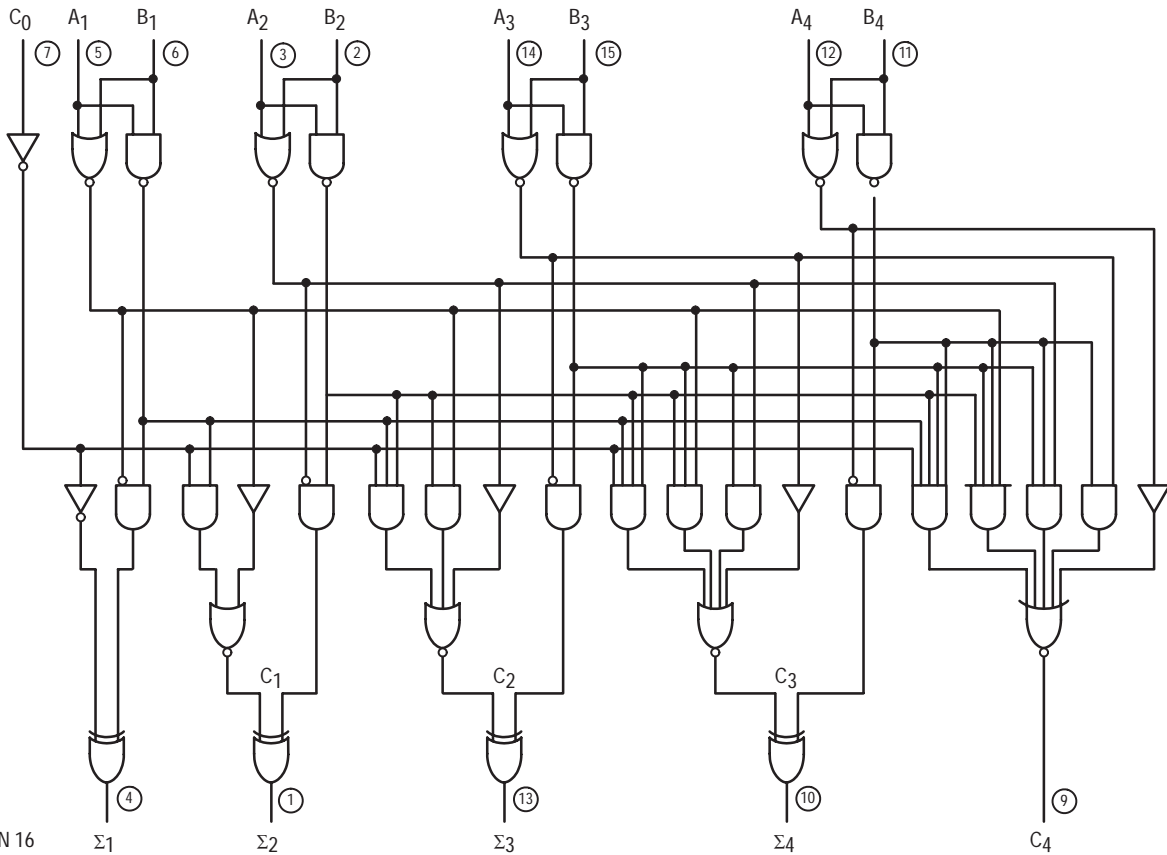
LOGIC SYMBOL



V_{CC} = PIN 16
 GND = PIN 8

SN54/74LS283

LOGIC DIAGRAM



VCC = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs ($\Sigma_1 - \Sigma_4$) and outgoing carry (C_4) outputs.

$$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C ₀	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C ₄
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10+9=19)

(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C₀, A₁, B₁, can be arbitrarily assigned to pins 7, 5 or 3.

SN54/74LS283

FUNCTIONAL TRUTH TABLE

C (n-1)	A _n	B _n	Σ _n	C _n
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

C₁ – C₃ are generated internally
 C₀ is an external input
 C₄ is an output generated internally

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	C ₀		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		Any A or B		40	μA		
		C ₀		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		Any A or B		0.2	mA		
I _{IL}	Input LOW Current	C ₀		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		Any A or B		-0.8	mA		
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total, Output HIGH			34	mA	V _{CC} = MAX	
	Total, Output LOW			39			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS283

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to Any Σ Output		16 15	24 24	ns	$C_L = 15\text{ pF}$ Figures 1 & 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 11	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	

AC WAVEFORMS

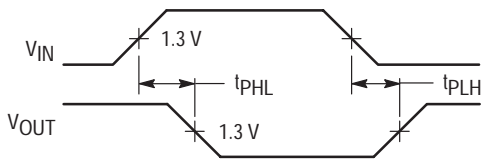


Figure 1

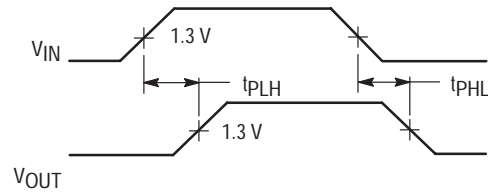


Figure 2

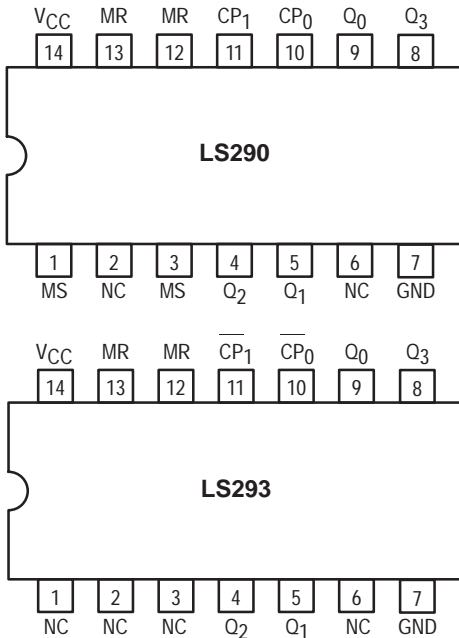


DECADE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS290 and SN54/74LS293 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS290) or divide-by-eight (LS293) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to CP) to form BCD, Bi-quinary, or Modulo-16 counters. Both of the counters have a 2-input gated Master Reset (Clear), and the LS290 also has a 2-input gated Master Set (Preset 9).

- Corner Power Pin Versions of the LS290 and LS293
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

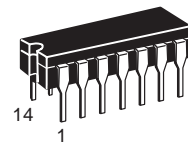
CP ₀	Clock (Active LOW going edge) Input to +2 Section.
CP ₁	Clock (Active LOW going edge) Input to +5 Section (LS290).
CP ₁	Clock (Active LOW going edge) Input to +8 Section (LS293).
MR ₁ , MR ₂	Master Reset (Clear) Inputs
MS ₁ , MS ₂	Master Set (Preset-9, LS290) Inputs
Q ₀	Output from +2 Section (Notes b & c)
Q ₁ , Q ₂ , Q ₃	Outputs from +5 & +8 Sections (Note b)

NOTES:

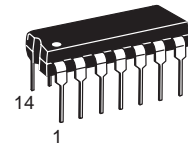
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
 c) The Q₀ Outputs are guaranteed to drive the full fan-out plus the CP₁ Input of the device.

SN54/74LS290 SN54/74LS293

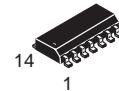
DECADE COUNTER; 4-BIT BINARY COUNTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

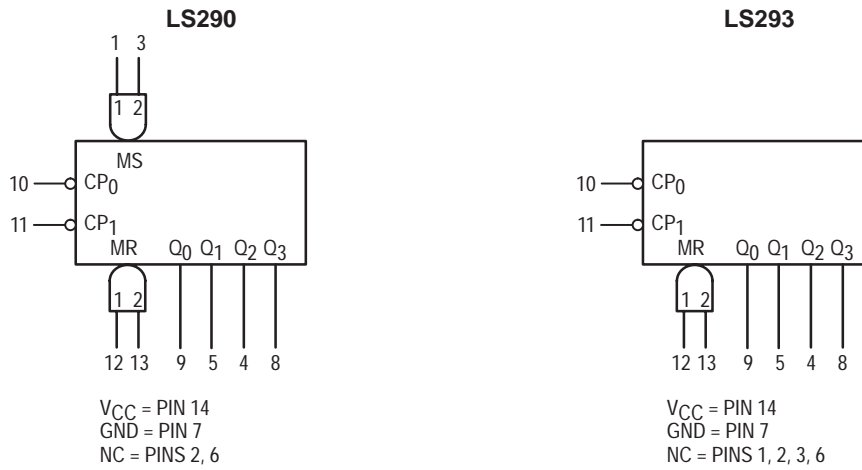
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOADING (Note a)

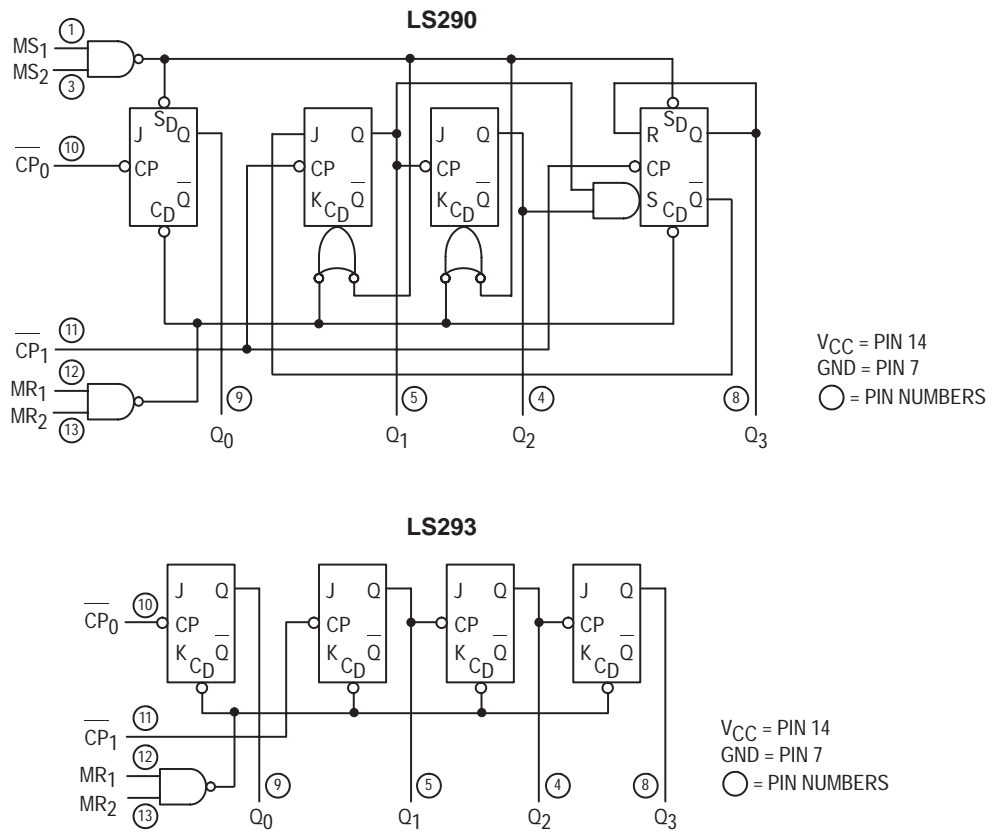
HIGH	LOW
0.05 U.L.	1.5 U.L.
0.05 U.L.	2.0 U.L.
0.05 U.L.	1.0 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

SN54/74LS290 • SN54/74LS293

LOGIC SYMBOL



LOGIC DIAGRAMS



SN54/74LS290 • SN54/74LS293

FUNCTIONAL DESCRIPTION

The LS290 and LS293 are 4-bit ripple type Decade, and 4-Bit Binary counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS290) or divide-by-eight (LS293) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q₀ output of each device is designed and specified to drive the rated fan-out plus the CP₁ input of the device.

A gated AND asynchronous Master Reset (MR₁ · MR₂) is provided on both counters which overrides the clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set (MS₁ · MS₂) is provided on the LS290 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes:

LS290

A. BCD Decade (8421) Counter — the CP₁ input must be

externally connected to the Q₀ output. The CP₀ input receives the incoming count and a BCD count sequence is produced.

- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q₃ output must be externally connected to the CP₀ input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at output Q₀.
- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (CP₀ as the input and Q₀ as the output). The CP₁ input is used to obtain binary divide-by-five operation at the Q₃ output.

LS293

A. 4-Bit Ripple Counter — The output Q₀ must be externally connected to input CP₁. The input count pulses are applied to input CP₀. Simultaneous division of 2, 4, 8, and 16 are performed at the Q₀, Q₁, Q₂, and Q₃ outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input CP₁. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q₁, Q₂, and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS290 MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X			Count	
X	L	X	L			Count	
L	X	X	L			Count	
X	L	L	X			Count	

LS293 MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H			Count	
H	L			Count	
L	L			Count	

LS290
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q₀ is connected to Input CP₁ for BCD count.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TRUTH TABLE

COUNT	OUTPUT			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q₀ connected to input CP₁.

SN54/74LS290 • SN54/74LS293

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current MS, MR CP ₀ CP ₁ (LS290) CP ₁ (LS293)			-0.4 -2.4 -3.2 -1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			15	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS290 • SN54/74LS293

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, $C_L = 15\text{ pF}$)

Symbol	Parameter	Limits						Unit
		LS290			LS293			
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}	$\overline{\text{CP}}_0$ Input Clock Frequency	32			32			MHz
f_{MAX}	$\overline{\text{CP}}_1$ Input Clock Frequency	16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{\text{CP}}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_0$ Input to Q_3 Output		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_2 Output		21 23	32 35		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{\text{CP}}_1$ Input to Q_3 Output		21 23	32 35		34 34	51 51	ns
t_{PHL}	MS Input to Q_0 and Q_3 Outputs		20	30				ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40				ns
t_{PHL}	MR Input to Any Output		26	40		26	40	ns

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits				Unit
		LS290		LS293		
		Min	Max	Min	Max	
t_W	$\overline{\text{CP}}_0$ Pulse Width	15		15		ns
t_W	$\overline{\text{CP}}_1$ Pulse Width	30		30		ns
t_W	MS Pulse Width	15				ns
t_W	MR Pulse Width	15		15		ns
t_{rec}	Recovery Time MR to CP	25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVEFORMS

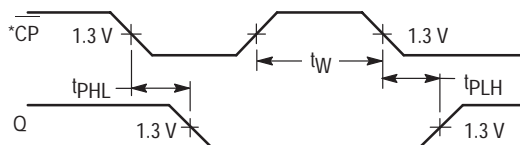


Figure 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

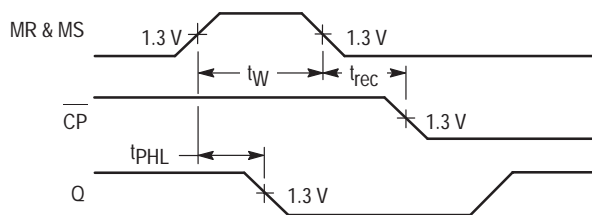


Figure 2

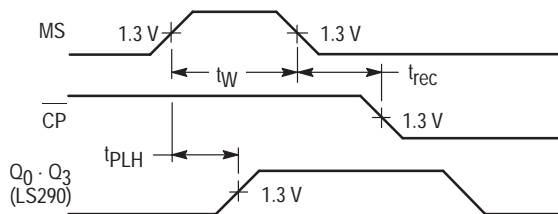


Figure 3



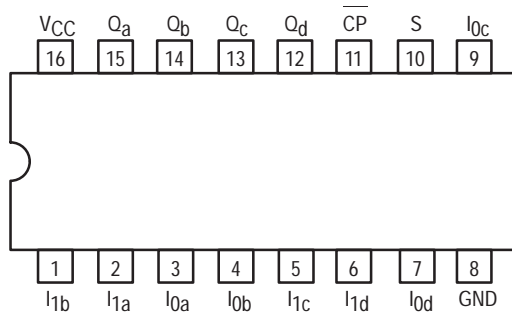
QUAD 2-INPUT MULTIPLEXER WITH STORAGE

The SN54/74LS298 is a Quad 2-Port Register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources.) The selected data is transferred to the output register synchronous with the HIGH to LOW transition of the Clock input.

The LS298 is fabricated with the Schottky barrier process for high speed and is completely compatible with all Motorola TTL families.

- Select From Two Data Sources
- Fully Edge-Triggered Operation
- Typical Power Dissipation of 65 mW
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

<u>S</u>	Common Select Input
<u>CP</u>	Clock (Active LOW Going Edge) Input
I _{0a} -I _{0d}	Data Inputs From Source 0
I _{1a} -I _{1d}	Data Inputs From Source 1
Q _a -Q _d	Register Outputs (Note b)

LOADING (Note a)

LOADING (Note a)	
HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

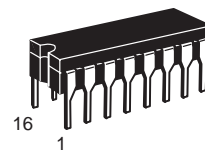
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

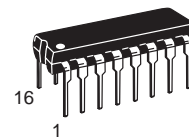
SN54/74LS298

QUAD 2-INPUT MULTIPLEXER WITH STORAGE

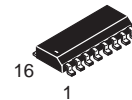
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

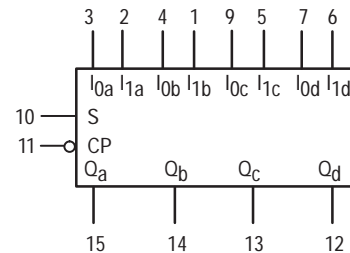


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

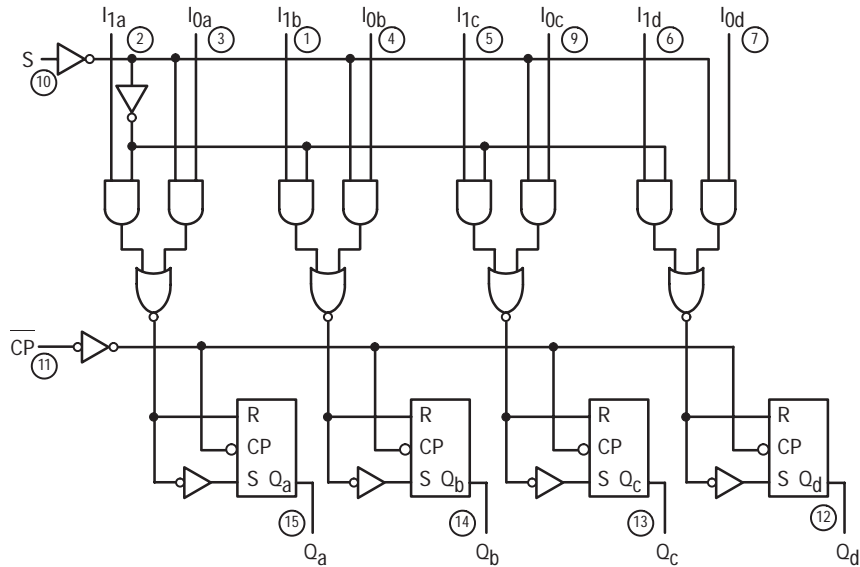
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS298

LOGIC OR BLOCK DIAGRAM



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

FUNCTIONAL DESCRIPTION

The LS298 is a high speed Quad 2-Port Register. It selects four bits of data from two sources (ports) under the control of a Common Select Input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH to LOW

transition of the Clock input (\overline{CP}). The 4-bit output register is fully edge-triggered. The Data inputs (I) and Select input (S) must be stable only one setup time prior to the HIGH to LOW transition of the clock for predictable operation.

TRUTH TABLE

INPUTS			OUTPUT
S	I ₀	I ₁	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Don't Care
 l = LOW Voltage Level one setup time prior to the HIGH to LOW clock transition.
 h = HIGH Voltage Level one setup time prior to the HIGH to LOW clock transition.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS298

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				21	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output			18	27	ns	V _{CC} = 5.0 V, C _L = 15 pF
				21	32	ns	

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _W	Clock Pulse Width		20			ns	V _{CC} = 5.0 V
t _S	Data Setup Time		15			ns	
t _S	Select Setup Time		25			ns	
t _H	Data Hold Time		5.0			ns	
t _H	Select Hold Time		0				

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following

the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

SN54/74LS298

AC WAVEFORMS

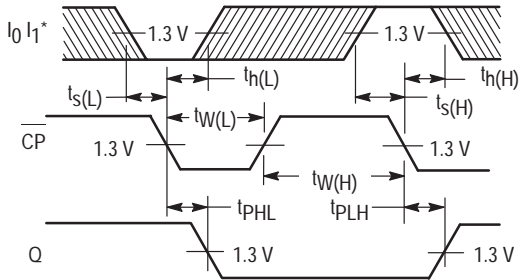


Figure 1

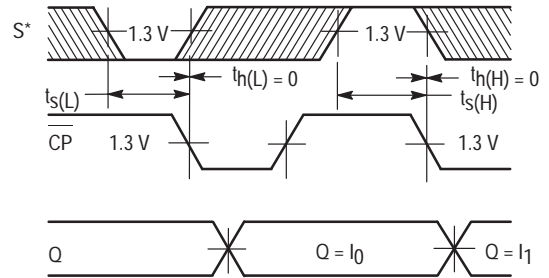


Figure 2

*The shaded areas indicate when the input is permitted to change for predictable output performance.



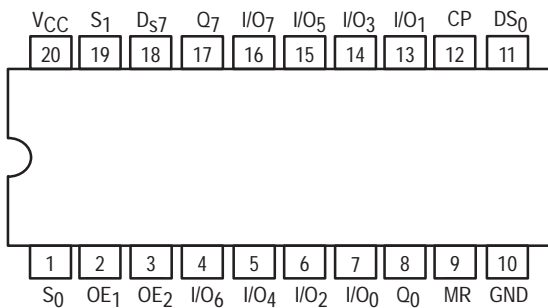
8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

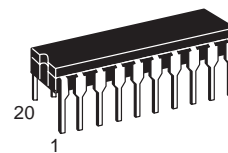


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

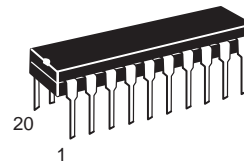
SN54/74LS299

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

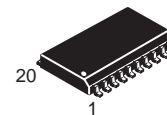
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

PIN NAMES

CP	Clock Pulse (active positive-going edge) Input
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
I/O _n	Parallel Data Input or Parallel Output (3-State) (Note c)
$\overline{OE}_1, \overline{OE}_2$	3-State Output Enable (active LOW) Inputs
Q ₀ , Q ₇	Serial Outputs (Note b)
MR	Asynchronous Master Reset (active LOW) Input
S ₀ , S ₁	Mode Select Inputs

NOTES:

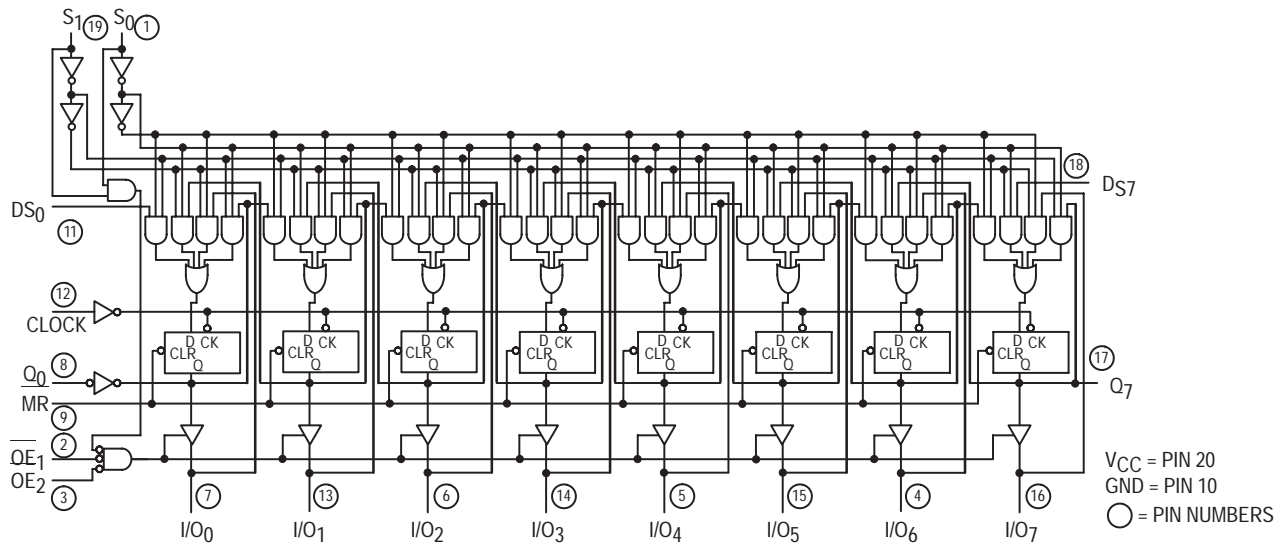
- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74). The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 (25) U.L.	15 (7.5) U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
0.5 U.L.	0.25 U.L.
1 U.L.	0.5 U.L.

SN54/74LS299

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								RESPONSE
MR	S ₁	S ₀	OE ₁	OE ₂	CP	DS ₀	DS ₇	
L	X	X	H	X	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage LOW
L	X	L	L	L	X	X	X	
H	L	H	X	X	↯	D	X	Shift Right; D → Q ₀ ; Q ₀ → Q ₁ ; etc.
H	L	H	L	L	↯	D	X	Shift Right; D → Q ₀ & I/O ₀ ; Q ₀ → Q ₁ & I/O ₁ ; etc.
H	H	L	X	X	↯	X	D	Shift Left; D → Q ₇ ; Q ₇ → Q ₆ ; etc.
H	H	L	L	L	↯	X	D	Shift Left; D → Q ₇ & I/O ₇ ; Q ₇ → Q ₆ & I/O ₆ ; etc.
H	H	H	X	X	↯	X	X	Parallel Load; I/O _n → Q _n
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O _n = Q _n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	Q ₀ , Q ₇	54, 74		-0.4	mA
I _{OL}	Output Current — Low	Q ₀ , Q ₇	54		4.0	mA
		Q ₀ , Q ₇	74		8.0	
I _{OH}	Output Current — High	I/O ₀ –I/O ₇	54		-1.0	mA
		I/O ₀ –I/O ₇	74		-2.6	
I _{OL}	Output Current — Low	I/O ₀ –I/O ₇	54		12	mA
		I/O ₀ –I/O ₇	74		24	

SN54/74LS299

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage I/O ₀ -I/O ₇	54	2.4	3.2		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.4	3.1		V		
V _{OH}	Output HIGH Voltage Q ₀ , Q ₇	54	2.5	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.7	3.4		V		
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇	54, 74			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74			0.5	V	I _{OL} = 8.0 mA	
I _{OZH}	Output Off Current HIGH I/O ₀ -I/O ₇				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW I/O ₀ -I/O ₇				-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	Others			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		S ₀ , S ₁ , I/O ₀ -I/O ₇			40	μA		
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		S ₀ , S ₁ I/O ₀ -I/O ₇			0.2	mA		
I _{IL}	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		S ₀ , S ₁			-0.8	mA		
I _{OS}	Short Circuit Current (Note 1)	Q ₀ , Q ₇	-20		-100	mA	V _{CC} = MAX	
		I/O ₀ -I/O ₇	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				53	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS299

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	C _L = 15 pF
t _{PHL} t _{PLH}	Propagation Delay, Clock to Q ₀ or Q ₇		26 22	39 33	ns	
t _{PHL}	Propagation Delay, Clear to Q ₀ or Q ₇		27	40	ns	
t _{PHL} t _{PLH}	Propagation Delay, Clock to I/O ₀ –I/O ₇		26 17	39 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PHL}	Propagation Delay, Clear to I/O ₀ –I/O ₇		26	40	ns	
t _{PZH} t _{PZL}	Output Enable Time		13 19	21 30	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		10 10	15 15	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width HIGH	25			ns	V _{CC} = 5.0 V
t _W	Clock Pulse Width LOW	13			ns	
t _W	Clear Pulse Width LOW	20			ns	
t _S	Data Setup Time	20			ns	
t _S	Select Setup Time	35			ns	
t _H	Data Hold Time	0			ns	
t _H	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

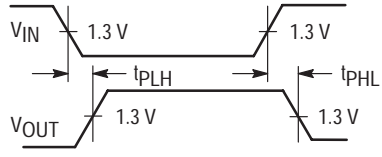


Figure 1

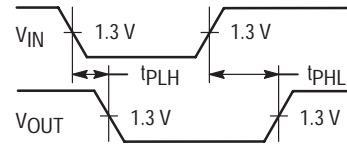


Figure 2

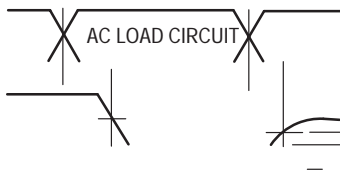


Figure 3

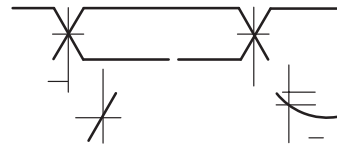


Figure 4

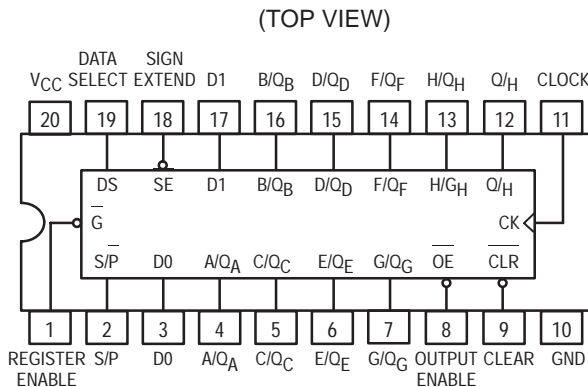
Figure 5



8-BIT SHIFT REGISTERS WITH SIGN EXTEND

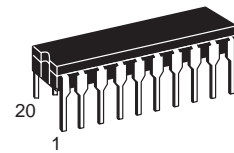
These 8-bit shift registers have multiplexed input/output data ports to accomplish full 8-bit data handling in a single 20-pin package. Serial data may enter the shift-right register through either D0 or D1 inputs as selected by the data select pin. A serial output is also provided. Synchronous parallel loading is achieved by taking the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data is entered on the low-to-high clock transition. The data extend function repeats the sign in the Q_A flip-flop during shifting. An overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not affect synchronous operation of the register.

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Sign Extend Function
- Direct Overriding Clear
- 3-State Outputs Drive Bus Lines Directly

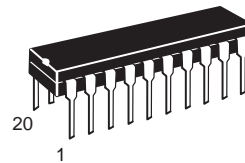


SN54/74LS322A

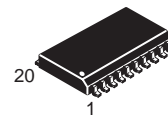
8-BIT SHIFT REGISTERS WITH SIGN EXTEND
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

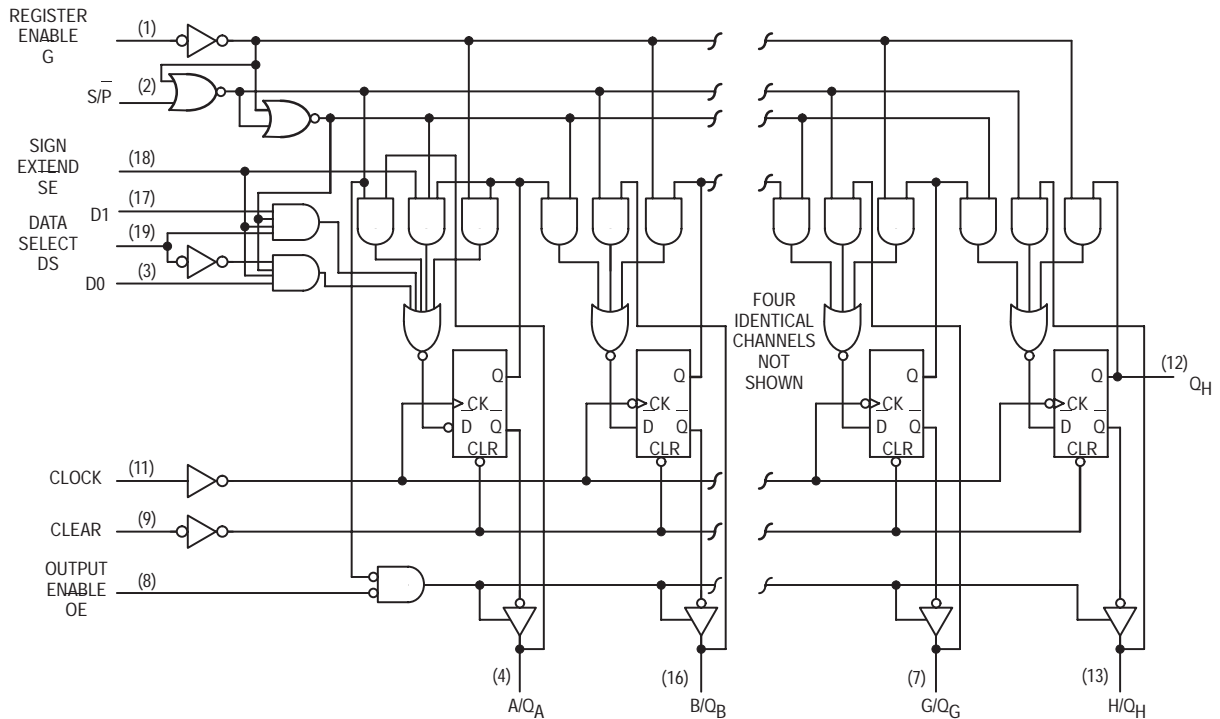
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	Q _H '	54, 74		-0.4	mA
I _{OL}	Output Current — Low	Q _H ' Q _H '	54 74		4.0 8.0	mA
I _{OH}	Output Current — High	Q _A -Q _H Q _A -Q _H	54 74		-1.0 -2.6	mA
I _{OL}	Output Current — Low	Q _A -Q _H Q _A -Q _H	54 74		12 24	mA

SN54/74LS322A

BLOCK DIAGRAM



FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT QH'
	CLEAR	REGISTER ENABLE	S/P	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/QA	B/QB	C/QC ... H/QH		
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	QA0	QB0	QC0	QH0	QH0
Shift Right	H	L	H	H	L	L	↑	D0	QAn	QBn	QGn	QGn
	H	L	H	H	H	L	↑	D1	QAn	QBn	QGn	QGn
Sign Extend	H	L	H	L	X	L	↑	QAn	QAn	QBn	QGn	QGn
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = HIGH Level (steady state)

L = LOW Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from LOW to HIGH level

QA0...QH0 = the level of QA through QH, respectively, before the indicated steady-state conditions were established

QAn...QHn = the level of QA through QH, respectively, before the most recent ↑ transition of the clock

D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively

a...h = the level of steady-state inputs at inputs A through H respectively

SN54/74LS322A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage Q _A -Q _H	54	2.4	3.2		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.4	3.2		V		
V _{OH}	Output HIGH Voltage Q _H '	54	2.5	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.7	3.4		V		
V _{OL}	Output LOW Voltage Q _A -Q _H	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage Q _H '	54, 74			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74			0.5	V	I _{OL} = 8.0 mA	
I _{OZH}	Output Off Current HIGH Q _A -Q _H				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW Q _A -Q _H				-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	Other			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		A-H, Data Select			40	μA		
		Sign Extend			60	μA		
		Other			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		Data Select			0.2	mA		
		Sign Extend			0.3	mA		
		A-H			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
I _{IL}	Input LOW Current	Other			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		Data Select			-0.8	mA		
		Sign Extend			-1.2	mA		
I _{OS}	Short Circuit Current (Note 1)	Q _H '	-20		-100	mA	V _{CC} = MAX	
		Q _A -Q _H	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				60	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS322A

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	C _L = 15 pF
t _{PHL} t _{PLH}	Propagation Delay, Clock to Q _H '		26 22	35 33	ns	
t _{PHL}	Propagation Delay, Clear to Q _H '		27	35	ns	
t _{PHL} t _{PLH}	Propagation Delay, Clock to Q _A -Q _H		22 16	33 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PHL}	Propagation Delay, Clear to Q _A -Q _H		22	35	ns	
t _{PZH} t _{PZL}	Output Enable Time		15 15	35 35	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		15 15	25 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width HIGH	25			ns	V _{CC} = 5.0 V
t _W	Clock Pulse Width LOW	15			ns	
t _W	Clear Pulse Width LOW	20			ns	
t _S	Data Setup Time	20			ns	
t _S	Select Setup Time	15			ns	
t _H	Data Hold Time	0			ns	
t _H	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.



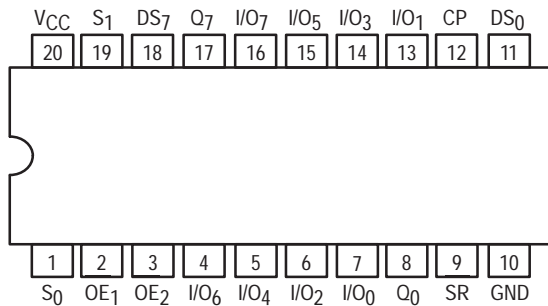
8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS323 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Its function is similar to the SN54/74LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading.

Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Parallel Load and Store
- Separate Continuous Inputs and Outputs from Q₀ and Q₇ Allow Easy Cascading
- Fully Synchronous Reset
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

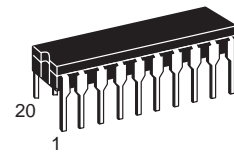


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

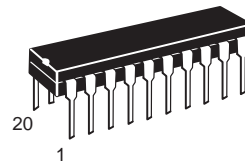
SN54/74LS323

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

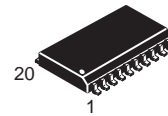
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

PIN NAMES

CP	Clock Pulse (active positive going edge) Input
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
I/O _n	Parallel Data Input or Parallel Output (3-State) (Note c)
OE ₁ , OE ₂	3-State Output Enable (active LOW) Inputs
Q ₀ , Q ₇	Serial Outputs (Note b)
S ₀ , S ₁	Mode Select Inputs
SR	Synchronous Reset (active LOW) Input

NOTES:

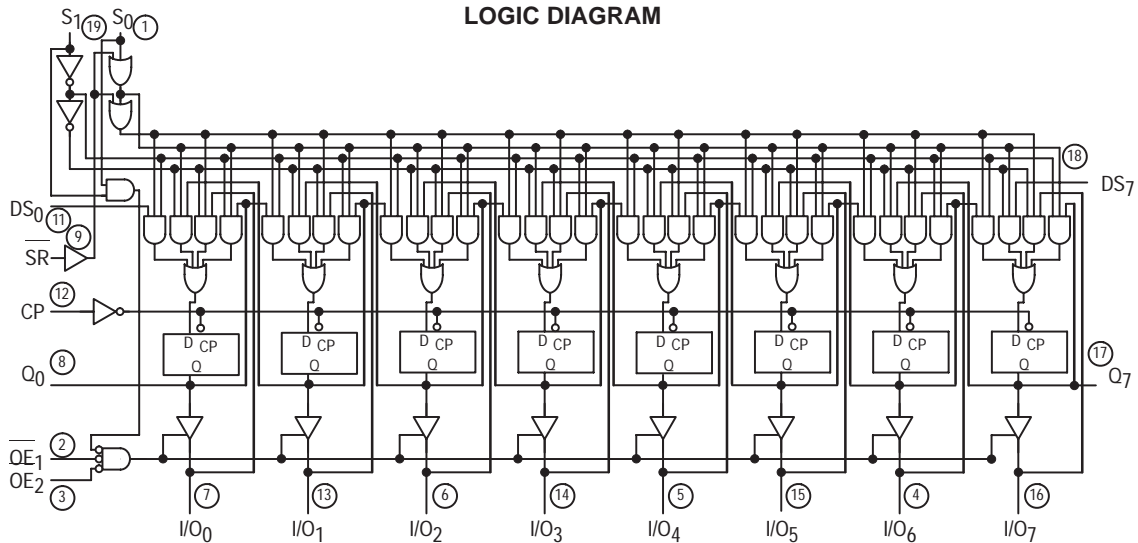
- 1 TTL LOAD = 40 μA HIGH/1.6 mA LOW.
- The output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial Temperature Ranges.
- The output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial Temperature Ranges. The output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial Temperature Ranges.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
1.0 U.L.	0.5 U.L.
65 (25) U.L.	15 (7.5) U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
1 U.L.	
0.5 U.L.	0.25 U.L.

SN54/74LS323

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The logic diagram and truth table indicate the functional characteristics of the SN54/74LS323 Universal Shift/Storage Register. This device is similar in operation to the SN54/74LS299 except for synchronous reset. A partial list of the common features are described below:

1. They use eight D-type edge-triggered flip-flops that respond only to the LOW-to-HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control (S_0, S_1) and data inputs ($DS_0, DS_7, I/O_0-I/O_7$) may be stable at least a setup time prior to the positive transition of the Clock Pulse.
2. When $S_0 = S_1 = 1$, $I/O_0-I/O_7$ are parallel inputs to flip-flops Q_0-Q_7 respectively, and the outputs of Q_0-Q_7 are in the high impedance state regardless of the state of OE_1 or OE_2 .

An important unique feature of the SN54/74LS323 is a fully Synchronous Reset that requires only to be stable at least one setup time prior to the positive transition of the Clock Pulse.

TRUTH TABLE

INPUTS								RESPONSE
SR	S_1	S_0	OE_1	OE_2	CP	DS_0	DS_7	
L	X	X	H	X	\downarrow	X	X	Synchronous Reset; $Q_0 = Q_7 = \text{LOW}$ I/O voltage undetermined
L	X	X	X	H	\downarrow	X	X	
L	H	H	X	X	\downarrow	X	X	
L	L	X	L	L	\downarrow	X	X	Synchronous Reset; $Q_0 = Q_7 = \text{LOW}$ I/O voltage LOW
L	X	L	L	L	\downarrow	X	X	
H	L	H	X	X	\downarrow	D	X	Shift Right; $D \rightarrow Q_0; Q_0 \rightarrow Q_1$; etc.
H	L	H	L	L	\downarrow	D	X	Shift Right; $D \rightarrow Q_0 \ \& \ I/O_0; Q_0 \rightarrow Q_1 \ \& \ I/O_1$; etc.
H	H	L	X	X	\downarrow	X	D	Shift Left; $D \rightarrow Q_7; Q_7 \rightarrow Q_6$; etc.
H	H	L	L	L	\downarrow	X	D	Shift Left; $D \rightarrow Q_7 \ \& \ I/O_7; Q_7 \rightarrow Q_6 \ \& \ I/O_6$; etc.
H	H	H	X	X	\downarrow	X	X	Parallel Load $I/O_n \rightarrow Q_n$
H	L	L	H	X	X	X	X	Hold; I/O Voltage Undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold; $I/O_n = Q_n$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN54/74LS323

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	Q ₀ , Q ₇	54, 74		-0.4	mA
I _{OL}	Output Current — Low	Q ₀ , Q ₇	54		4.0	mA
		Q ₀ , Q ₇	74		8.0	
I _{OH}	Output Current — High	I/O ₀ –I/O ₇	54		-1.0	mA
		I/O ₀ –I/O ₇	74		-2.6	
I _{OL}	Output Current — Low	I/O ₀ –I/O ₇	54		12	mA
		I/O ₀ –I/O ₇	74		24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage I/O ₀ –I/O ₇	54	2.4	3.2		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.4	3.1		V		
V _{OH}	Output HIGH Voltage Q ₀ , Q ₇	54	2.5	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.7	3.4		V		
V _{OL}	Output LOW Voltage I/O ₀ –I/O ₇	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage Q ₀ –Q ₇	54, 74			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74			0.5	V	I _{OL} = 8.0 mA	
I _{OZH}	Output Off Current HIGH I/O ₀ –I/O ₇				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW I/O ₀ –I/O ₇				-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	Others			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		S ₀ , S ₁ , I/O ₀ –I/O ₇			40	μA		
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		S ₀ , S ₁ I/O ₀ –I/O ₇			0.2	mA		
I _{IL}	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		S ₀ , S ₁			-0.8	mA		
I _{OS}	Short Circuit Current (Note 1)	Q ₀ , Q ₇	-20		-100	mA	V _{CC} = MAX	
		I/O ₀ –I/O ₇	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				53	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS323

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	C _L = 15 pF
t _{PHL} t _{PLH}	Propagation Delay, Clock to I/O ₀ or Q ₇		26 22	39 33	ns	
t _{PHL} t _{PLH}	Propagation Delay, Clock to I/O ₀ –I/O ₇		25 17	39 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PZH} t _{PZL}	Output Enable Time		14 20	21 30	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		10 10	15 15	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width HIGH	25			ns	V _{CC} = 5.0 V
t _W	Clock Pulse Width LOW	15			ns	
t _W	Clear Pulse Width LOW	20			ns	
t _S	Data Setup Time	20			ns	
t _S	Select Setup Time	35			ns	
t _H	Data Hold Time	0			ns	
t _H	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

SN54/74LS323

3-STATE WAVEFORMS

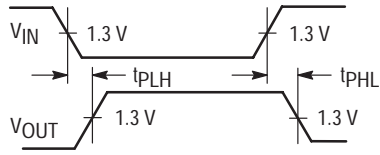


Figure 1

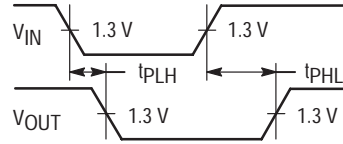


Figure 2

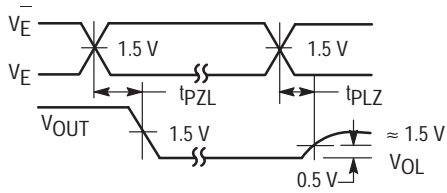


Figure 3

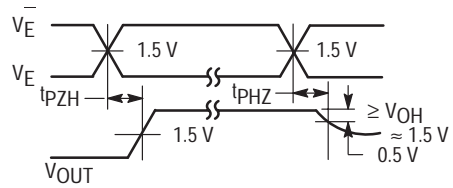
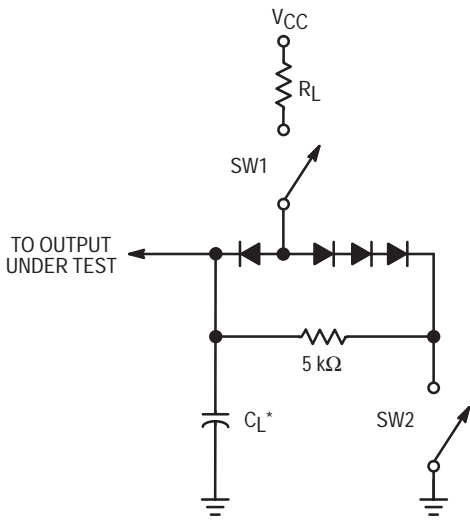


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed



8-INPUT PRIORITY ENCODERS WITH 3-STATE OUTPUTS

The SN54/74LS348 and the SN54/74LS848 are eight input priority encoders which provide the 8-line to 3-line function.

The outputs (A0–A2) and inputs (0–7) are active low. The active low input which has the highest priority (input 7 has the highest) is represented on the outputs (output A0 is the lowest bit). An example would be if inputs 1, 2 and 4 were low, then a binary 4 would be represented on the outputs.

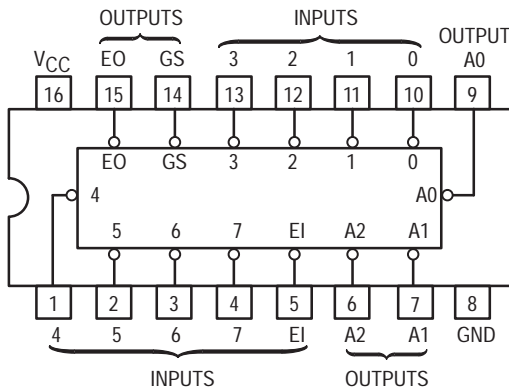
The GS (Group Signal) output is active low when any of the inputs are low. It serves to indicate when any of the inputs are active.

A0, A1 and A2 are three-state outputs. This allows for up to 64 line expansion without the need for special external circuitry.

A logical one on the Enable Input (EI) forces A0, A1 and A2 to the disabled state and outputs GS and EO to the high state. A high on all data inputs (0–7) together with a low on the EI input disables outputs A0, A1, and A2 and forces output GS to the high state and output EO to the low state.

Use of the EI input in conjunction with the EO output provides for the capability of having priority encoding of n input signals.

The LS848 has special internal circuitry providing for a greatly reduced negative going glitch on the GS (Group Signal) output and on a reduced tendency for the A0, A1 and A2 outputs to become momentarily enabled. Both of these occurrences happen when the EI input goes from a logical one to a logical zero and all data inputs (0–7) are held at logical ones. The internal glitch reduction circuitry does add an additional fan-in of one on all data inputs (compared to that of the LS348).



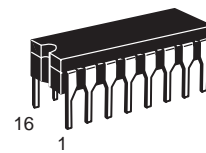
FUNCTION TABLE

		INPUTS								OUTPUTS					
		EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
	L	H	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
	L	X	X	X	X	X	X	X	L	H	L	L	L	L	H
	L	X	X	X	X	X	L	H	H	H	L	H	L	L	H
	L	X	X	X	X	L	H	H	H	H	L	H	H	L	H
	L	X	X	X	L	H	H	H	H	H	H	L	L	L	H
	L	X	X	L	H	H	H	H	H	H	H	L	H	L	H
	L	X	L	H	H	H	H	H	H	H	H	H	L	L	H
	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H

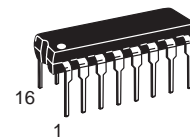
SN54/74LS348
SN54/74LS848

8-INPUT PRIORITY ENCODERS WITH 3-STATE OUTPUTS

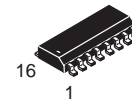
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

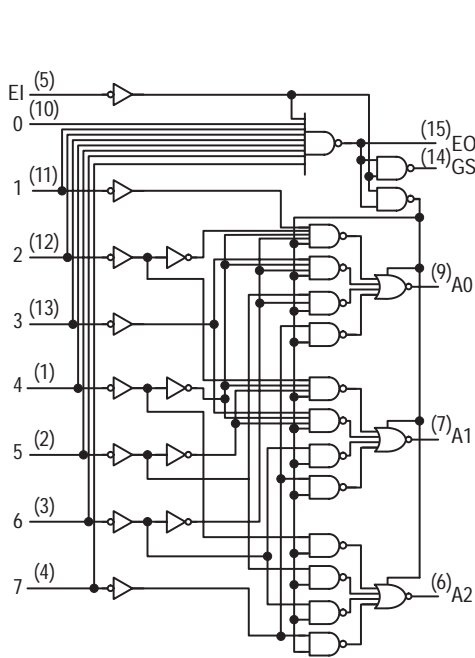
ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

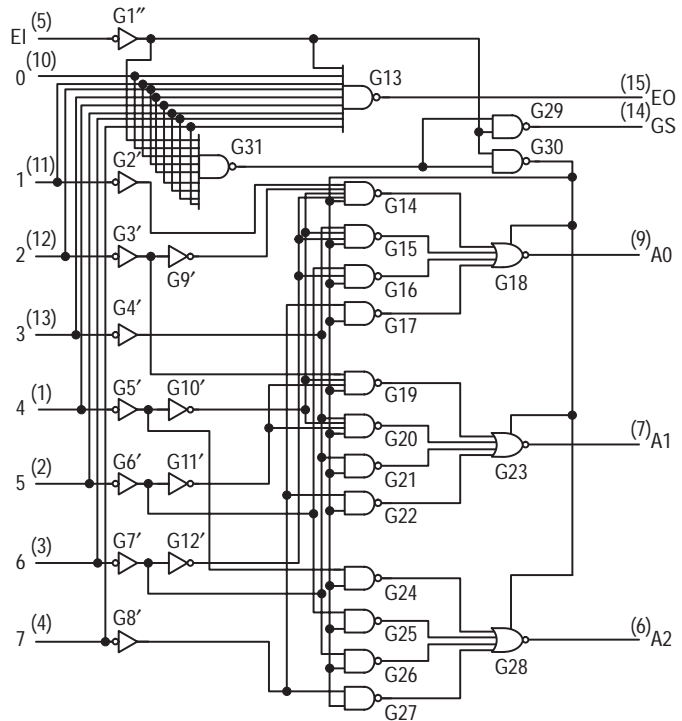
H = HIGH Logic Level
L = LOW Logic Level
X = Irrelevant
Z = High Impedance State

SN54/74LS348 • SN54/74LS848

BLOCK DIAGRAMS



SN54/74LS348



SN54/74LS848

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	EO, GS	54, 74		-0.4	mA
I _{OH}	Output Current — High	A0, A1, A2	54		-1.0	mA
		A0, A1, A2	74		-2.6	
I _{OL}	Output Current — Low	EO, GS	54		4.0	mA
			74		8.0	
I _{OL}	Output Current — Low	A0, A1, A2	54		12	mA
		A0, A1, A2	74		24	

SN54/74LS348 • SN54/74LS848

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage A0, A1, A2	54, 74	2.4	3.1		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
	EO, GS	54	2.5	3.5		V		
	EO, GS	74	2.7	3.5		V		
V _{OL}	Output LOW Voltage EO, GS	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
V _{OL}	Output LOW Voltage A0, A1, A2	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					40	μA		
					40	μA		
					60	μA		
	Input HIGH Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
					0.2	mA		
I _{IL}	Input LOW Current Input 0, EI — LS348 Input 0 — LS848 Other — LS348 Other — LS848				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
					-0.8	mA		
					-0.8	mA		
					-1.2	mA		
I _{OS}	Short Circuit Current (Note 1) EO, GS A0, A1, A2		-20		-120	mA	V _{CC} = MAX	
			-30		-130	mA		
I _{CC}	Power Supply Current Total, Output HIGH			12	23	mA	V _{CC} = MAX All Inputs and Outputs Open	
	Total, Output LOW			13	25		V _{CC} = MAX, Inputs 7, EI = GND All Others Open	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS348 • SN54/74LS848

AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$)

Symbol	From (Input)	To (Output)	Waveform	LS348 Limits			LS848 Limits			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max		
t _{PLH}	1 thru 7	A0, A1 or A2	In-Phase output		11	17		12	18	ns	C _L = 45 pF R _L = 667 Ω
t _{PHL}					20	30		20	30		
t _{PLH}	1 thru 7	A0, A1 or A2	Out-of-Phase output		23	35		23	35	ns	
t _{PHL}					23	35		23	35		
t _{PZH}	EI	A0, A1 or A2			25	39		25	39	ns	
t _{PZL}					24	41		24	41		
t _{PLH}	0 thru 7	E0	Out-of-Phase output		11	18		11	18	ns	
t _{PHL}					26	40		26	40		
t _{PLH}	0 thru 7	GS	In-Phase output		38	55		38	55	ns	
t _{PHL}					9.0	21		9.0	21		
t _{PLH}	EI	GS	In-Phase output		11	17		11	17	ns	
t _{PHL}					14	36		14	36		
t _{PLH}	EI	EO	In-Phase output		17	21		17	21	ns	
t _{PHL}					25	40		30	45		
t _{PHZ}	EI	A0, A1 or A2			18	27		18	27	ns	C _L = 5.0 pF R _L = 667 Ω
t _{PLZ}					23	35		23	35		

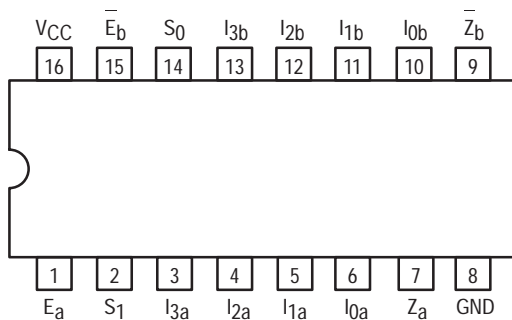


DUAL 4-INPUT MULTIPLEXER

The SN54/74LS352 is a very high-speed Dual 4-input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The SN54/74LS352 is the functional equivalent of the SN54/74LS153 except with inverted outputs.

- Inverted Version of the SN54/74LS153
- Separate Enables for Each Multiplexer
- Input Clamp Diode Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0, S_1	Common Select Inputs
E	Enable (Active LOW) Input
I_0-I_1	Multiplexer Inputs
Z	Multiplexer Outputs (note b)

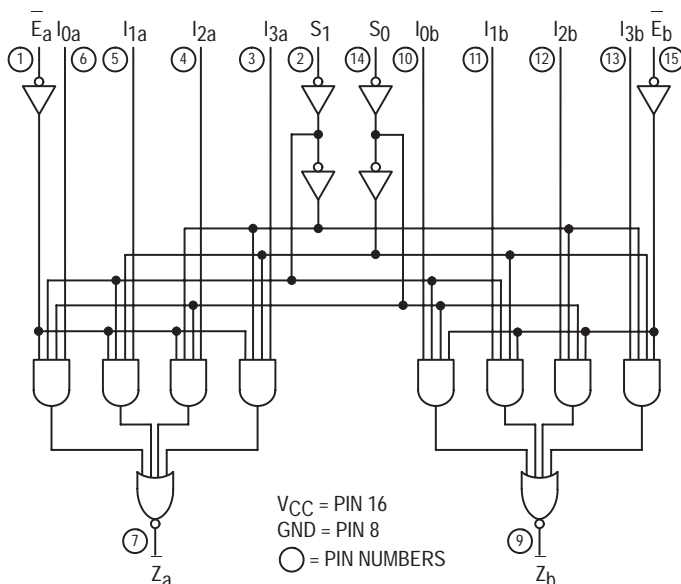
LOADING (Note a)

	HIGH	LOW
S_0, S_1	0.5 U.L.	0.25 U.L.
E	0.5 U.L.	0.25 U.L.
I_0-I_1	0.5 U.L.	0.25 U.L.
Z	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

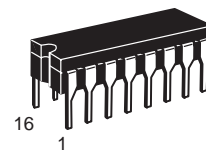
LOGIC DIAGRAM



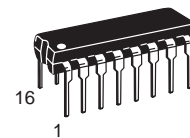
SN54/74LS352

DUAL 4-INPUT MULTIPLEXER

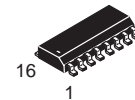
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

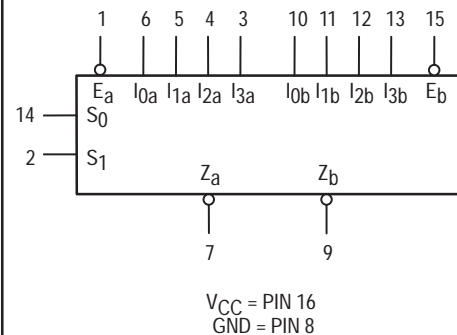


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS352

FUNCTIONAL DESCRIPTION

The SN54/74LS352 is a Dual 4-Input Multiplexer. It selects two bits of data from up to four sources under the control of the common Select Inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (E_a, E_b) which

can be used to strobe the outputs independently. When the Enables (E_a, E_b) are HIGH, the corresponding outputs (Z_a, Z_b) are forced HIGH.

The logic equations for the outputs are shown below.

$$\overline{Z}_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The SN54/74LS352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select Inputs. A less obvious application is a function gen-

erator. The SN54/74LS352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	E	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS352

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5	V	
V_{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74	0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current			10	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		19 25	29 38	ns	Figure 1 or 2
t_{PLH} t_{PHL}	Propagation Delay, Enable to Output		16 21	24 32	ns	Figure 2
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		13 17	20 26	ns	Figure 1

$V_{CC} = 5.0 \text{ V}$,
 $C_L = 15 \text{ pF}$

AC WAVEFORMS

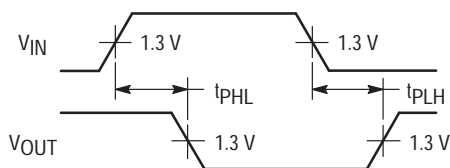


Figure 1

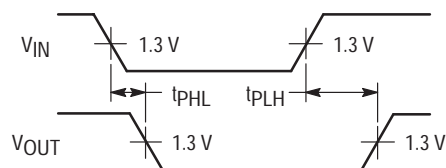


Figure 2

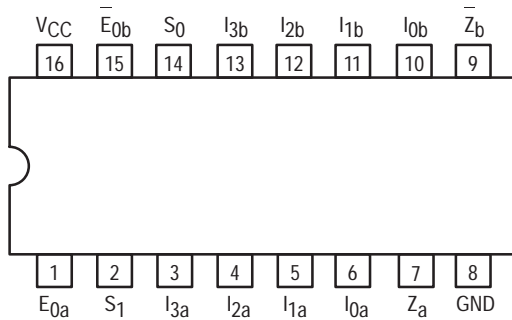


DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS353 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

- Inverted Version of the SN54/74LS253
- Schottky Process for High Speed
- Multifunction Capability
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0, S_1 Common Select Inputs

Multiplexer A
 E_{0a} Output Enable (Active LOW) Input
 $I_{0a}-I_{3a}$ Multiplexer Inputs
 Z_a Multiplexer Output (Note b)

Multiplexer B
 E_{0b} Output Enable (Active LOW) Input
 $I_{0b}-I_{3b}$ Multiplexer Inputs
 Z_b Multiplexer Output (Note b)

LOADING (Note a)

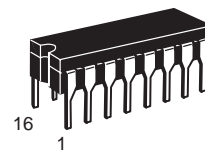
	HIGH	LOW
S_0, S_1	0.5 U.L.	0.25 U.L.
E_{0a}	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{3a}$	0.5 U.L.	0.25 U.L.
Z_a	65 (25) U.L.	15 (7.5) U.L.
E_{0b}	0.5 U.L.	0.25 U.L.
$I_{0b}-I_{3b}$	0.5 U.L.	0.25 U.L.
Z_b	65 (25) U.L.	15 (7.5) U.L.

- NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

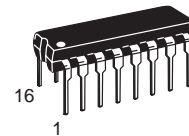
SN54/74LS353

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

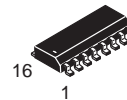
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

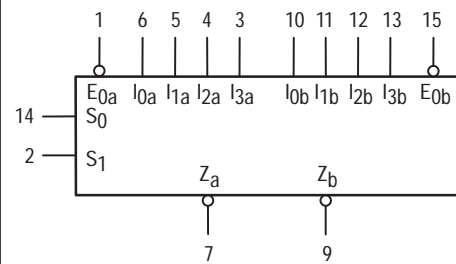


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

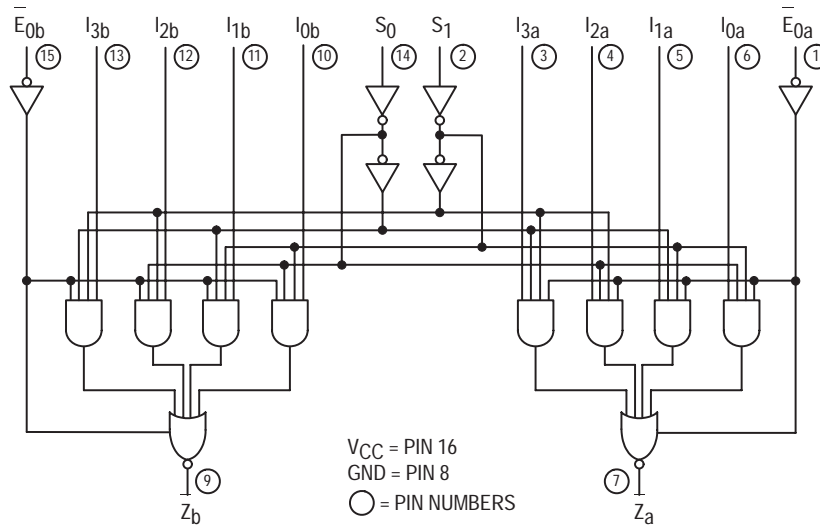
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS353

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS353 contains two identical 4-input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable (E_{0a} , E_{0b})

inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The logic equations for the outputs are shown below:

$$\bar{Z}_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\bar{Z}_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers

should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	\bar{E}_0	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Level

L = LOW Level

X = Immaterial

(Z) = High Impedance (off)

Address inputs S_0 and S_1 are common to both sections.

SN54/74LS353

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.4	3.1		V	
V _{OL}	Output LOW Voltage Q _A –Q _H	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-130	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output 3-State				14	mA	V _{CC} = MAX
	Total, Output LOW				12		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			11 13	25 20	ns	Figure 1	C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Select to Output			20 21	45 32			
t _{PZH}	Output Enable Time to HIGH Level			11	23	ns	Figures 4, 5	
t _{PZL}	Output Enable Time to LOW Level			15	23	ns	Figures 3, 5	
t _{PLZ}	Output Disable Time to LOW Level			12	27	ns	Figures 3, 5	C _L = 5.0 pF
t _{PHZ}	Output Disable Time to HIGH Level			27	41			

SN54/74LS353

3-STATE WAVEFORMS

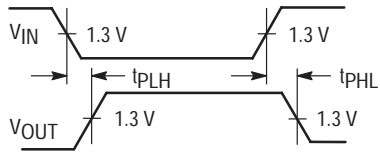


Figure 1

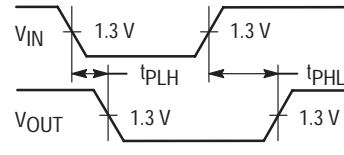


Figure 2

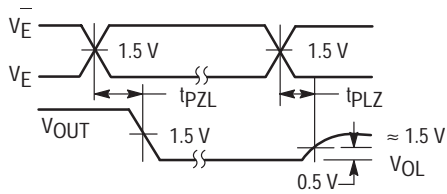


Figure 3

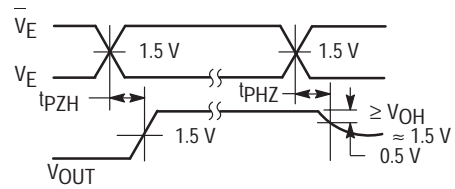
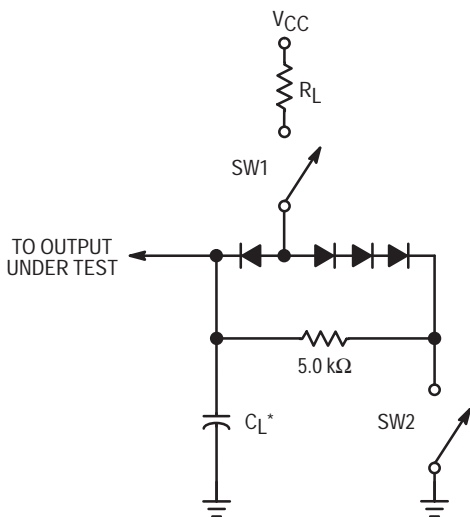


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5



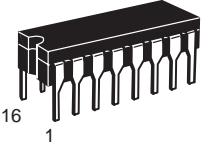
3-STATE HEX BUFFERS

These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

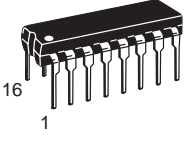
When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

SN54/74LS365A
SN54/74LS366A
SN54/74LS367A
SN54/74LS368A

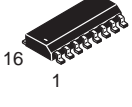
3-STATE HEX BUFFERS
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08



D SUFFIX
 SOIC
 CASE 751B-03

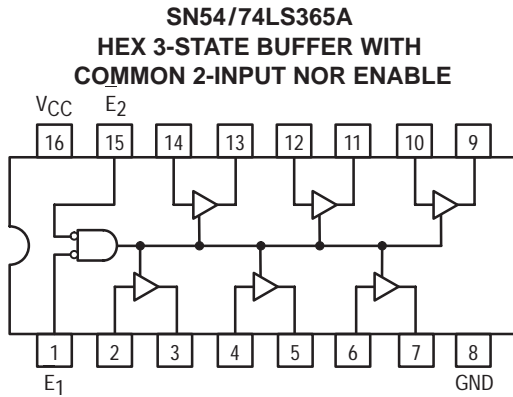
ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

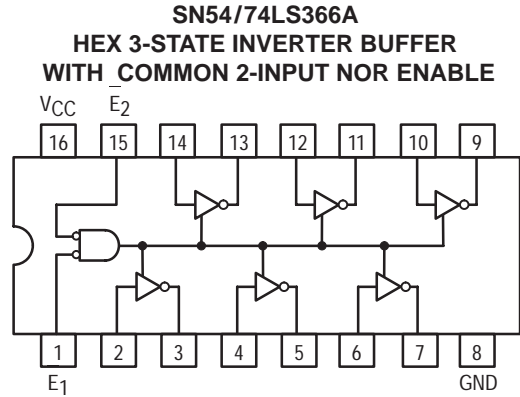
Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-1.0	mA
74				-2.6		
I _{OL}	Output Current — Low	54			12	mA
		74			24	

**SN54/74LS365A • SN54/74LS366A
SN54/74LS367A • SN54/74LS368A**



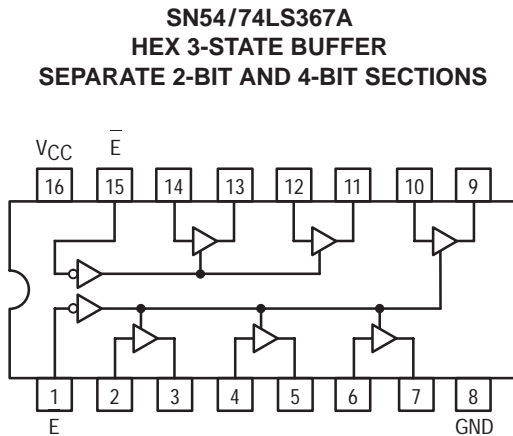
TRUTH TABLE

INPUTS			OUTPUT
\bar{E}_1	\bar{E}_2	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)



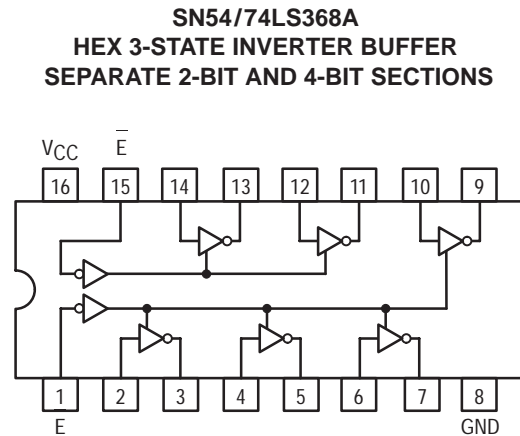
TRUTH TABLE

INPUTS			OUTPUT
\bar{E}_1	\bar{E}_2	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)



TRUTH TABLE

INPUTS		OUTPUT
\bar{E}	D	
L	L	L
L	H	H
H	X	(Z)



TRUTH TABLE

INPUTS		OUTPUT
\bar{E}	D	
L	L	H
L	H	L
H	X	(Z)

SN54/74LS365A • SN54/74LS366A SN54/74LS367A • SN54/74LS368A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current E Inputs			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
	D Inputs			-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V Either E Input at 2.0 V	
				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V Both E Inputs at 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-40		-225	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current LS365A, 367A			24	mA	V _{CC} = MAX	
	LS366A, 368A			21			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS365A/LS367A			LS366A/LS368A				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay		10 9.0	16 22		7.0 12	15 18	ns	C _L = 45 pF, R _L = 667 Ω
t _{PZH} t _{PZL}	Output Enable Time		19 24	35 40		18 28	35 45		
t _{PHZ} t _{PLZ}	Output Disable Time			30 35			32 35	ns	C _L = 5.0 pF



OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

D ₀ -D ₇	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH going edge) Input
OE	Output Enable (Active LOW) Input
O ₀ -O ₇	Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
D ₀ -D ₇	0.5 U.L.	0.25 U.L.
LE	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
OE	0.5 U.L.	0.25 U.L.
O ₀ -O ₇	65 (25) U.L.	15 (7.5) U.L.

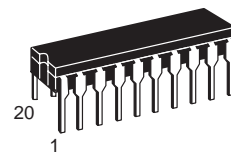
NOTES:

- a) 1 TTL Units Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

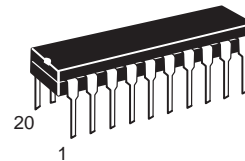
SN54/74LS373
SN54/74LS374

**OCTAL TRANSPARENT LATCH
WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT**

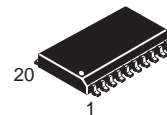
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



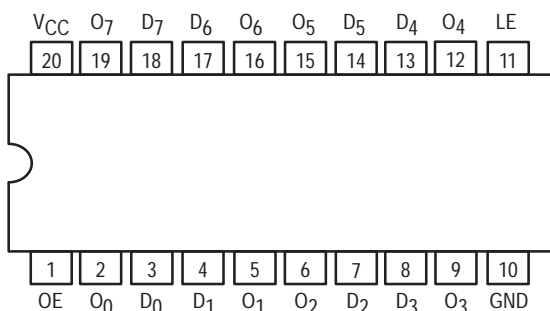
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

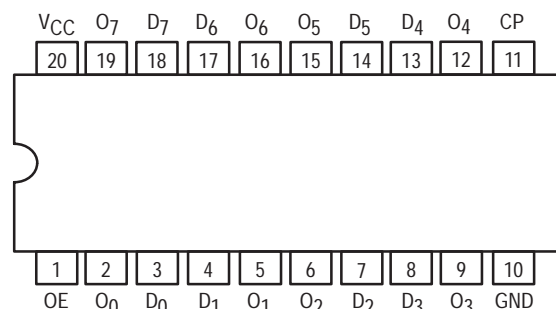
SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS373



SN54/74LS374



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS373 • SN54/74LS374

TRUTH TABLE

D _n	LE	OE	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z*

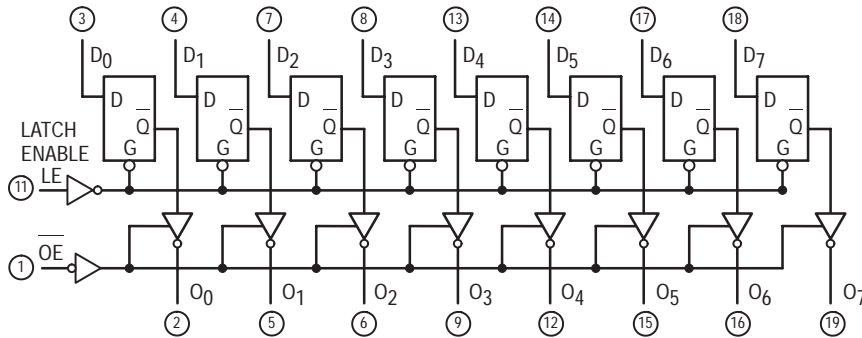
D _n	LE	OE	O _n
H		L	H
L		L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

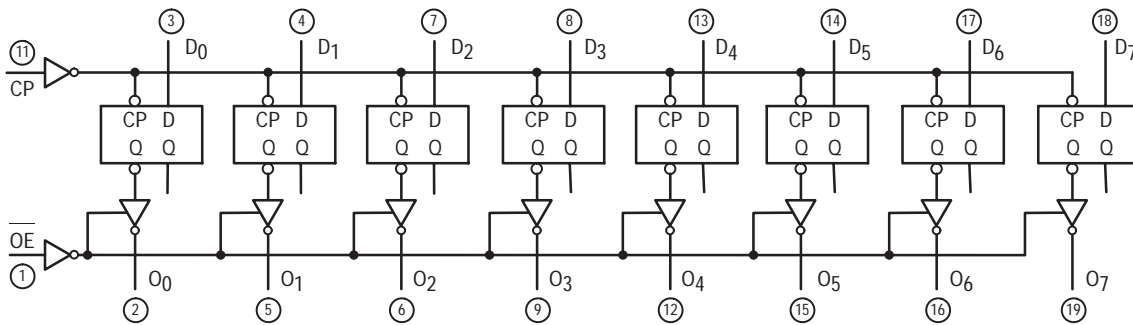
LOGIC DIAGRAMS

SN54LS/74LS373



V_{CC} = PIN 20
GND = PIN 10
○ = PIN NUMBERS

SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS373 • SN54/74LS374

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			40	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency				35	50		MHz	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t _{PLH} t _{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t _{PZH} t _{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t _W	Clock Pulse Width	15		15		ns
t _S	Setup Time	5.0		20		ns
t _H	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

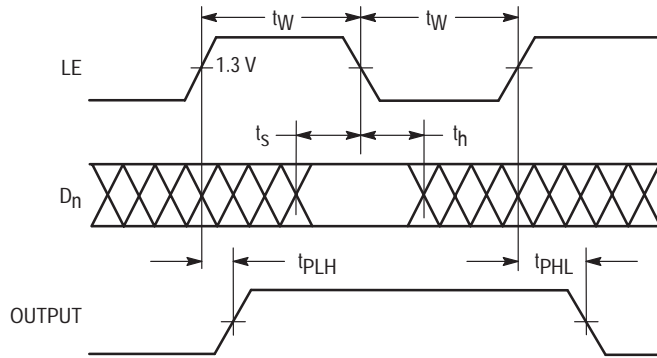


Figure 1

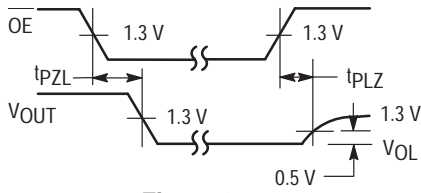


Figure 2

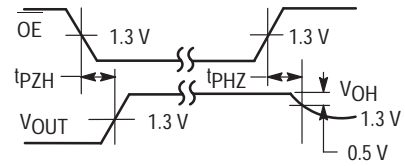
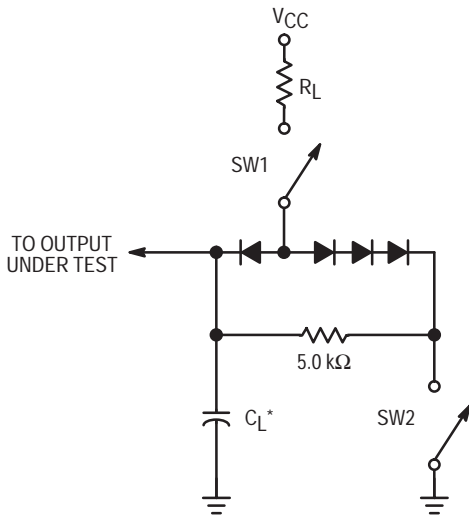


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pLZ}	Closed	Closed
t_{pHZ}	Closed	Closed

SN54/74LS374

AC WAVEFORMS

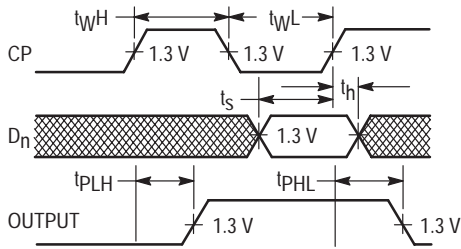


Figure 5

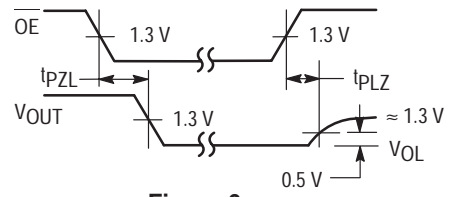


Figure 6

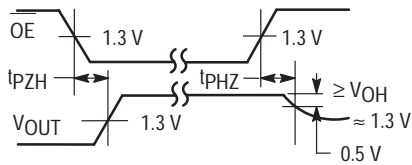
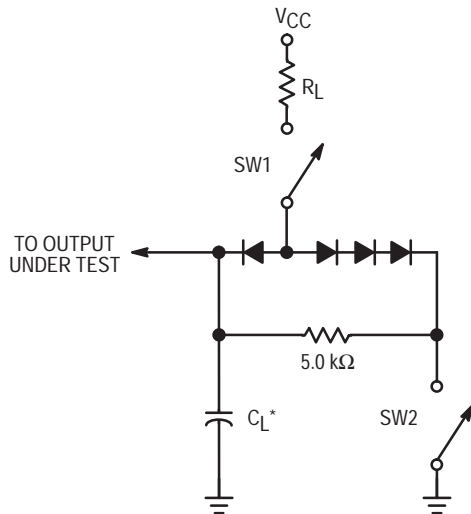


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 8

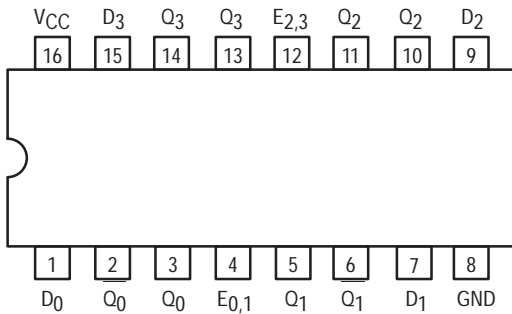
SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

4-BIT D LATCH

The SN54/74LS375 is a 4-Bit D-Type Latch for use as temporary storage for binary information between processing limits and input/output or indicator units. When the Enable (E) is HIGH, information present at the D input will be transferred to the Q output and, if E is HIGH, the Q output will follow the input. When E goes LOW, the information present at the D input prior to its setup time will be retained at the Q outputs.

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE (Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
 t_n = bit time before enable negative-going transition.
 t_{n+1} = bit time after enable negative-going transition.

PIN NAMES

D_1-D_4	Data Inputs
E_{0-1}	Enable Input Latches 0, 1
E_{2-3}	Enable Input Latches 2, 3
Q_1-Q_4	Latch Outputs (Note b)
Q_1-Q_4	Complimentary Latch Outputs (Note b)

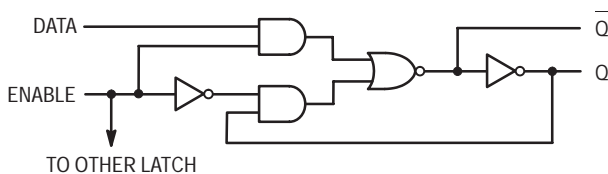
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
2.0 U.L.	1.0 U.L.
2.0 U.L.	1.0 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

NOTES:

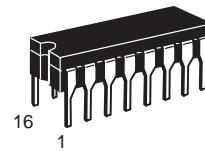
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 25 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM

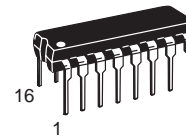


SN54/74LS375

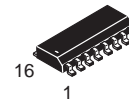
4-BIT D LATCH LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

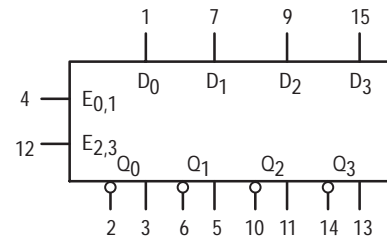


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS375

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	D Input E Input			20 80	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		D Input E Input			0.1 0.4	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	D Input E Input			-0.4 -1.6	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				12	mA	V _{CC} = MAX

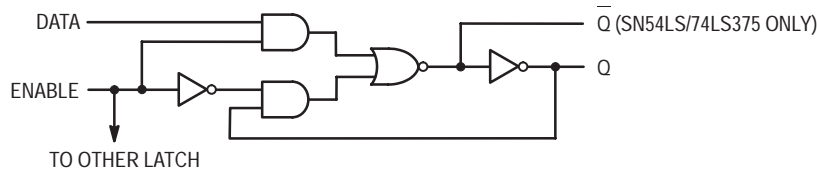
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Data to Q			15 9.0	27 17	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Data to \bar{Q}			12 7.0	20 15	ns	
t _{PLH} t _{PHL}	Propagation Delay, Enable to Q			15 14	27 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, Enable to \bar{Q}			16 7.0	30 15	ns	

SN54/74LS375

LOGIC DIAGRAM



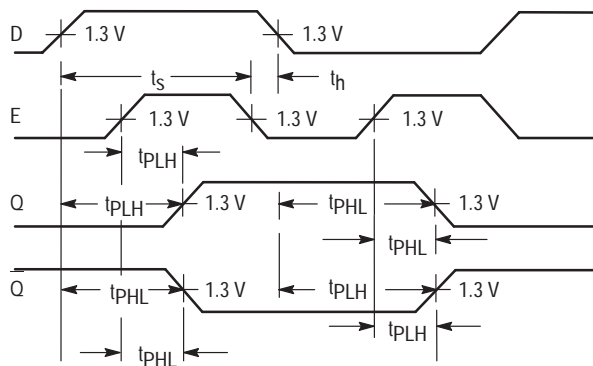
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Enable Pulse Width	20			ns	V _{CC} = 5.0 V
t _s	Setup Time	20			ns	
t _h	Hold Time	0			ns	

AC WAVEFORMS



DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.



OCTAL D FLIP-FLOP WITH ENABLE; HEX D FLIP-FLOP WITH ENABLE; 4-BIT D FLIP-FLOP WITH ENABLE

The SN54/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

The SN54/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the SN54/74LS174, but with common Enable rather than common Master Reset.

The SN54/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the SN54/74LS175 but features the common Enable rather than common Master Reset.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

\bar{E}	Enable (Active LOW) Input
D_0-D_3	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
Q_0-Q_3	True Outputs (Note b)
$\bar{Q}_0-\bar{Q}_3$	Complemented Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
\bar{E}	0.5 U.L.	0.25 U.L.
D_0-D_3	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
Q_0-Q_3	10 U.L.	5 (2.5) U.L.
$\bar{Q}_0-\bar{Q}_3$	10 U.L.	5 (2.5) U.L.

NOTES:

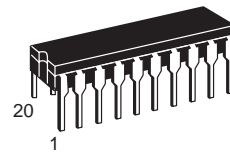
a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

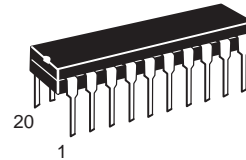
SN54/74LS377
SN54/74LS378
SN54/74LS379

**OCTAL D FLIP-FLOP WITH
ENABLE; HEX D FLIP-FLOP
WITH ENABLE; 4-BIT D FLIP-FLOP
WITH ENABLE**

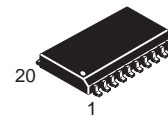
LOW POWER SCHOTTKY



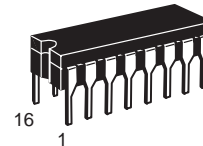
J SUFFIX
CERAMIC
CASE 732-03



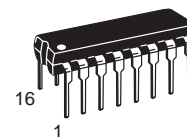
N SUFFIX
PLASTIC
CASE 738-03



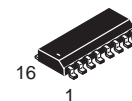
DW SUFFIX
SOIC
CASE 751D-03



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

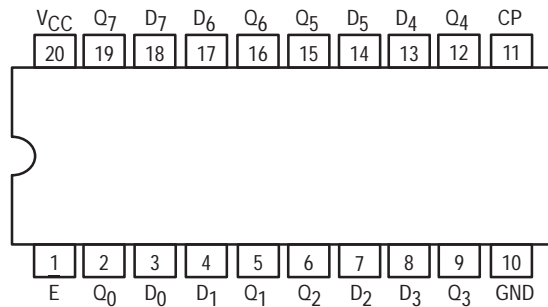
ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC
SN74LSXXXD	SOIC

SN54/74LS377 • SN54/74LS378 • SN54/74LS379

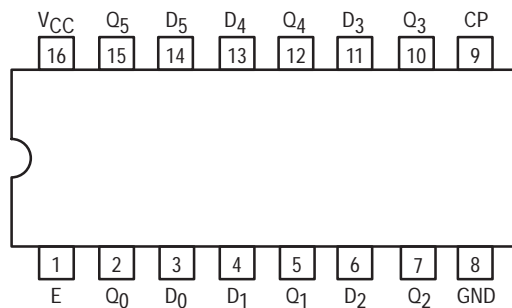
CONNECTION DIAGRAM DIPS (TOP VIEW)

SN54/74LS377



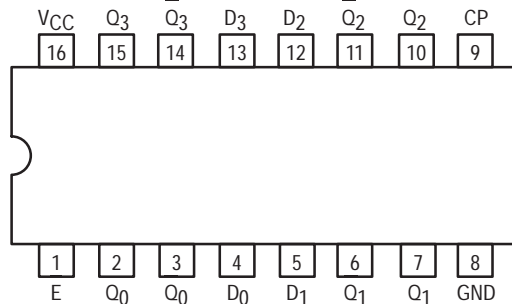
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS378



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS379

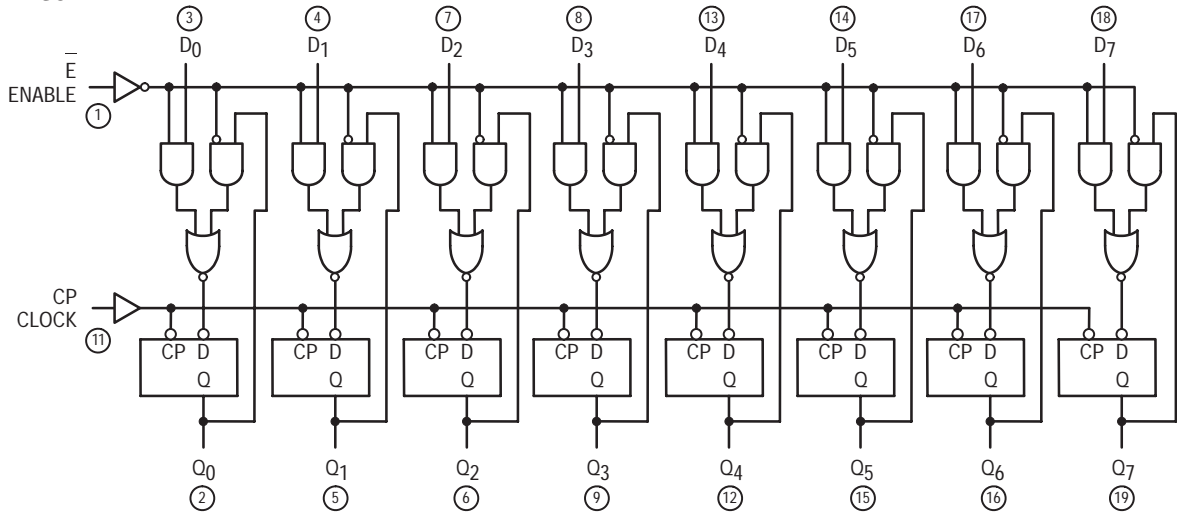


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

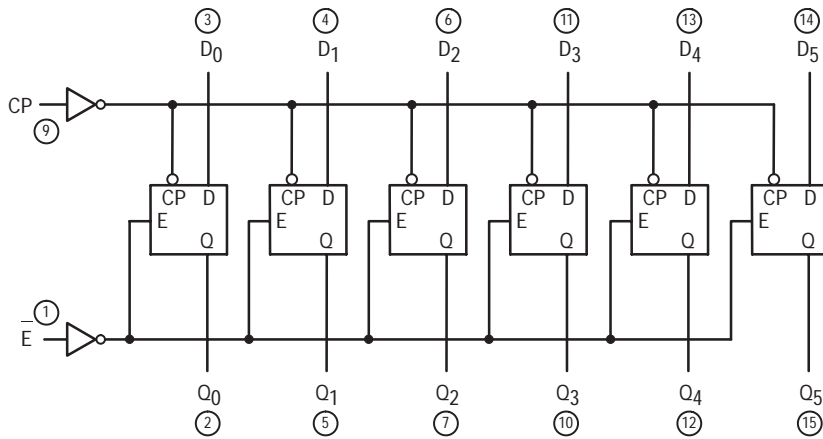
SN54/74LS377 • SN54/74LS378 • SN54/74LS379

LOGIC DIAGRAMS

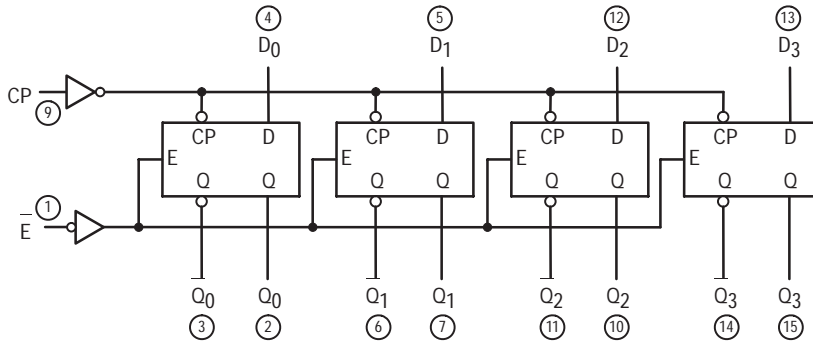
SN54/74LS377



SN54/74LS378



SN54/74LS379



SN54/74LS377 • SN54/74LS378 • SN54/74LS379

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			-0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current	LS377		28	mA	$V_{CC} = \text{MAX}$, NOTE 1	
		LS378		22			
		LS379		15			

NOTE: With all inputs open and GND applied to all data and enable inputs, I_{CC} is measured after a momentary GND, then 4.5 V is applied to clock.

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	30	40		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH}	Propagation Delay, Clock to Output		17	27	ns	
t_{PHL}			18	27		

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Any Pulse Width	20			ns	$V_{CC} = 5.0 \text{ V}$
t_S	Data Setup Time	20			ns	
t_s	Enable Setup Time	Inactive — State	10		ns	
		Active — State	25		ns	
t_h	Any Hold Time	5.0			ns	

DEFINITION OF TERMS




SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

SN54/74LS377 • SN54/74LS378 • SN54/74LS379

TRUTH TABLE

E	CP	D _n	Q _n	Q̄ _n
H		X	No Change	No Change
L		H	H	L
L		L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

AC WAVEFORMS

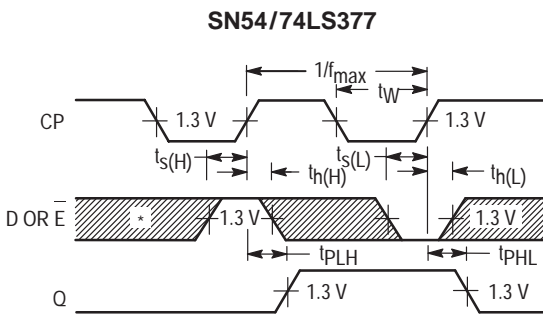


Figure 1. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock

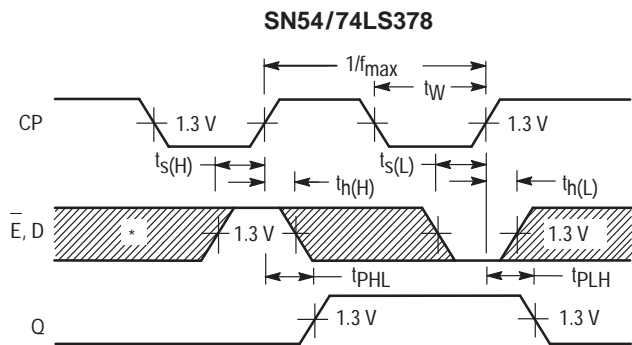
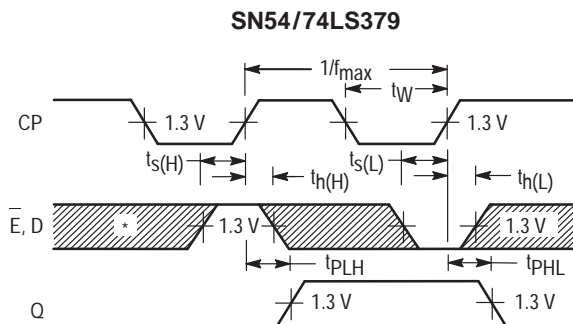


Figure 2. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock

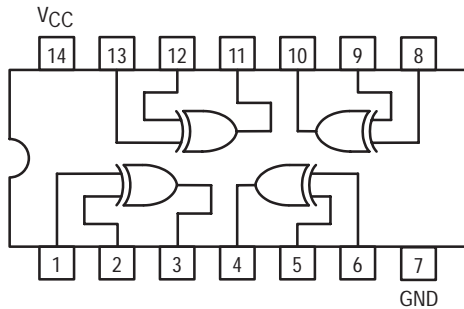


*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data, Enable to Clock

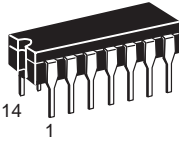


QUAD 2-INPUT EXCLUSIVE-OR GATE

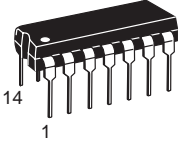


SN54/74LS386

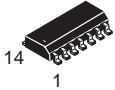
**QUAD 2-INPUT EXCLUSIVE-OR GATE
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS386

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			10	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Other Input LOW		12 10	23 17	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Other Input HIGH		20 13	30 22	ns	



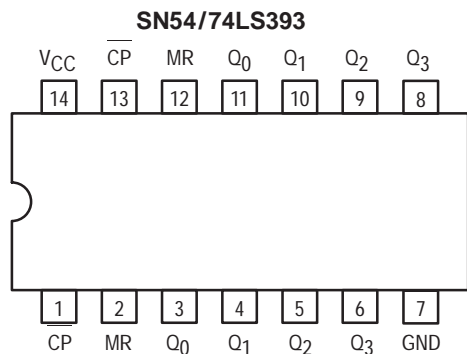
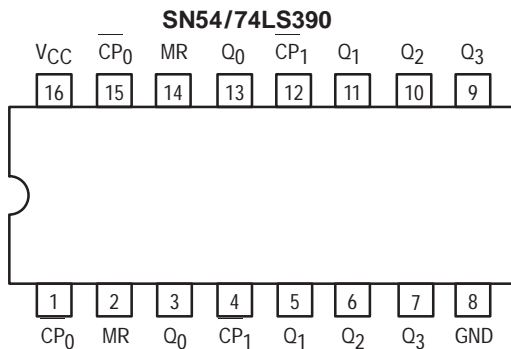
DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by-five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing $\div 2$, $\div 2.5$, $\div 5$
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

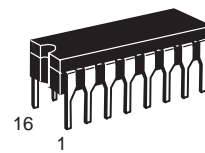
CONNECTION DIAGRAM DIP (TOP VIEW)



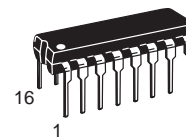
NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

**SN54/74LS390
SN54/74LS393**

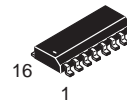
**DUAL DECADE COUNTER;
DUAL 4-STAGE
BINARY COUNTER
LOW POWER SCHOTTKY**



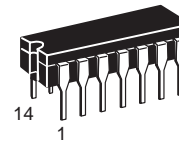
**J SUFFIX
CERAMIC
CASE 620-09**



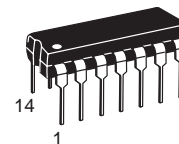
**N SUFFIX
PLASTIC
CASE 648-08**



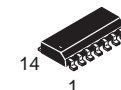
**D SUFFIX
SOIC
CASE 751B-03**



**J SUFFIX
CERAMIC
CASE 632-08**



**N SUFFIX
PLASTIC
CASE 646-06**



**D SUFFIX
SOIC
CASE 751A-02**

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

SN54/74LS390 • SN54/74LS393

PIN NAMES

$\overline{\text{CP}}$	Clock (Active LOW going edge) Input to +16 (LS393)
$\overline{\text{CP}}_0$	Clock (Active LOW going edge) Input to +2 (LS390)
$\overline{\text{CP}}_1$	Clock (Active LOW going edge) Input to +5 (LS390)
MR	Master Reset (Active HIGH) Input
Q_0 – Q_3	Flip-Flop outputs (Note b)

LOADING (Note a)

	HIGH	LOW
$\overline{\text{CP}}$	0.5 U.L.	1.0 U.L.
$\overline{\text{CP}}_0$	0.5 U.L.	1.0 U.L.
$\overline{\text{CP}}_1$	0.5 U.L.	1.5 U.L.
MR	0.5 U.L.	0.25 U.L.
Q_0 – Q_3	10 U.L.	5 (2.5) U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

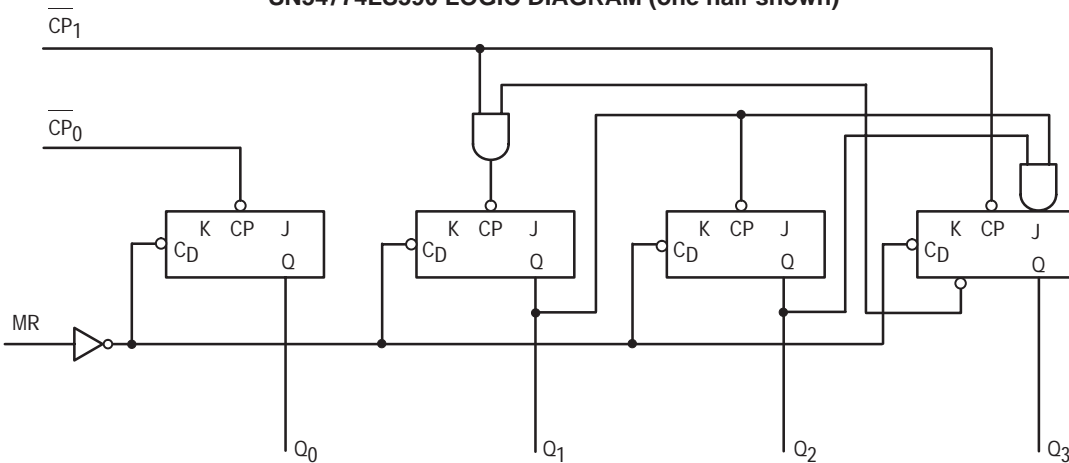
FUNCTIONAL DESCRIPTION

Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the $\div 16$ Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

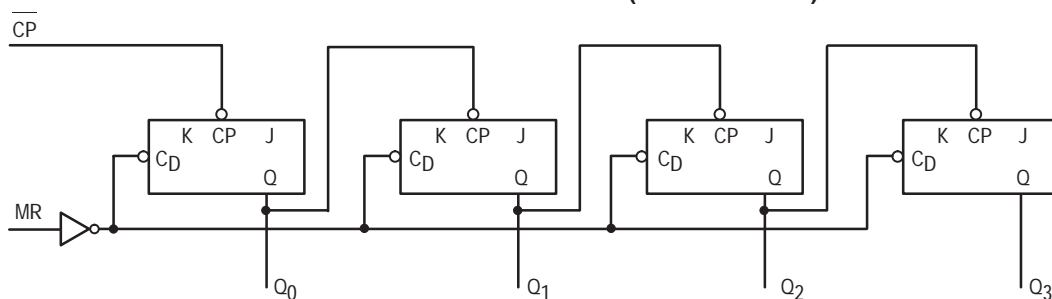
Each half of the LS390 contains a $\div 5$ section that is independent except for the common MR function. The $\div 5$

section operates in 4.2.1 binary sequence, as shown in the $\div 5$ Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a $\div 10$ function having a 50% duty cycle output, connect the input signal to $\overline{\text{CP}}_1$ and connect the Q_3 output to the $\overline{\text{CP}}_0$ input; the Q_0 output provides the desired 50% duty cycle output. If the input frequency is connected to $\overline{\text{CP}}_0$ and the Q_0 output is connected to $\overline{\text{CP}}_1$, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54/74LS390 LOGIC DIAGRAM (one half shown)



SN54/74LS393 LOGIC DIAGRAM (one half shown)



SN54/74LS390 • SN54/74LS393

**SN54/74LS390 BCD
TRUTH TABLE**
(Input on CP₀; Q₀ CP₁)

COUNT	OUTPUTS			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**SN54/74LS390 ÷5
TRUTH TABLE**
(Input on CP₁)

COUNT	OUTPUTS		
	Q ₃	Q ₂	Q ₁
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L

**SN54/74LS390 ÷10 (50% @ Q₀)
TRUTH TABLE**
(Input on CP₁, Q₃ to CP₀)

COUNT	OUTPUTS			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	H	L
2	L	H	L	L
3	L	H	H	L
4	H	L	L	L
5	L	L	L	H
6	L	L	H	H
7	L	H	L	H
8	L	H	H	H
9	H	L	L	H

**SN54/74LS393
TRUTH TABLE**

COUNT	OUTPUTS			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS390 • SN54/74LS393

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	MR			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		CP, CP ₀			-1.6	mA	
		CP ₁			-2.4	mA	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				26	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency CP ₀ to Q ₀		25	35		MHz	C _L = 15 pF
f _{MAX}	Maximum Clock Frequency CP ₁ to Q ₁		20			MHz	
t _{PLH} t _{PHL}	Propagation Delay, CP to Q ₀	LS393		12 13	20 20	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}_0$ to Q ₀	LS390		12 13	20 20	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}$ to Q ₃	LS393		40 40	60 60	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}_0$ to Q ₂	LS390		37 39	60 60	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}_1$ to Q ₁	LS390		13 14	21 21	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}_1$ to Q ₂	LS390		24 26	39 39	ns	
t _{PLH} t _{PHL}	$\overline{\text{CP}}_1$ to Q ₃	LS390		13 14	21 21	ns	
t _{PHL}	MR to Any Output	LS390/393		24	39	ns	

SN54/74LS390 • SN54/74LS393

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width LS393	20			ns	$V_{CC} = 5.0\text{ V}$
t_W	CP_0 Pulse Width LS390	20			ns	
t_W	CP_1 Pulse Width LS390	40			ns	
t_W	MR Pulse Width LS390/393	20			ns	
t_{rec}	Recovery Time LS390/393	25			ns	

AC WAVEFORMS

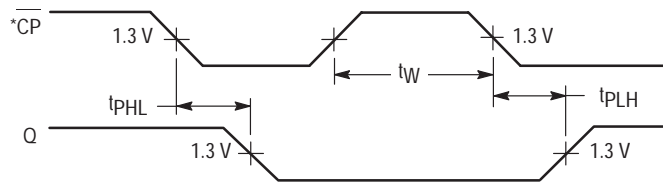


Figure 1

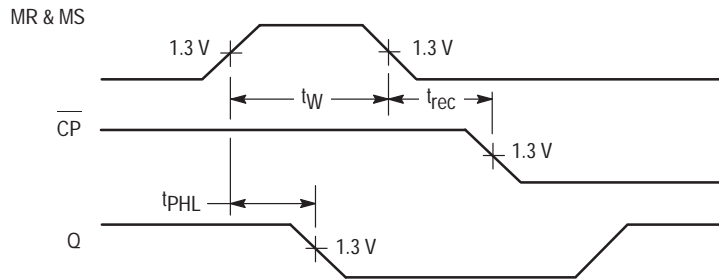


Figure 2

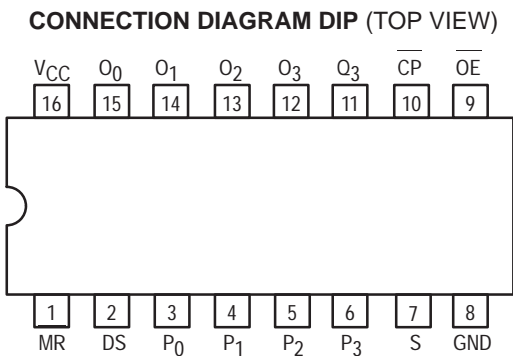
*The number of Clock Pulses required between t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.



4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

The SN74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active HIGH Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- Shift Left or Parallel 4-Bit Register
- 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects



PIN NAMES

P ₀ –P ₃	Parallel Inputs
D _S	Serial Data Input
S	Mode Select Input
CP	Clock (Active LOW) Input
MR	Master Reset (Active LOW) Input
OE	Output Enable (Active HIGH) Input
O ₀ –O ₃	3-State Register Outputs
Q ₃	Register Output

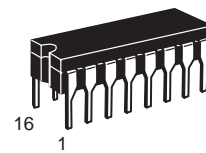
NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

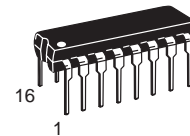
LOADING (Note a)	
HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.
10 U.L.	5 U.L.

SN74LS395

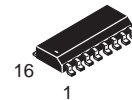
4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

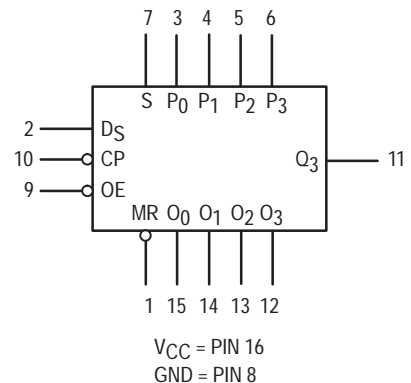


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

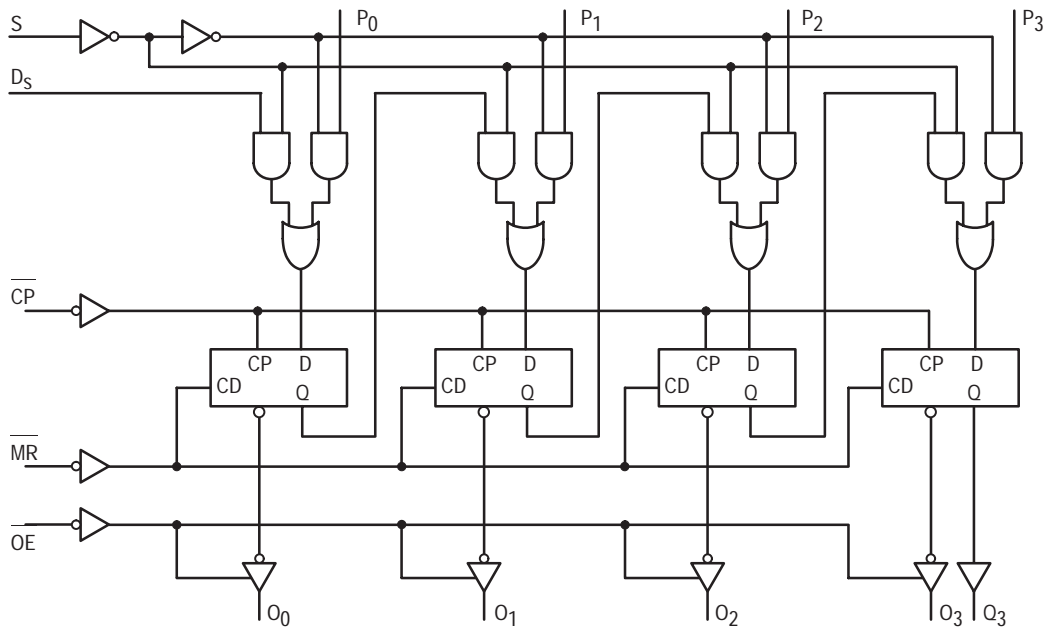
SN74LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN74LS395

LOGIC DIAGRAM



FUNCTION DESCRIPTION

The SN74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_n , D_s and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the

S input is LOW, a CP HIGH-LOW transition transfers data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 . A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2 , O_2 to P_1 and O_1 to P_0 , with P_3 acting as the linking input from another package.

When the OE input is HIGH, the output buffers are disabled and the Q_0 – Q_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	MR	CP	S	D_s	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H		L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H		L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H		H	X	P_n	P_0	P_1	P_2	P_3

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

t_n, t_{n+1} = time before and after CP HIGH-to-LOW transition

NOTE:—

When OE is HIGH, outputs O_0 – O_3 are in the high impedance state; however, this does not affect other operations or the Q_3 output.

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			–0.4	mA
I_{OL}	Output Current — Low			8.0	mA

SN74LS395

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.7	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
V _{OL}	Output LOW Voltage		0.25	0.4	V	I _{OL} = 4.0 mA
			0.35	0.5	V	I _{OL} = 8.0 mA
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _O = 2.4 V
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _O = 0.4 V
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				-0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH			31	mA	V _{CC} = MAX, \overline{OE} = GND, \overline{CP} = GND
	Total, Output LOW			34	mA	V _{CC} = MAX, OE = 4.5 V, CP momentary 3.0 V then GND

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Input Clock Frequency	30	45		MHz	V _{CC} = 5.0 V C _L = 15 pF
t _{PHL}	Propagation Delay, Clear to Output		22	35	ns	
t _{PLH}	Propagation Delay, Low to High		15	30	ns	
t _{PHL}	Propagation Delay, High to Low		25	30	ns	
t _{PZH}	Output Enable Time		15	25	ns	C _L = 5.0 pF
		t _{PZL}	17	25		
t _{PLZ}	Output Disable Time		12	20	ns	
		t _{PHZ}	11	17		

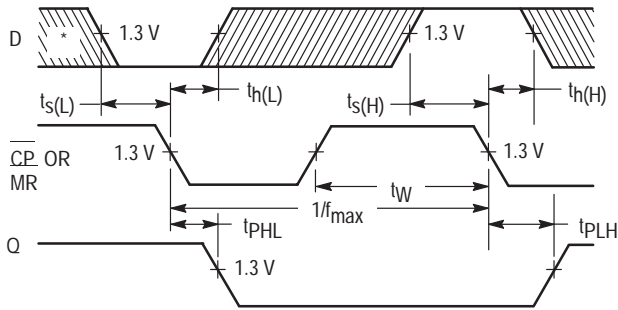
AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width	16			ns	V _{CC} = 5.0 V
t _s	Setup Time, Mode Select	40			ns	
t _s	Setup Time, All Others	20			ns	
t _h	Data Hold Time	10			ns	

SN74LS395

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for $S = \text{LOW}$ and P_n for $S = \text{HIGH}$.

Figure 1

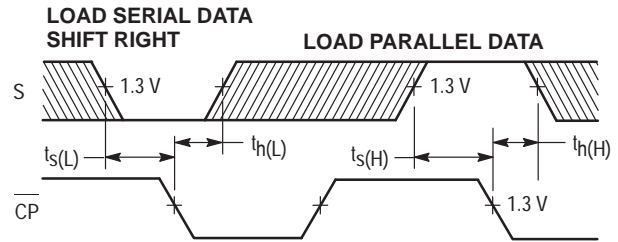


Figure 2

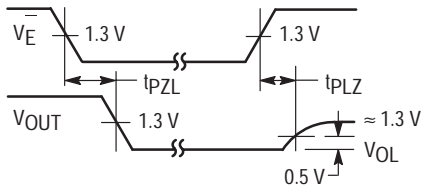


Figure 3

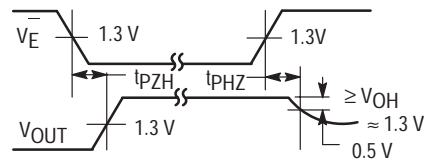
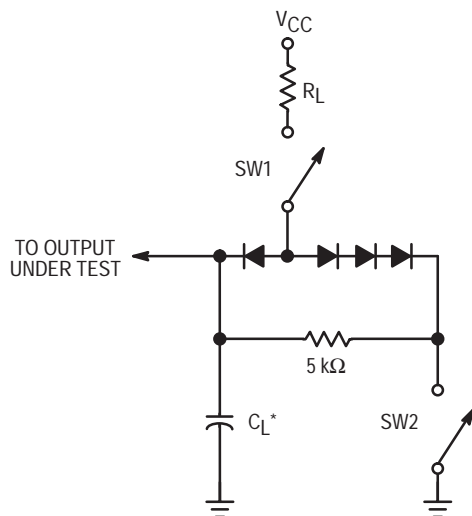


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

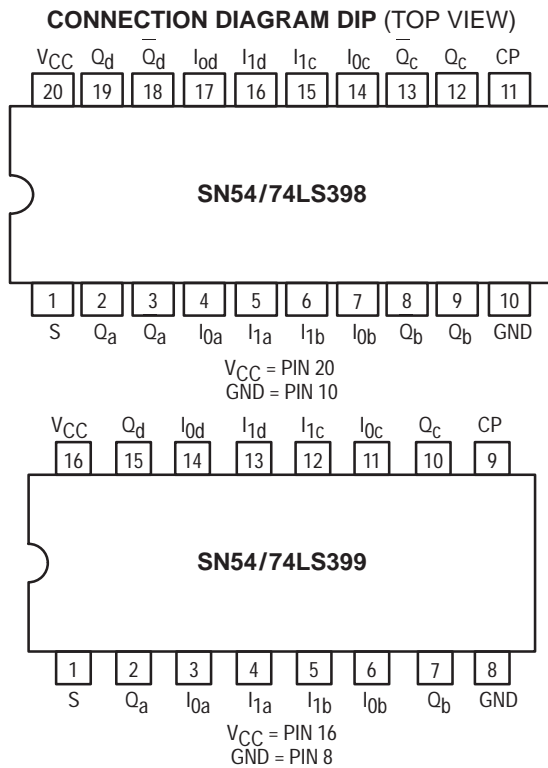
SYMBOL	SW1	SW2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pLZ}	Closed	Closed
t_{pHZ}	Closed	Closed



QUAD 2-PORT REGISTER

The SN54/74LS398 and SN54/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The SN54/74LS398 features both Q and \bar{Q} inputs, while the SN54/74LS399 has only Q outputs.

- Select From Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complemented Outputs on SN54/74LS398
- Input Clamp Diodes Limit High-Speed Termination Effects



PIN NAMES

S	Common Select Input
CP	Clock (Active HIGH Going Edge) Input
$I_{0a}-I_{0d}$	Data Inputs From Source 0
$I_{1a}-I_{1d}$	Data Inputs From Source 1
$Q_a-\bar{Q}_d$	Register True Outputs (Note b)
$Q_a-\bar{Q}_d$	Register Complementary Outputs (Note b)

LOADING (Note a)

	HIGH	LOW
S	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{0d}$	0.5 U.L.	0.25 U.L.
$I_{1a}-I_{1d}$	0.5 U.L.	0.25 U.L.
$Q_a-\bar{Q}_d$	10 U.L.	5 (2.5) U.L.
$Q_a-\bar{Q}_d$	10 U.L.	5 (2.5) U.L.

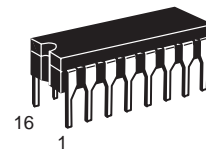
NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

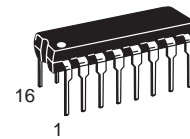
SN54/74LS398 SN54/74LS399

QUAD 2-PORT REGISTER

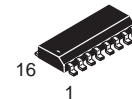
LOW POWER SCHOTTKY



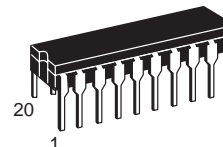
J SUFFIX
CERAMIC
CASE 620-09



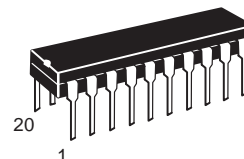
N SUFFIX
PLASTIC
CASE 648-08



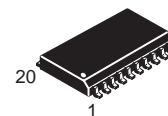
D SUFFIX
SOIC
CASE 751B-03



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



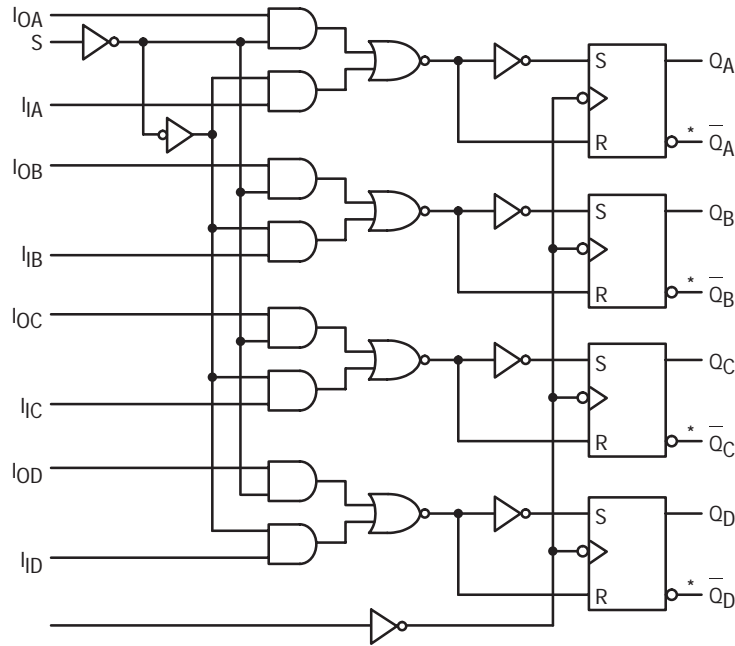
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC
SN74LSXXXD	SOIC

SN54/74LS398 • SN54/74LS399

FUNCTIONAL BLOCK DIAGRAM



* SN54/74LS398 only

FUNCTIONAL DESCRIPTION

The SN54/74LS398 and SN54/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock in-

put (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The SN54/74LS398 has both Q and \bar{Q} Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I ₀	I ₁	Q	Q*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*SN54/74LS398 only

l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

SN54/74LS398 • SN54/74LS399

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			13	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output Q		18 21	27 32	ns	V _{CC} = 5.0 V C _L = 15 pF

SN54/74LS398 • SN54/74LS399

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width	20			ns	$V_{CC} = 5.0\text{ V}$
t_S	Data Setup Time	25			ns	
t_S	Select Setup Time	45			ns	
t_H	Hold Time, Any Input	0			ns	

DEFINITIONS OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

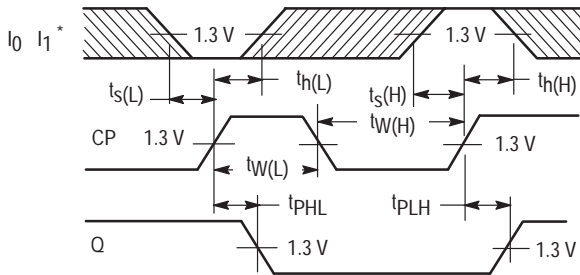


Figure 1

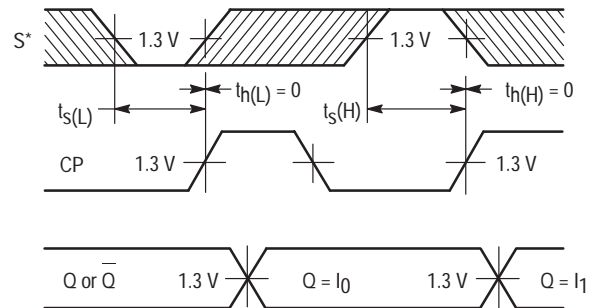


Figure 2

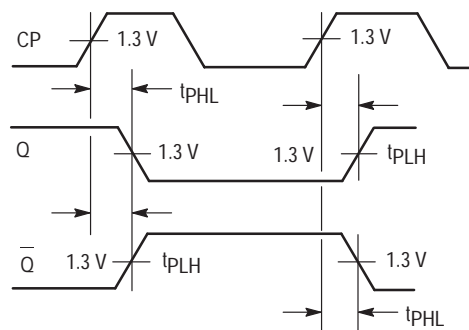


Figure 3

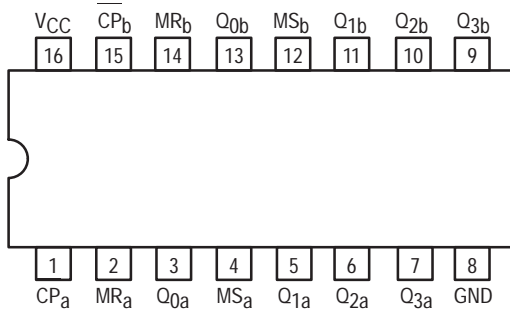
*The shaded areas indicate when the input is permitted to change for predictable output performance.

DUAL DECADE COUNTER

The SN54/74LS490 contains a pair of high-speed 4-stage ripple counters. Each half of the SN54/74LS490 has individual Clock, Master Reset and Master Set (Preset 9) inputs. Each section counts in the 8, 4, 2, 1 BCD code.

- Dual Version of SN54/74LS490
- Individual Asynchronous Clear and Preset to 9 for Each Counter
- Count Frequency — Typically 65 MHz
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

MS Master Set (Set to 9) Input
 MR Master Reset
 CP Clock Input (Active LOW Going Edge)
 Q₀–Q₃ Counter Outputs (Note b)

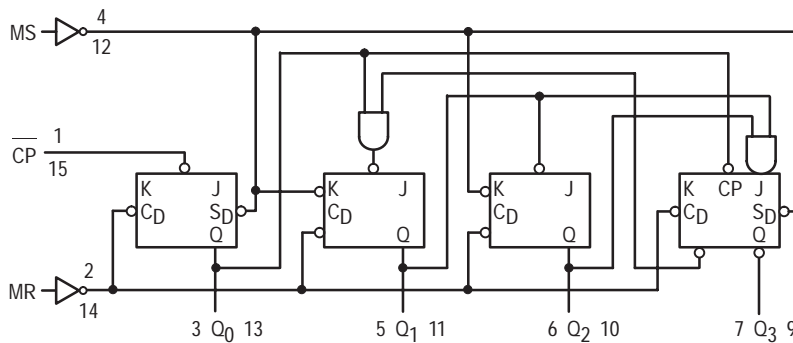
LOADING (Note a)

	HIGH	LOW
MS	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
CP	1.5 U.L.	1.5 U.L.
Q ₀ –Q ₃	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

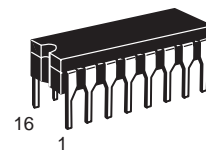
LOGIC DIAGRAM (ONE HALF SHOWN)



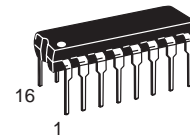
SN54/74LS490

DUAL DECADE COUNTER

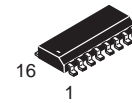
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 620-09



N SUFFIX
 PLASTIC
 CASE 648-08



D SUFFIX
 SOIC
 CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXD SOIC

TRUTH TABLE

COUNT	OUTPUTS			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

SN54/74LS490

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	MS, MR		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		Clock		-1.6			
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			26	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC SET-UP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Any Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	MR or MS to Setup Time	25			ns	

SN54/74LS490

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, $\overline{\text{CP}}$ to Q ₀		12 13	20 20	ns	Figure 1
t _{PLH} t _{PHL}	Propagation Delay, $\overline{\text{CP}}$ to Q ₁ or Q ₃		24 26	39 39	ns	Figure 3
t _{PLH} t _{PHL}	Propagation Delay, $\overline{\text{CP}}$ to Q ₂		32 36	54 54	ns	Figure 2
t _{PHL}	Propagation Delay, MR to Output		24	39	ns	Figure 2
t _{PLH} t _{PHL}	Propagation Delay, MS to Output		24 20	39 36	ns	Figure 2

V_{CC} = 5.0 V,
C_L = 15 pF

AC WAVEFORMS

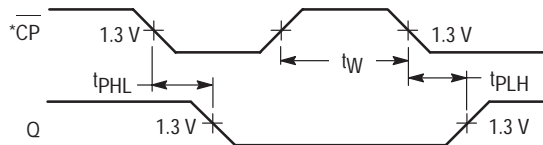


Figure 1

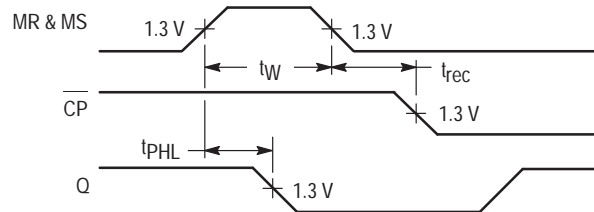


Figure 2

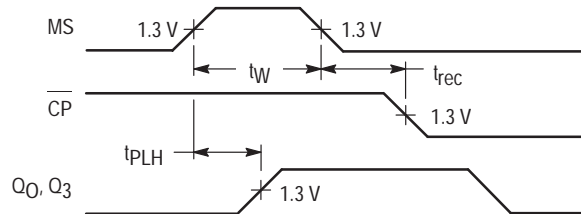


Figure 3

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.



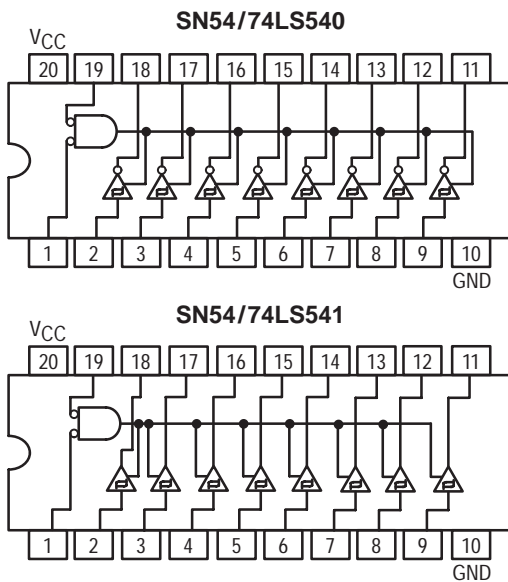
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The SN54/74LS540 and SN54/74LS541 are octal buffers and line drivers with the same functions as the LS240 and LS241, but with pinouts on the opposite side of the package.

These device types are designed to be used as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These devices are especially useful as output ports for the microprocessors, allowing ease of layout and greater PC board density.

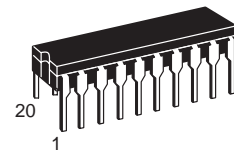
- Hysteresis at Inputs to Improve Noise Margin
- PNP Inputs Reduce Loading
- 3-State Outputs Drive Bus Lines
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Input Clamp Diodes Limit High-Speed Termination Effects

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

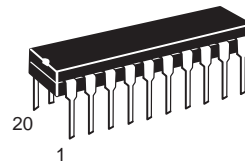


SN54/74LS540 SN54/74LS541

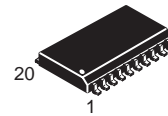
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

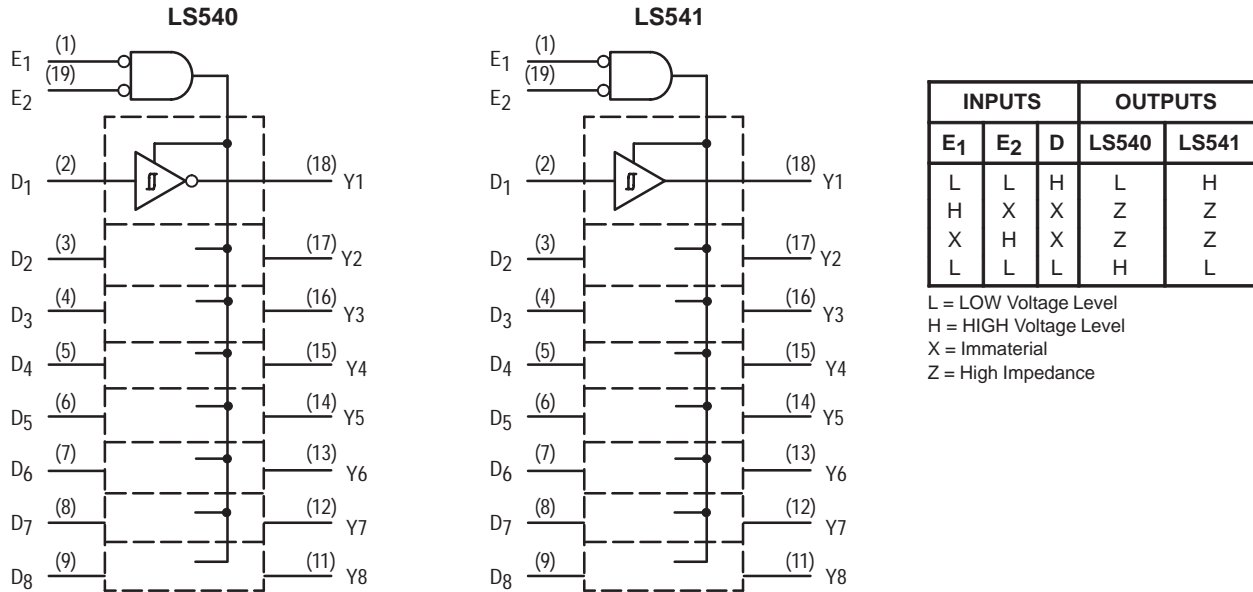
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-12 -15	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS540 • SN54/74LS541

BLOCK DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54, 74	2.4	3.4	V	$V_{CC} = \text{MIN}$, $I_{OH} = -3.0 \text{ mA}$	
		54, 74	2.0		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IL} = 0.5 \text{ V}$	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL} \text{ or } V_{IH}$ per Truth Table
		74		0.35	0.5	V	
$V_{T+} - V_{T-}$	Hysteresis	0.2	0.4		V	$V_{CC} = \text{MIN}$	
I_{OZH}	Output Off Current HIGH			20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 2.7 \text{ V}$	
I_{OZL}	Output Off Current LOW			-20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.4 \text{ V}$	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-40		-225	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current Total, Output HIGH	LS540		25	mA	$V_{CC} = \text{MAX}$	
		LS541		32	mA		
	Total, Output LOW	LS540		45	mA		
		LS541		52	mA		
	Total Output 3-State	LS540		52	mA		
		LS541		55	mA		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS540 • SN54/74LS541

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Propagation Delay, Data to Output	LS540	9.0	15	ns	$V_{CC} = 5.0\text{ V}$ $C_L = 45\text{ pF}$ $R_L = 667\ \Omega$
t_{PLH}		LS541	12	15		
t_{PHL}		LS540	12	15		
t_{PHL}		LS541	12	18		
t_{PZH}	Output Enable Time to HIGH Level	LS540	15	25	ns	$C_L = 5.0\text{ pF}$
t_{PZH}		LS541	15	32		
t_{PZL}	Output Enable Time to LOW Level	LS540	20	38	ns	
t_{PZL}		LS541	20	38		
t_{PHZ}	Output Disable Time to HIGH Level	LS540	10	18	ns	
t_{PHZ}		LS541	10	18		
t_{PLZ}	Output Disable Time to LOW Level	LS540	15	25	ns	
t_{PLZ}		LS541	15	29		

AC WAVEFORMS

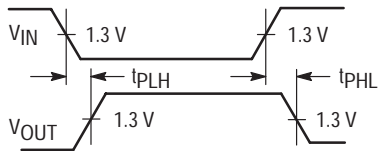


Figure 1

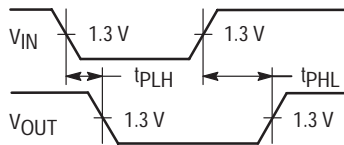


Figure 2

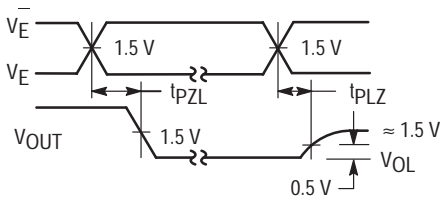


Figure 3

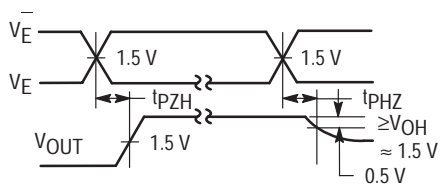
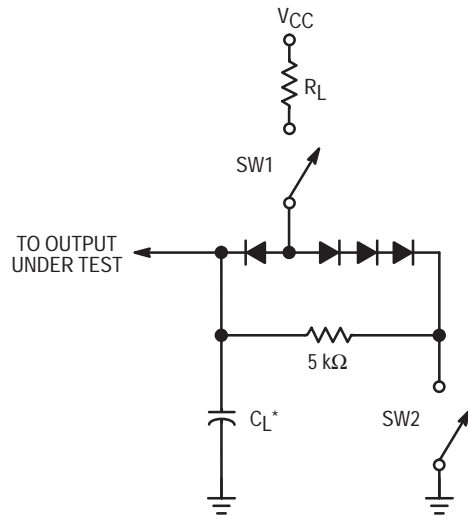


Figure 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 5



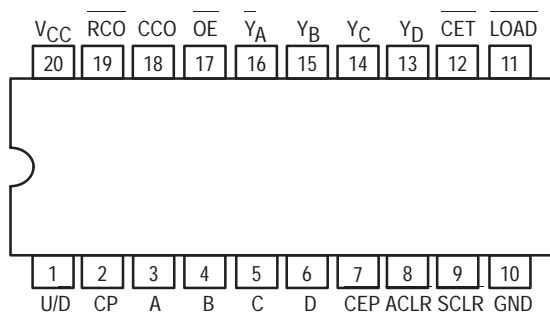
FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

The SN54/74LS569A is designed as programmable up/down BCD and Binary counters respectively. These devices have 3-state outputs for use in bus organized systems. With the exception of output enable (OE) and asynchronous clear (ACLR), all functions occur on the positive edge of the clock pulse (CP).

When the LOAD input is LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Enabling of the counters occurs only when CEP and CET are LOW and $\overline{\text{LOAD}}$ is HIGH. Direction of the count is controlled by the up-down input (U/D), HIGH counts up and LOW counts down. High-speed counting and cascading is implemented by internal look-ahead carry logic and an active LOW ripple carry output (RCO). On the LS569A, the RCO is LOW at binary 15 during up-count and during down-count it is also LOW at binary 0. During normal cascading operation RCO connected to the succeeding block at CET is the only requisite. When counting and when RCO is LOW, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse. Two active LOW reset lines are provided, a master reset asynchronous clear (ACLR) and a synchronous clear (SCLR). When in a HIGH state, the output control (OE) input forces the counter output into a HIGH impedance state and when LOW, the counter outputs are enabled.

- ESD > 3500 Volts

CONNECTION DIAGRAM (TOP VIEW)



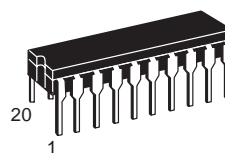
V_{CC} = PIN 20
GND = PIN 10

Note: Pin 1 is marked for orientation.

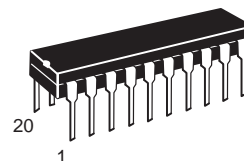
SN54/74LS569A

FOUR-BIT UP/DOWN COUNTER WITH THREE-STATE OUTPUTS

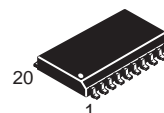
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High Except RCO, CCO	54 74			-1.0 -2.6	mA
I_{OH}	Output Current — High RCO, CCO	54, 74			-0.44	mA
I_{OL}	Output Current — Low Except RCO, CCO	54 74			12 24	mA
I_{OL}	Output Current — Low, RCO, CCO	54 74			4.0 8.0	mA

SN54/74LS569A

FUNCTION TABLE

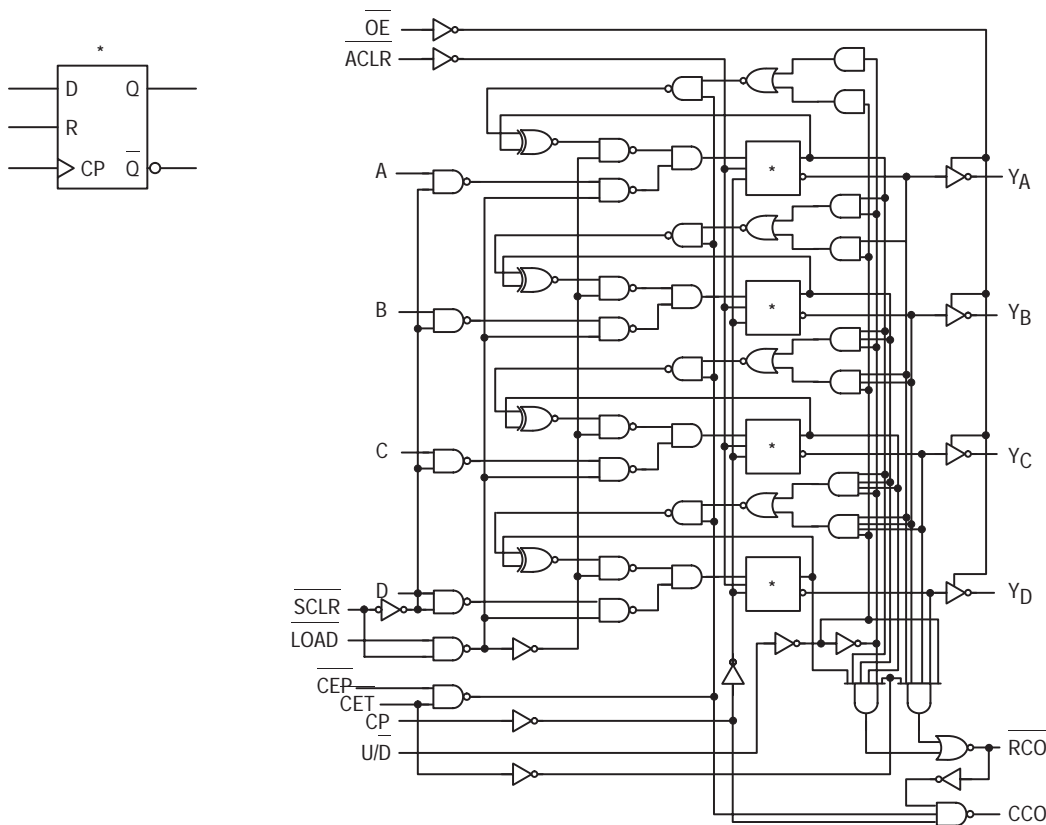
INPUTS											OUTPUTS							
CP	D	C	B	A	LOAD	CET	CEP	U/D	ACLR	SCLR	OE	RCO	CCO	Y _D	Y _C	Y _B	Y _A	
↑	X	X	X	X	H	L	L	H	H	H	L	A/R	A/R	$(Q_T - CP) + 1$				Count Up
↑	X	X	X	X	H	L	L	L	H	H	L	A/R	A/R	$(Q_T - CP) - 1$				Count Down
↑	X	X	X	X	H	H	X	X	H	H	L	H	H	NC	NC	NC	NC	Count Inhibit
↑	X	X	X	X	H	L	H	X	H	H	L	A/R	H	NC	NC	NC	NC	Count Inhibit
Ω	X	X	X	X	X	L	L	H	H	H	L	L	∅	H	H	H	H	Overflow
↑	X	X	X	X	X	L	H	H	H	H	L	L	H	H	H	H	H	Overflow
↑	X	X	X	X	X	H	X	H	H	H	L	H	H	H	H	H	H	Overflow Inhibit
∅	X	X	X	X	X	L	L	L	H	H	L	L	∅	L	L	L	L	Underflow
↑	X	X	X	X	X	L	H	L	H	H	L	L	H	L	L	L	L	Underflow
↑	X	X	X	X	X	H	X	L	H	H	L	H	H	L	L	L	L	Underflow Inhibit
↑	L	H	L	H	L	X	X	X	H	H	L	H	H	L	H	L	H	Load Example
↑	X	X	X	X	X	H	X	H	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
∅	X	X	X	X	X	L	L	L	H	L	L	L	∅	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	L	H	L	H	L	L	L	H	L	L	L	L	Clear (Synchronous)
↑	X	X	X	X	X	H	X	L	H	L	L	H	H	L	L	L	L	Clear (Synchronous)
X	X	X	X	X	X	X	X	H	L	X	L	H	H	L	L	L	L	Asynchronous Clear
∅	X	X	X	X	X	L	L	L	L	X	L	L	∅	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	L	H	L	L	X	L	L	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	H	X	L	L	X	L	H	H	L	L	L	L	Asynchronous Clear
X	X	X	X	X	X	X	X	X	X	X	H	X	X	Hi-Z				Output Disabled

$(Q_T - CP)$ = Output state prior to clock edge
 NC = No change

A/R = Assumes required output state;
 High except during Overflow and Underflow

X = Don't care

LOGIC DIAGRAM

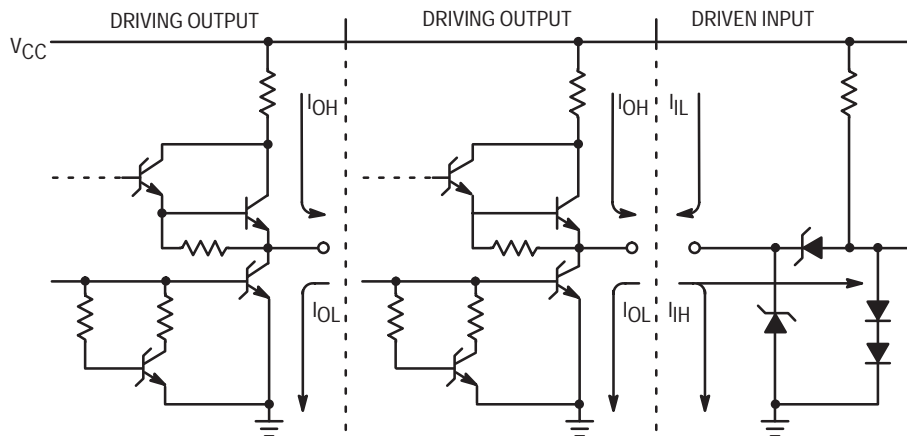


SN54/74LS569A

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.	$\overline{\text{ACLR}}$	Asynchronous Clear. <u>Master</u> reset of counters to zero when ACLR is LOW, independent of the clock.
$\overline{\text{CEP}}$	Count Enable Parallel. Can be used to enable and inhibit <u>counting</u> in high speed cascaded operation. CEP must be LOW to count.	$\overline{\text{SCLR}}$	Synchronous clear of <u>counters</u> to zero on the next clock edge when SCLR is LOW.
$\overline{\text{CET}}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.	$\overline{\text{OE}}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.	Y_A, Y_B, Y_C, Y_D	The four counter outputs.
$\overline{\text{LOAD}}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.	$\overline{\text{RCO}}$	Ripple Carry Output. Output will be LOW on the <u>maximum count</u> on up-count. Upon down-count, RCO is LOW at 0000.
$\overline{\text{U/D}}$	Up/Down Count Control. HIGH counts up and LOW counts down.	CCO	<u>Clock</u> Carry Output. While counting and RCO is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

SN54/74LS569A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	YA-YD	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
			74	2.4	3.1	V	
	RCO, CCO	54	2.5	3.5	V		
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = I _{OL} MAX V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _O = 2.7 V
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _O = 0.4 V
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		CET			-0.8	mA	
I _{OS}	Short Circuit Current (Note 1)	RCO, CCO	-20		-100	mA	V _{CC} = MAX
		Others	-30		-130	mA	
I _{CC}	Power Supply Current, 3-State				43	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		

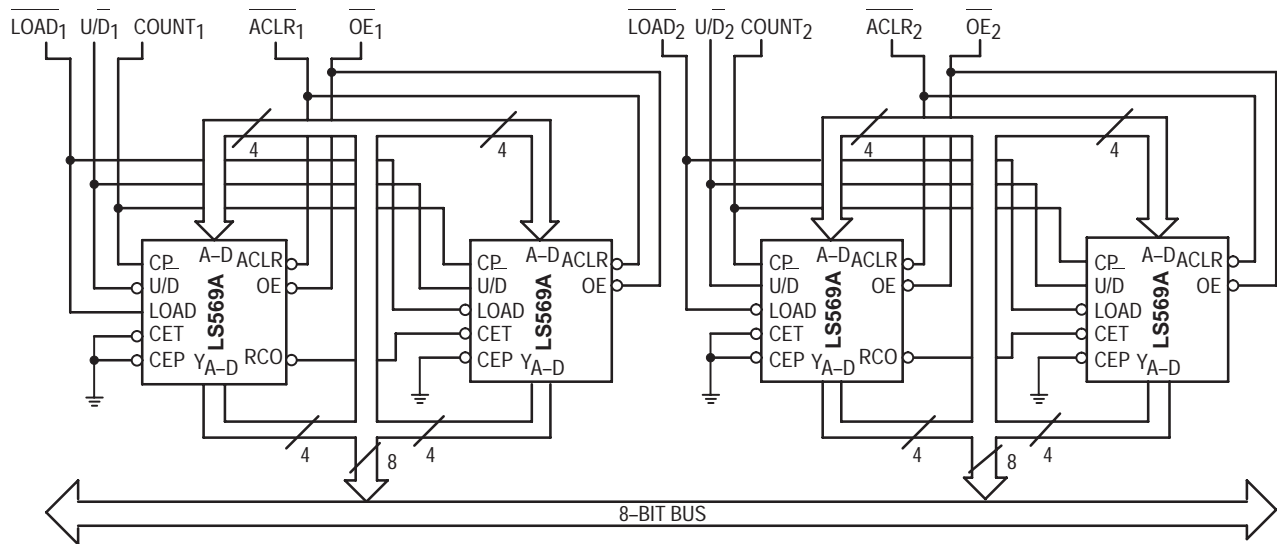
f _{MAX}	Maximum Toggle Frequency	35			MHz	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay Clock to Q			15 20	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to RCO			14 15	ns	
t _{PLH} t _{PHL}	Propagation Delay U/D to RCO			20 24	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to RCO			20 25	ns	
t _{PLH} t _{PHL}	Propagation Delay CET to CCO			16 28	ns	
t _{PLH} t _{PHL}	Propagation Delay CEP to CCO			16 26	ns	
t _{PLH} t _{PHL}	Propagation Delay Clock to CCO			15 17	ns	
t _{PLH} t _{PHL}	Propagation Delay ACLR to Q			22 32	ns	
t _{PZH} t _{PZL}	Output Enable Time			15 20	ns	
t _{PHZ} t _{PLZ}	Output Disable Time			20 27	ns	C _L = 5.0 pF

SN54/74LS569A

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width (Low)	20			ns	$V_{CC} = 5.0\text{ V}$
t_s	Setup Time, A, B, C, D	20			ns	
t_s	Setup Time, SCLR	20			ns	
t_s	Setup Time, LOAD	25			ns	
t_s	Setup Time, U/D	30			ns	
t_s	Setup Time, CET, CEP	20			ns	
t_h	Hold Time, Any Inputs	0			ns	
t_{rec}	ACLR	15			ns	

MICROPROGRAMMABLE DUAL-EVENT 8-BIT COUNTERS

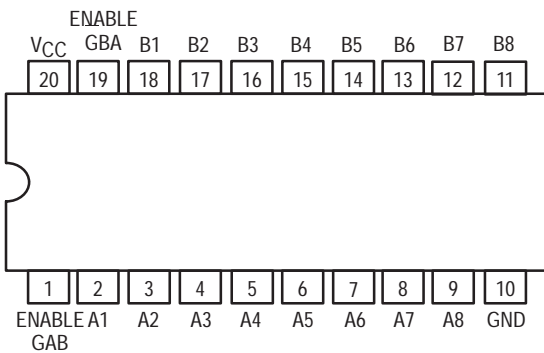




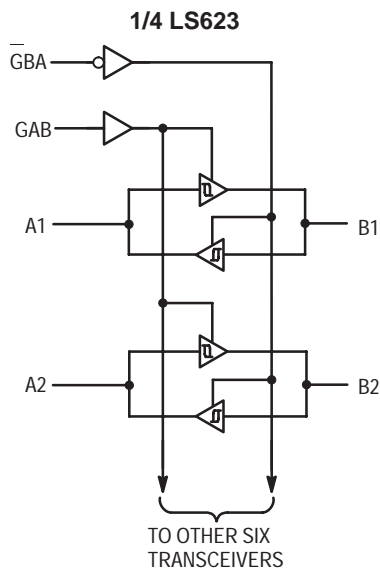
OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

The SN54/74LS623 series is an octal bus transceiver designed for asynchronous two-way communication between data buses. Control function implementation allows maximum timing flexibility. Enable inputs may be used to disable the device so that buses are effectively isolated. Depending on the Logic Levels at the enable inputs, Data transmission is allowed from the A bus to the B bus or from the B bus to the A bus. The dual-enable configuration gives the LS623 the capability to store data by simultaneous enabling of GBA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled all other data sources to the two sets of bus lines (16 in all) will remain at their last states.

CONNECTION DIAGRAM (TOP VIEW)

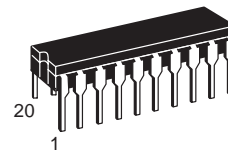


BLOCK DIAGRAM

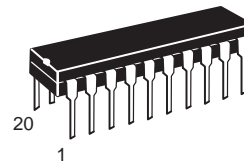


SN54/74LS623

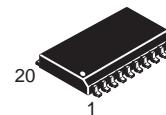
OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

FUNCTION TABLE

ENABLE INPUTS		OPERATION
GBA	GAB	LS623
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus, A data to B bus

H = HIGH Level, L = LOW Level, X = Irrelevant

SN54/74LS623

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-3.0	mA
		54 74			-12 -15	mA
I _{OL}	Output Current — Low	54			12	mA
		74			24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.5	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.6		
V _{T+} -V _{T-}	Hysteresis		0.2	0.4		V	V _{CC} = MIN
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4		V	V _{CC} = MIN, I _{OH} = ± 3.0 mA
		54, 74	2.0			V	V _{CC} = MIN, I _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V
I _{OZL}	Output Off Current LOW				-400	μA	V _{CC} = MAX, V _{OUT} = 4.0 V
I _{IH}	Input HIGH Current	A, or B, GBA or GAB			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		GAB or GAB			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		A or B			0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{OS}	Short Circuit Current (Note 1)		-40		-225	mA	V _{CC} = MAX
I _{CC}	Power Supply Current					mA	V _{CC} = MAX
	Total Output HIGH				70		
	Total Output LOW				90		
	Total at HIGH Z				95		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS623

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay A to B		8.0 11	15 15	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay B to A		8.0 11	15 15	ns	
t _{PZL} t _{PZH}	Output Enable Time GBA to A		31 26	40 40	ns	
t _{PZL} t _{PZH}	Output Enable Time GAB to B		31 26	40 40	ns	
t _{PLZ} t _{PHZ}	Output Disable Time GBA to A		15 15	25 25	ns	C _L = 5.0 pF
t _{PLZ} t _{PHZ}	Output Disable Time GAB to B		15 15	25 25	ns	



OCTAL BUS TRANSCEIVERS

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. These circuits allow data transmission from the A bus to B or from the B bus to A bus depending upon the logic level of the direction control (DIR) input. Enable input (G) can disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
LS640	3-State	Inverting
LS641	Open-Collector	True
LS642	Open-Collector	Inverting
LS645	3-State	True

FUNCTION TABLE

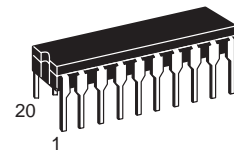
CONTROL INPUTS		OPERATION	
G	DIR	LS640 LS642	LS641 LS645
		L	L
L	H	A data to B bus	A data to B bus
H	X	Isolation	Isolation

H = HIGH Level, L = LOW Level, X = Irrelevant

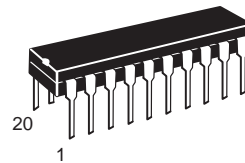
SN54/74LS640
SN54/74LS641
SN54/74LS642
SN54/74LS645

OCTAL BUS TRANSCEIVERS

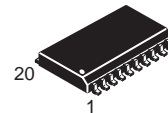
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03

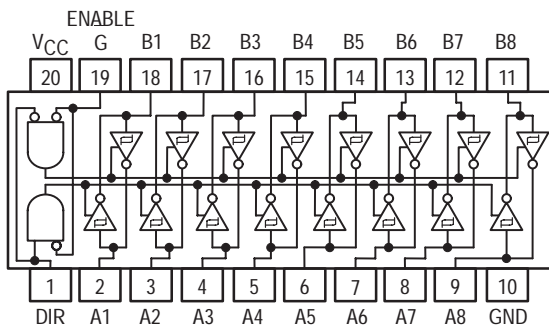


DW SUFFIX
 SOIC
 CASE 751D-03

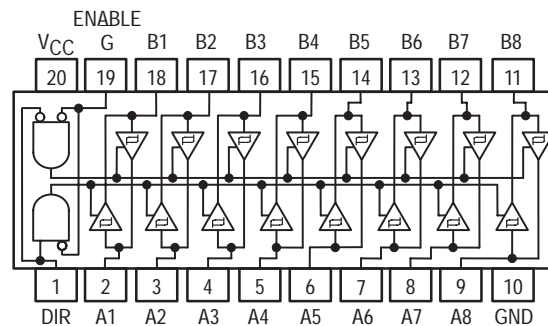
ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

CONNECTION DIAGRAMS DIP (TOP VIEW)



SN54/74LS640
SN54/74LS642



SN54/74LS641
SN54/74LS645

SN54/74LS640 • SN54/74LS645

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-3.0	mA
		54 74			-12 -15	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.5	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.6			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.4	V	V _{CC} = MIN, I _{OH} = 3.0 mA	
		54, 74	2.0		V	V _{CC} = MIN, I _{OH} = MAX	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA
		74		0.35	0.5	V	I _{OL} = 24 mA
						V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW			-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	A or B, DIR or G		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		DIR or G		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		A or B		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Output Short Circuit Current (Note 1)	-40		-225	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current Total Output HIGH Total, Output LOW Total at HIGH Z			70	mA	V _{CC} = MAX	
				90			
				95			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS640			LS645				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay A to B		6.0 8.0	10 15		8.0 11	15 15	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay B to A		6.0 8.0	10 15		8.0 11	15 15		
t _{PZL} t _{PZH}	Output Enable Time G, DIR to A		31 23	40 40		31 26	40 40		
t _{PZL} t _{PZH}	Output Enable Time G, DIR to B		31 23	40 40		31 26	40 40		
t _{PLZ} t _{PHZ}	Output Disable Time G, DIR to A		15 15	25 25		15 15	25 25	ns	C _L = 5.0 pF
t _{PLZ} t _{PHZ}	Output Disable Time G, DIR to B		15 15	25 25		15 15	25 25		

SN54/74LS641 • SN54/74LS642

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Current — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.5	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.6		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54, 74		100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 12 mA
		74	0.35	0.5	V	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				-0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current Total, Output HIGH			70	mA	V _{CC} = MAX
	Total, Output LOW			90		
	Total at HIGH Z			95		

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS641			LS642				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, A to B		17 16	25 25		19 14	25 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, B to A		17 16	25 25		19 14	25 25		
t _{PLH} t _{PHL}	Propagation Delay, G, DIR to A		23 34	40 50		26 43	40 60		
t _{PLH} t _{PHL}	Propagation Delay, G, DIR to B		25 37	40 50		28 39	40 60		



SYNCHRONOUS 4-BIT UP/DOWN COUNTER

The SN54/74LS669 is a synchronous 4-bit up/down counter. The LS669 is a 4-bit binary counter. For high speed counting applications, this presettable counter features an internal carry lookahead for cascading purposes. By clocking all flip-flops simultaneously so the outputs change coincident with each other (when instructed to do so by the count enable inputs and internal gating) synchronous operation is provided. This helps to eliminate output counting spikes, normally associated with asynchronous (ripple-clock) counters. The four master-slave flip-flops are triggered on the rising (positive-going) edge of the clock waveform by a buffered clock input.

Circuitry of the load inputs allows loading with the carry-enable output of the cascaded counters. Because loading is synchronous, disabling of the counter by setting up a low level on the load input will cause the outputs to agree with the data inputs after the next clock pulse.

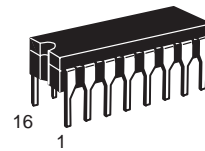
Cascading counters for N-bit synchronous applications are provided by the carry look-ahead circuitry, without additional gating. Two count-enable inputs and a carry output help accomplish this function. Count-enable inputs (P and T) must both be low to count. The level of the up-down input determines the direction of the count. When the input level is low, the counter counts down, and when the input is high, the count is up. Input T is fed forward to enable the carry output. The carry output will now produce a low level output pulse with a duration \approx equal to the high portion of the Q_A output when counting up and when counting down \approx equal to the low portion of the Q_A output. This low level carry pulse may be utilized to enable successive cascaded stages. Regardless of the level of the clock input, transitions at the P or T inputs are allowed. By diode-clamping all inputs, transmission line effects are minimized which allows simplification of system design.

Any changes at control inputs (ENABLE \bar{P} , ENABLE \bar{T} , LOAD, UP/DOWN) will have no effect on the operating mode until clocking occurs because of the fully independent clock circuits. Whether enabled, disabled, loading or counting, the function of the counter is dictated entirely by the conditions meeting the stable setup and hold times.

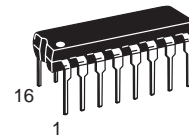
- Programmable Look-Ahead Up/Down Binary/Decade Counters
- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit
- Buffered Outputs

SN54/74LS669

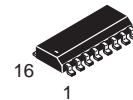
SYNCHRONOUS 4-BIT UP/DOWN COUNTER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

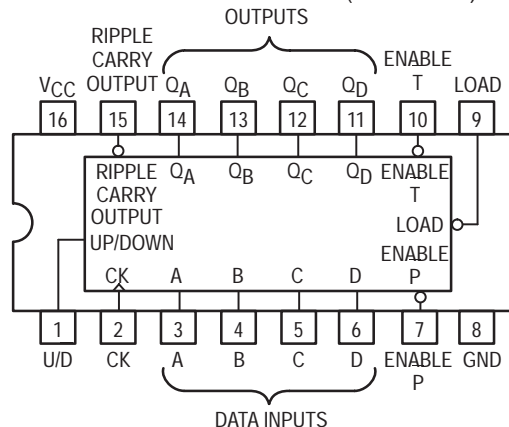


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

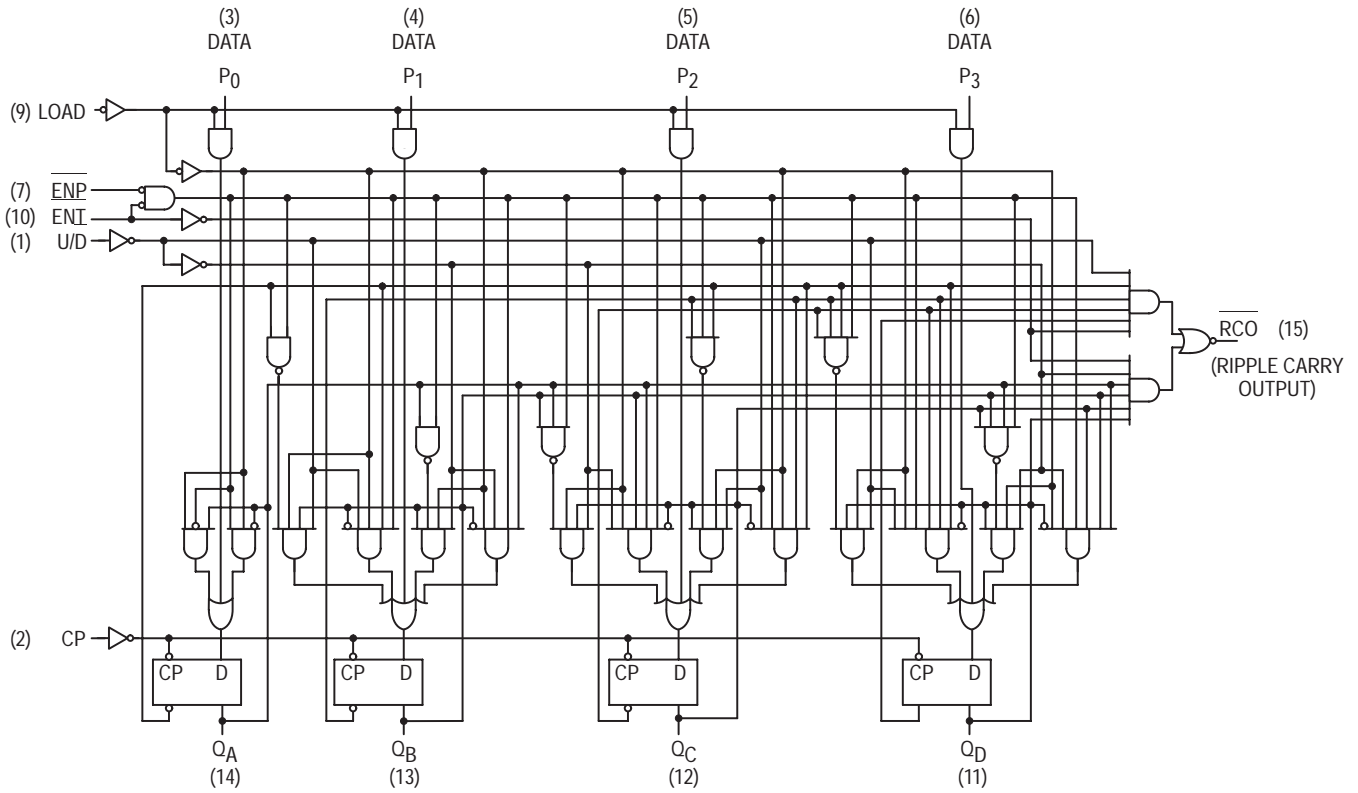
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM (TOP VIEW)



SN54/74LS669

LOGIC DIAGRAM



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS669

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{IH}	Input HIGH Current	Others			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
		Enable T			40	μA	
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
		Enable T			0.2	mA	
I _{IL}	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
		Enable T			-0.8	mA	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current				34	mA	V _{CC} = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

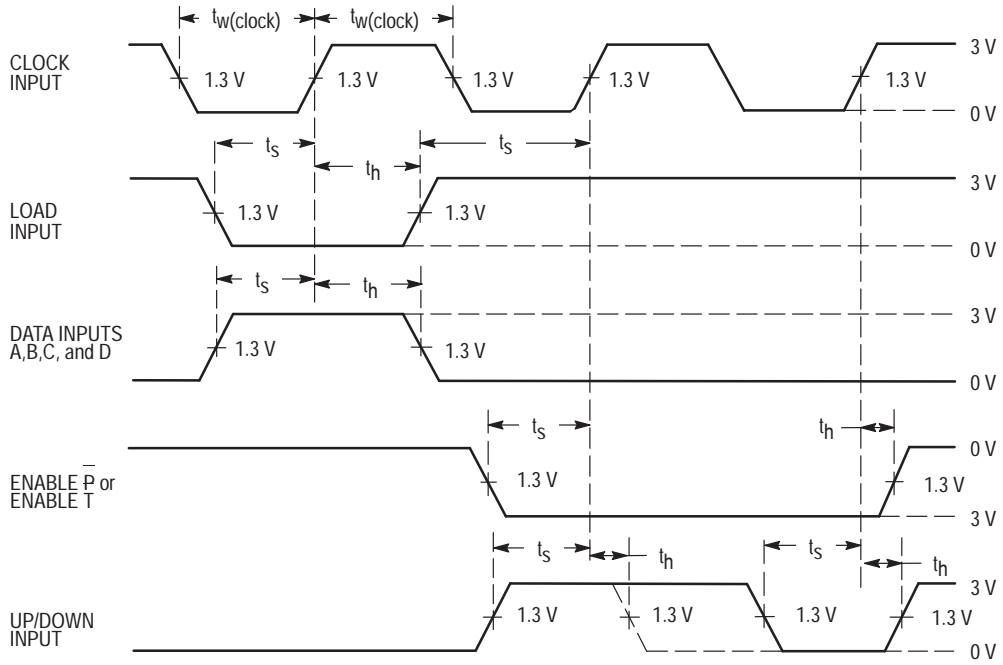
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	32		MHz	C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay, Clock to RCO		26 40	40 60	ns	
t _{PLH} t _{PHL}	Propagation Delay, Clock to Any Q		18 18	27 27	ns	
t _{PLH} t _{PHL}	Enable to $\overline{\text{RCO}}$		11 29	17 45	ns	
t _{PLH} t _{PHL}	$\overline{\text{U/D}}$ to $\overline{\text{RCO}}$		22 26	35 40	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

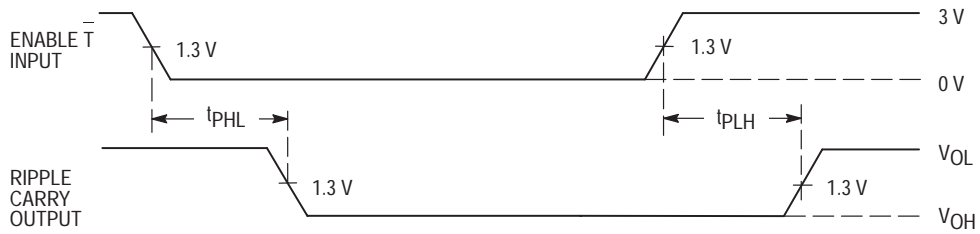
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width	20			ns	V _{CC} = 5.0 V
t _S	Data Setup Time	20			ns	
t _S	Enable Setup Time	35			ns	
t _S	Load Setup Time	25			ns	
t _S	U/D Setup Time	30			ns	
t _H	Hold Time, Any Input	0			ns	

SN54/74LS669

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS





4 x 4 REGISTER FILE WITH 3-STATE OUTPUTS

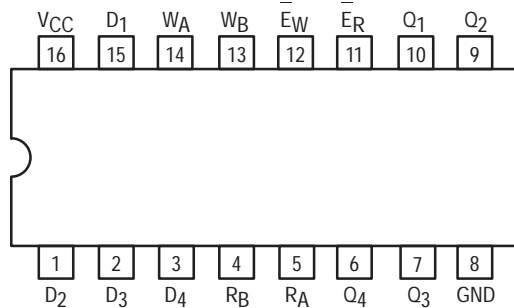
The TTL/MSI SN54/74LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

The SN54/74LS170 provides a similar function to this device but it features open-collector outputs.

- Simultaneous Read/Write Operation
- Expandable to 512 Words by n-Bits
- Typical Access Time to 20 ns
- 3-State Outputs for Expansion
- Typical Power Dissipation of 125 mW

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

D ₁ – D ₄	Data Inputs
W _A , W _B	Write Address Inputs
E _W	Write Enable (Active LOW) Input
R _A , R _B	Read Address Inputs
E _R	Read Enable (Active LOW) Input
Q ₁ – Q ₄	Outputs (Note b)

LOADING (Note a)

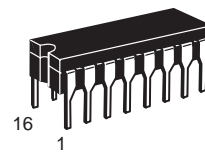
	HIGH	LOW
D ₁ – D ₄	0.5 U.L.	0.25 U.L.
W _A , W _B	0.5 U.L.	0.25 U.L.
E _W	1.0 U.L.	0.5 U.L.
R _A , R _B	0.5 U.L.	0.25 U.L.
E _R	1.5 U.L.	0.75 U.L.
Q ₁ – Q ₄	65 (25) U.L.	15 (7.5) U.L.

NOTES:

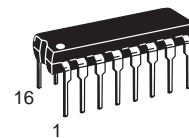
- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military and 65 U.L. for Commercial Temperature Ranges.

SN54/74LS670

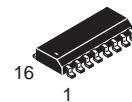
4 x 4 REGISTER FILE WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

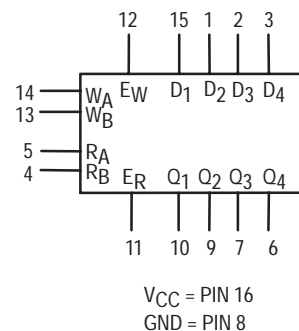


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

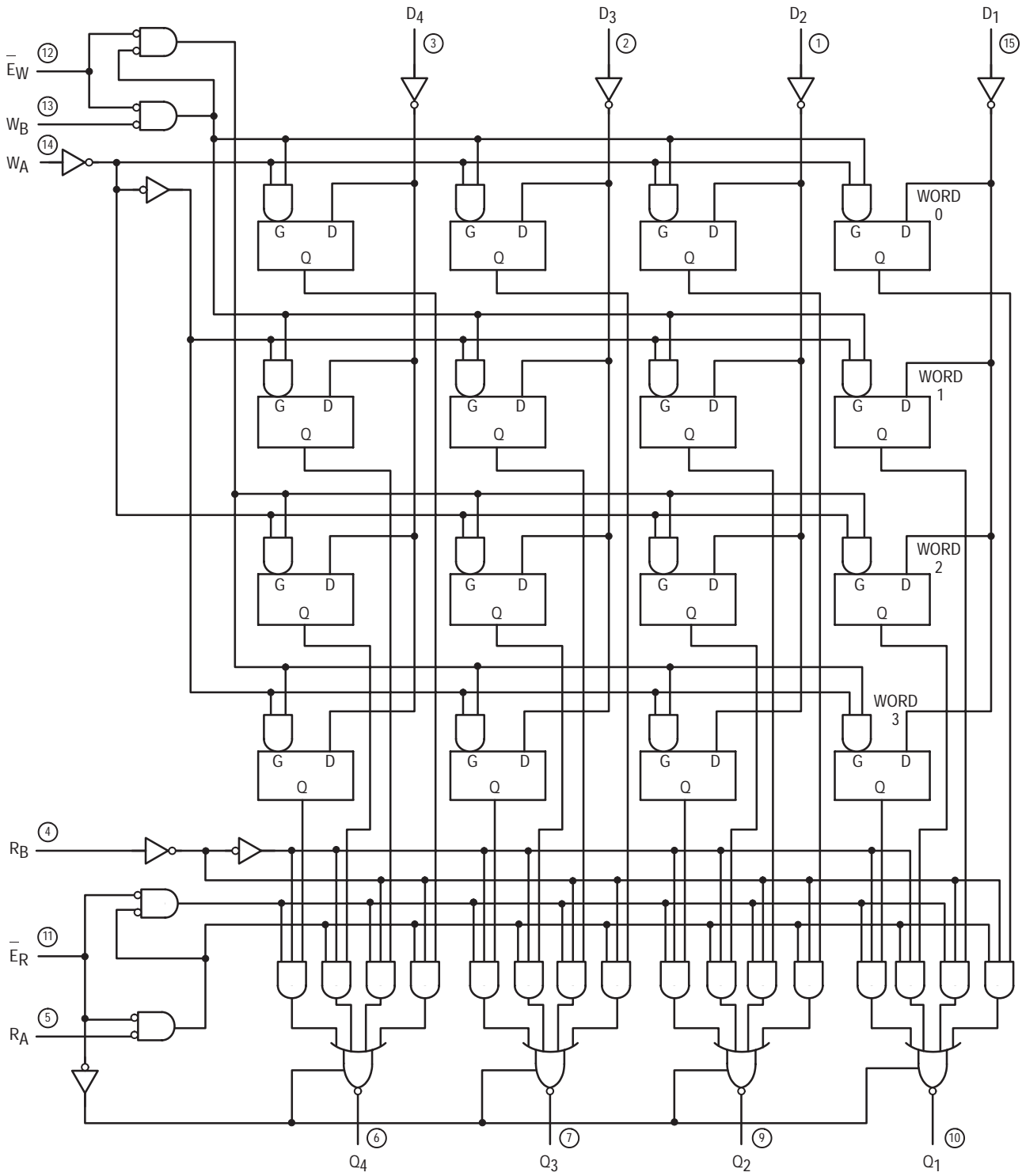
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS670

LOGIC DIAGRAM



V_{CC} = PIN 16
 GND = PIN 8
 ○ = PIN NUMBERS

SN54/74LS670

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	
I _{OZH}	Output Off Current HIGH			20	μA	V _{CC} = MAX, V _O = 2.7 V	
I _{OZL}	Output Off Current LOW			-20	μA	V _{CC} = MAX, V _O = 0.4 V	
I _{IH}	Input HIGH Current D, R, W E _W E _R			20 40 60	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	D, R, W E _W E _R			0.1 0.2 0.3	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current D, R, W E _W E _R			-0.4 -0.8 -1.2	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current			50	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS670

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, R_A or R_B to Output		23 25	40 45	ns	$V_{CC} = 5.0\text{ V}$, $C_L = 45\text{ pF}$
t_{PLH} t_{PHL}	Propagation Delay, E_W to Output		26 28	45 50	ns	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		25 23	45 40	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 22	35 40	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		16 30	35 50	ns	$C_L = 5.0\text{ pF}$

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Pulse Width	25			ns	$V_{CC} = 5.0\text{ V}$
t_s	Setup Time, (D)	10			ns	
t_s	Setup Time, (W)	15			ns	
t_h	Hold Time, (D)	15			ns	
t_h	Hold Time, (W)	5.0			ns	
t_{rec}	Recovery Time	25			ns	

AC WAVEFORMS

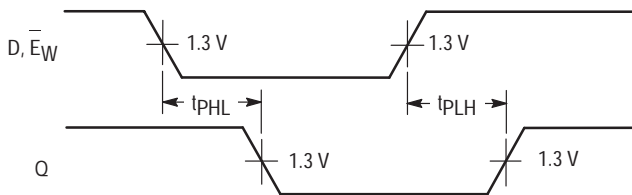


Figure 1

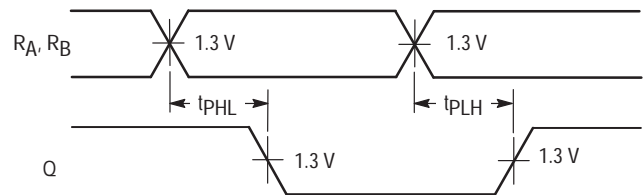


Figure 2

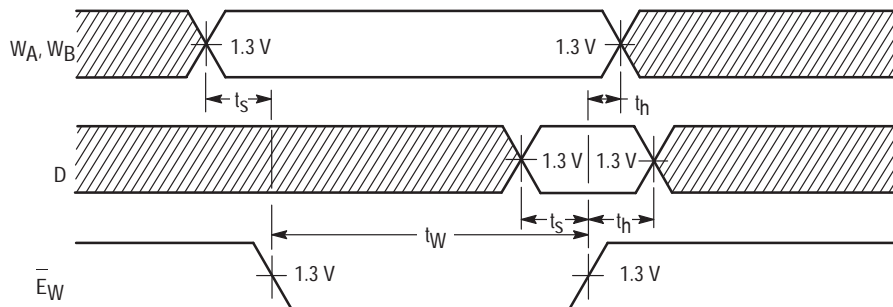


Figure 3

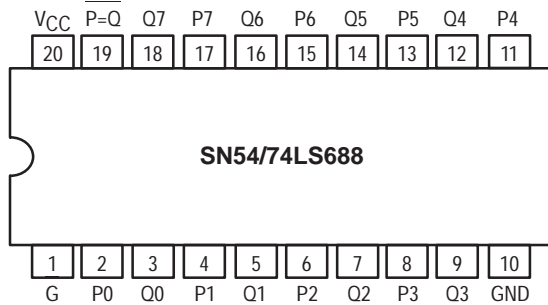
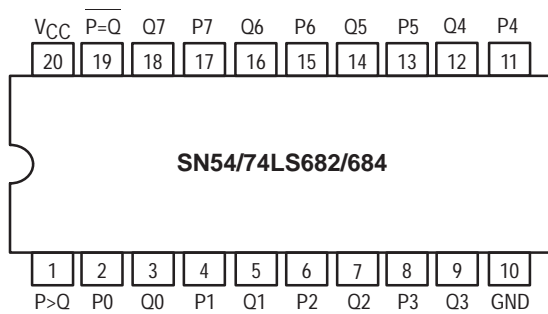


8-BIT MAGNITUDE COMPARATORS

The SN54/74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide P = Q outputs and the LS682 and LS684 have P > Q outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 kΩ pullup resistor on the Q inputs for analog or switch data.

CONNECTION DIAGRAMS (TOP VIEW)

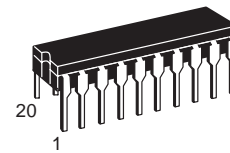


TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

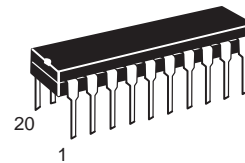
SN54/74LS682
SN54/74LS684
SN54/74LS688

8-BIT MAGNITUDE COMPARATORS

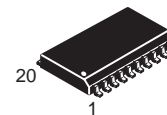
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03



DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		P = Q	P > Q
P, Q	G, GT	G2		
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = HIGH Level, L = LOW Level, X = Irrelevant

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

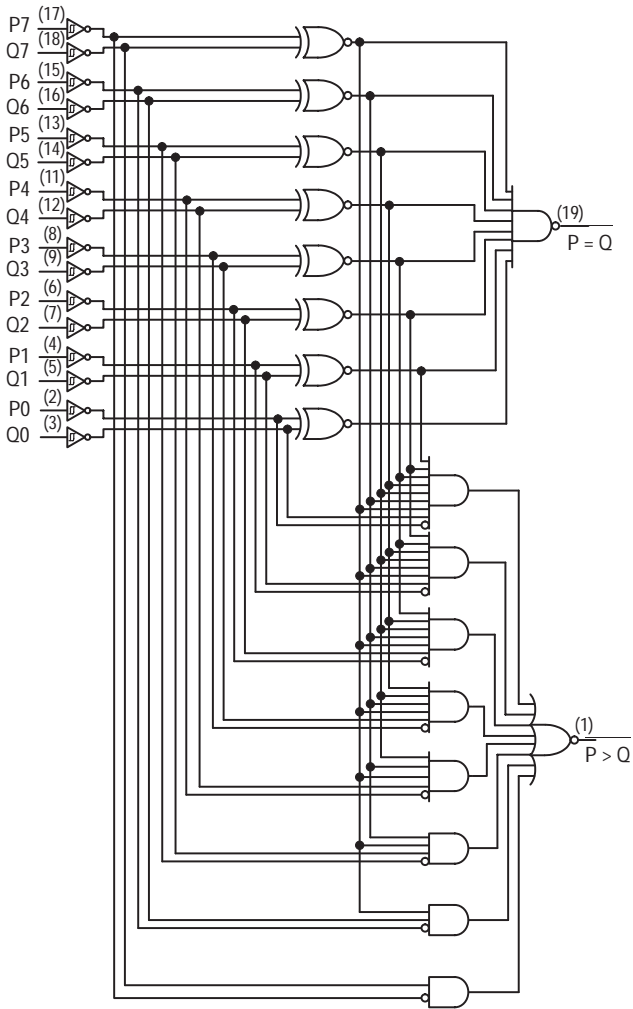
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	I _{OL} = 24 mA	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		LS628-Q Inputs		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
		Others		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	LS682-Q Inputs		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		Others		-0.2	mA		
I _{OS}	Short Circuit Current (Note 1)	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current	LS682		70	mA	V _{CC} = MAX	
		LS684		65	mA		
		LS688		65	mA		

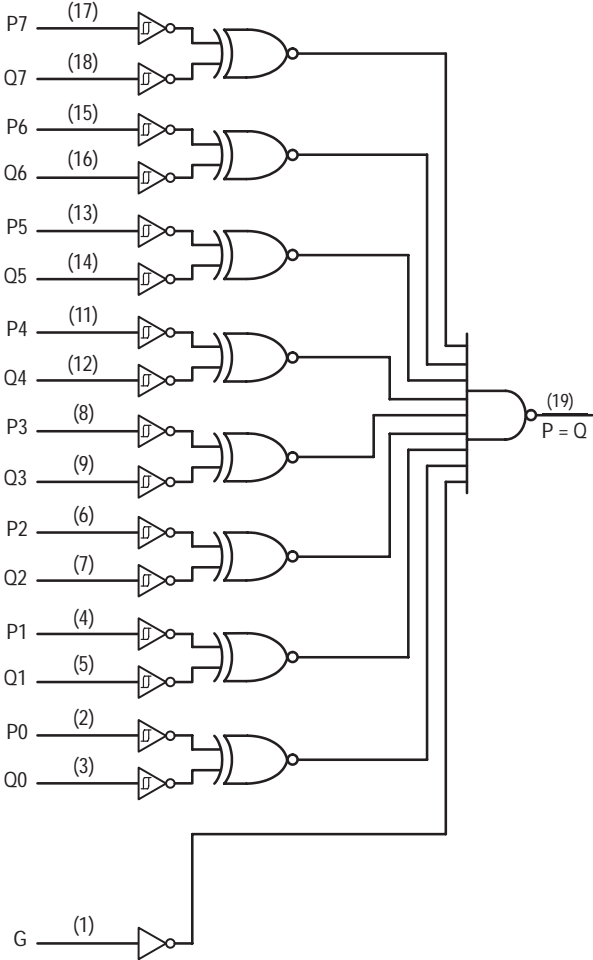
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

LOGIC DIAGRAMS



SN54/74LS682 thru LS684



SN54/74LS688

SN54/74LS682•SN54/74LS684•SN54/74LS688

AC CHARACTERISTICS (T_A = 25°C)

SN54/74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

SN54/74LS684

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

SN54/74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t _{PLH} t _{PHL}	Propagation Delay, $\overline{G}, \overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	



TRI-STATE OCTAL BUFFERS

The SN54/74LS795 thru SN54/74LS798 device types provide a second source for the 71/81LS95 thru 71/81LS98 series. These devices are octal low power Schottky versions of the 70/8095 thru 70/8098 3-STATE Hex Buffers. The LS795 and LS797 are noninverting and the LS796 and LS798 are inverting functions. On each buffer, one of the two inputs is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer. On the LS795 and LS796 access is through a 2-input NOR gate, with all eight 3-STATE enable lines common. On the LS797 and LS798, four buffers are enabled from one common line and the other four buffers from another common line. On all device types the 3-STATE condition is achieved by applying a high logic level to the enable pins.

TRUTH TABLES

LS795

INPUTS			OUTPUT
G1	G2	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

LS796

INPUTS			OUTPUT
G1	G2	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

LS797

INPUTS		OUTPUT
G	A	Y
H	X	Z
L	H	H
L	L	L

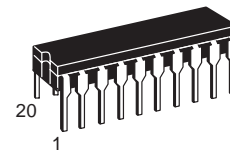
LS798

INPUTS		OUTPUT
G	A	Y
H	X	Z
L	H	L
L	L	H

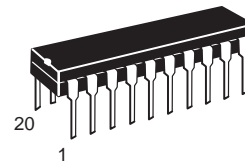
SN54/74LS795
SN54/74LS796
SN54/74LS797
SN54/74LS798

TRI-STATE OCTAL BUFFERS

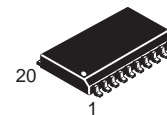
LOW POWER SCHOTTKY



J SUFFIX
 CERAMIC
 CASE 732-03



N SUFFIX
 PLASTIC
 CASE 738-03



DW SUFFIX
 SOIC
 CASE 751D-03

ORDERING INFORMATION

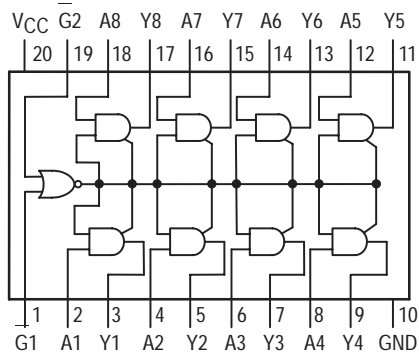
SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

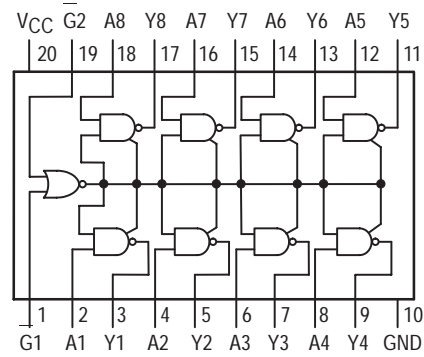
Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54			-2.6	mA
		74			-5.0	
I _{OL}	Output Current — Low	54			8.0	mA
		74			16	

SN54/74LS795 • SN54/74LS796
SN54/74LS797 • SN54/74LS798

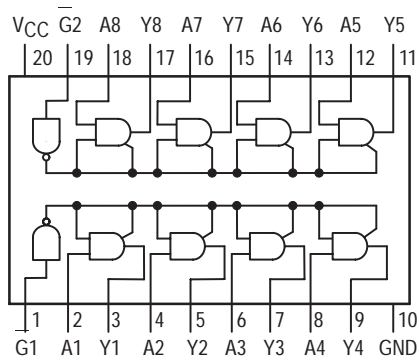
LOGIC DIAGRAMS



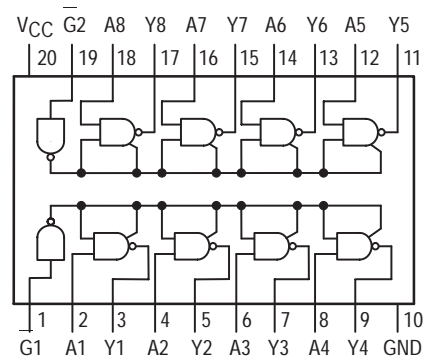
SN54/74LS795



SN54/74LS796



SN54/74LS797



SN54/74LS798

SN54/74LS795 THRU SN54/74LS798

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 8.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 16 mA	
I _{OZH}	Output Off Current — HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current — LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					-0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current A Input, Both G at 0.4 V G Input				-0.4 -0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
	A Input, Both G at 2.0 V				-20	μA	V _{CC} = MAX, V _{IN} = 0.5 V	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current	LS795/LS797			26	mA	V _{CC} = MAX	
		LS795/LS798			21	mA		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS795/LS797			LS796/LS798				
		Min	Typ	Max	Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay		11 15	16 22		6.0 13	10 17	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{PZH} t _{PZL}	Output Enable Time		16 13	25 20		17 16	27 25	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		13 19	20 27		13 18	20 27	ns	C _L = 5.0 pF

For:colleen

Printed on:Tue, Jun 23, 1998 17:15:53

From book:DL121CH6 (5) VIEW

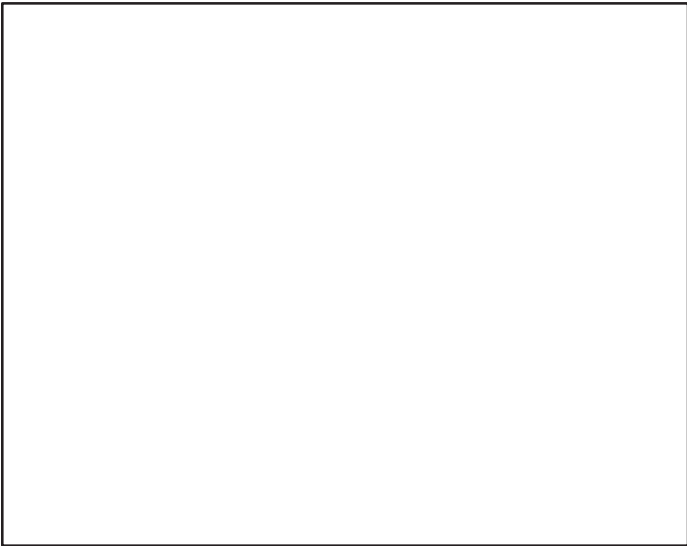
Document:CH6TAB121 VIEW

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FAST AND LS TTL



Reliability Data

6

THE “BETTER” PROGRAM

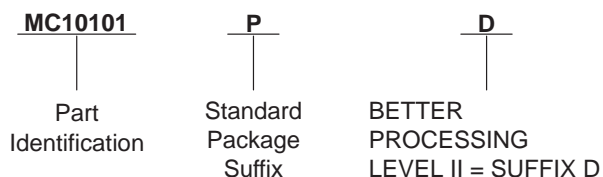
The “BETTER” program is offered on logic only, in dual-in-line ceramic and plastic packages.

Better Processing — Standard Product Plus:

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional).

HOW TO ORDER



Part Marking

The Standard Motorola part number with the corresponding “BETTER” suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. “BETTER” pricing will be quoted as an adder to standard commercial product price.

“RAP” Reliability Audit Program for Logic Integrated Circuits

1.0 INTRODUCTION

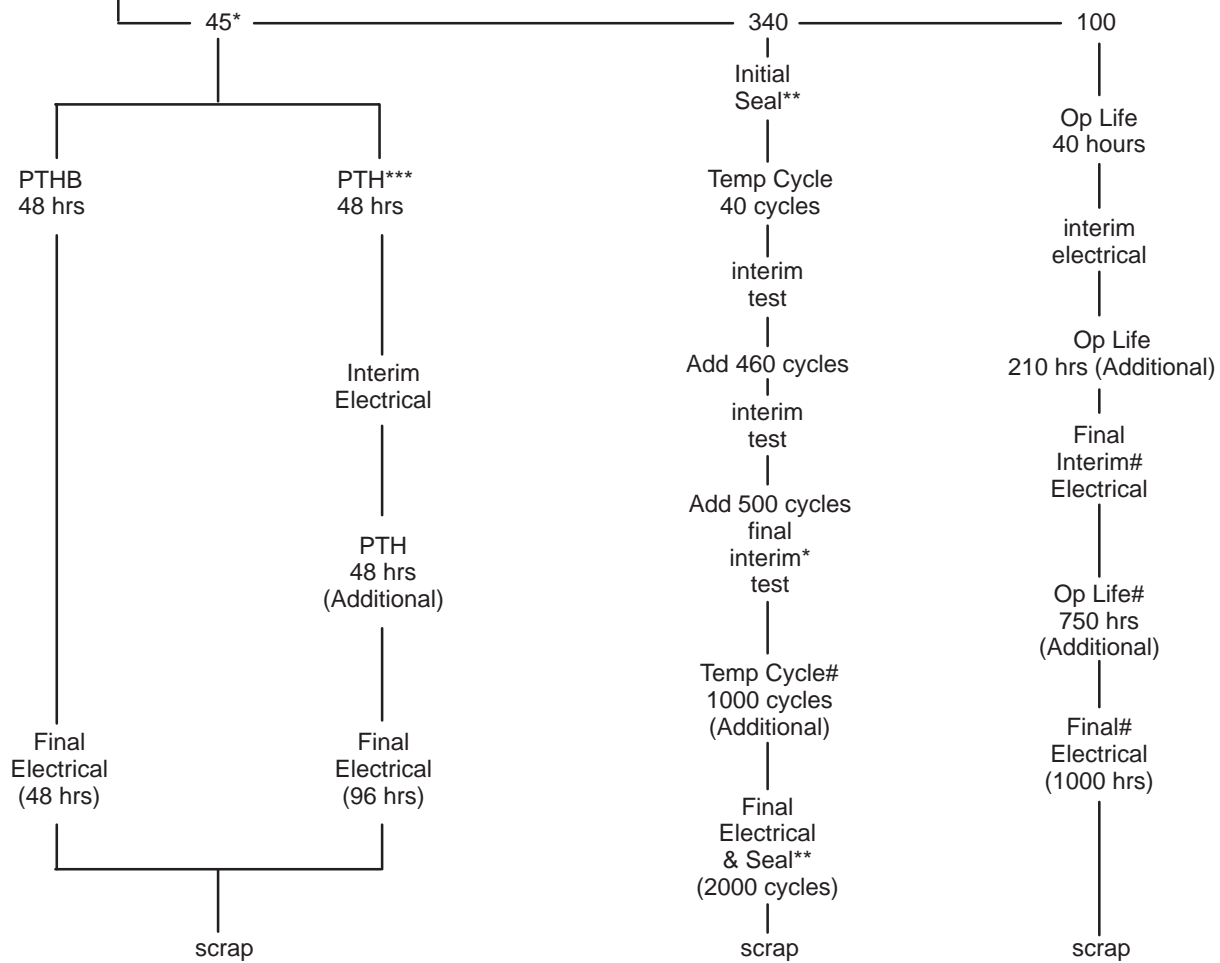
The Reliability Audit Program developed in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are available at all sales offices. Also available is the “Reliability and Quality

Handbook” which contains data for all Motorola Semiconductors (#BR518S).

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.

2.0 RAP TEST FLOW

Pull 500* piece sample from lot following Group A acceptance.



One sample per month for FAST, LS, 10H, 10K, MG CMOS, and HSL CMOS.

* PTHB or PTH not required for hermetic products: reduce total sample size to 450 pcs.

Additional sample reductions for high pin-count devices per TABLE II notes.

** Seal (Fine & Gross Leak) required for hermetic products.

*** PTH to be used when sockets for PTHB are not available.

3.0 TEST CONDITIONS AND COMMENTS

PTHB — 15 psig/121°C/100% RH at rated V_{CC} or V_{EE} — to be performed on plastic encapsulated devices only.

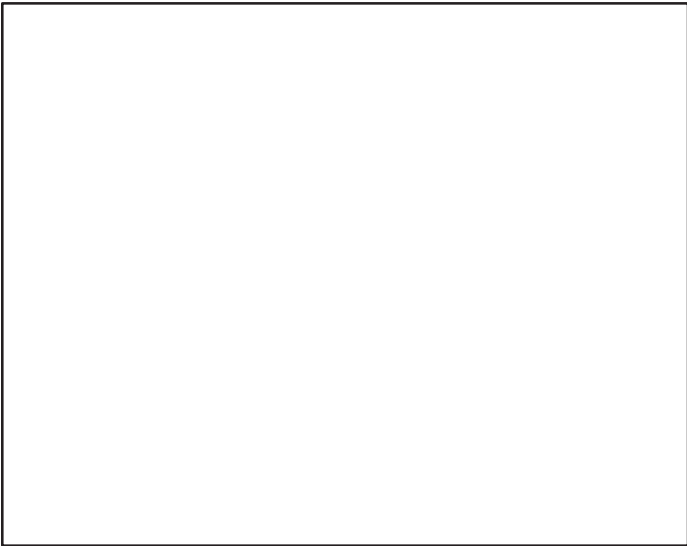
TEMP CYCLING — MIL-STD-883, Method 1010, Condition C, -65°C/+150°C.

OP LIFE — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias), $T_A = 145^\circ\text{C}$.

NOTES:

1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each logic I/C product family (MECL, TTL, etc.) and will include all assembly locations (Korea, Philippines, Malaysia, etc.)
5. 16 hrs. PTHB is equivalent to approximately 800 hours of 85°C/85% RH THB for $V_{CC} \leq 15\text{ V}$.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.

FAST AND LS TTL



**Package Information
Including
Surface Mount**

BIPOLAR LOGIC SURFACE MOUNT

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and/or offer increased functions with the same size product.

SURFACE MOUNT AVAILABILITY

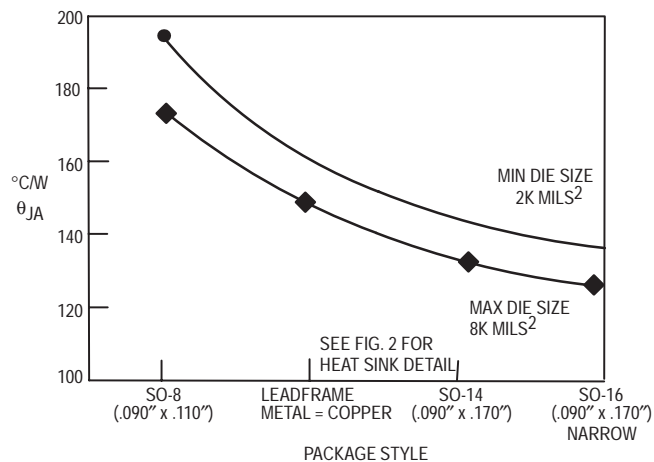
Bipolar Logic is currently offering LS-TTL and FAST-TTL in production quantities in SOIC packages.

Refer to the following Selector Guide (SG366/D) which indicate availability and package type for these families.

These families may be ordered in rails or on Tape and Reel. Refer to Tape and Reel information for ordering details.

THERMAL DATA

The power dissipation of surface mount packages is dependent on many factors that must be taken into consideration in the initial board design. The board material, the board surface metal thickness, pad area and the proximity to other heat generating components all have a bearing on the device dissipation capability.



DATA TAKEN USING PHILIPS SO TEST BOARD # 7322-078, 80873

Figure 2-1. Thermal Resistance, Junction-To-Ambient (°C/W)

Measurement specimens are solder mounted on printed circuit card 19 mm x 28 mm x 1.5 mm in still air. No auxiliary thermal condition aids are used.

This data was collected using thermal test die in 20-pin PLCC packages on PLCC test boards (2.24" x 2.24" x .062" glass epoxy, type FR-4, with solder coated 1 oz./sq. ft. copper).

TAPE AND REEL

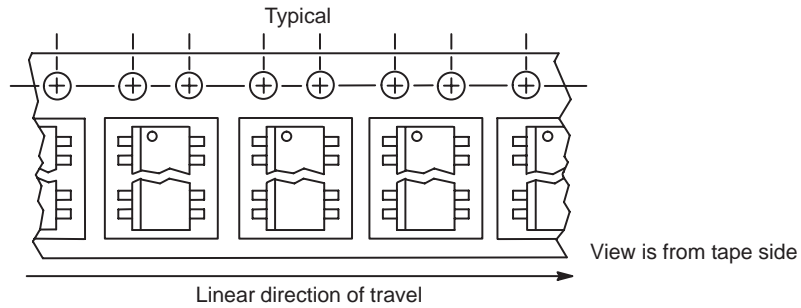
STANDARD BIPOLAR LOGIC INTEGRATED CIRCUITS

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA

RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

MECHANICAL POLARIZATION

SOIC DEVICES



GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix R2
- Tape Width 12 mm to 24 mm (see table)
- Units/Reel (see table)
- No Partial Reel Counts Available and Minimum Lot Size is Per Table

ORDERING INFORMATION

To order devices which are to be delivered in Tape and Reel, add the suffix R2 to the device number being ordered.

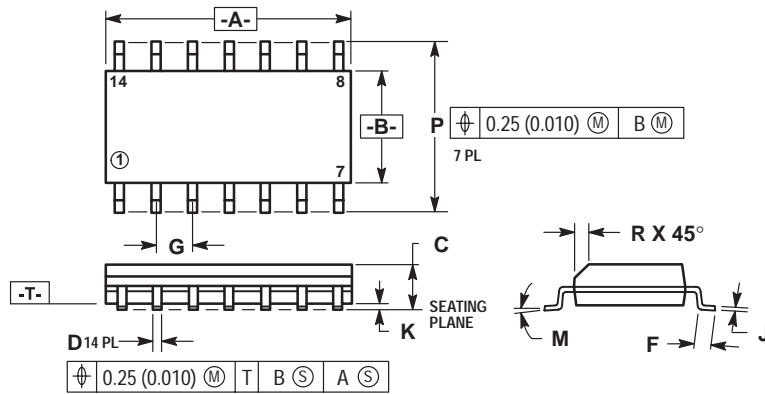
TABLE 2.1 Tape and Reel Data

Device Type	Tape Width (mm)	Device/Reel	Reel Size (inch)	Min Lot Size Per Part No. Tape and Reel
SO-8	12	2,500	13	5,000
SO-14	16	2,500	13	5,000
SO-16	16	2,500	13	5,000
SO-16 Wide	16	1,000	13	5,000
SO-20 Wide	24	1,000	13	5,000

PACKAGE OUTLINES

SOIC

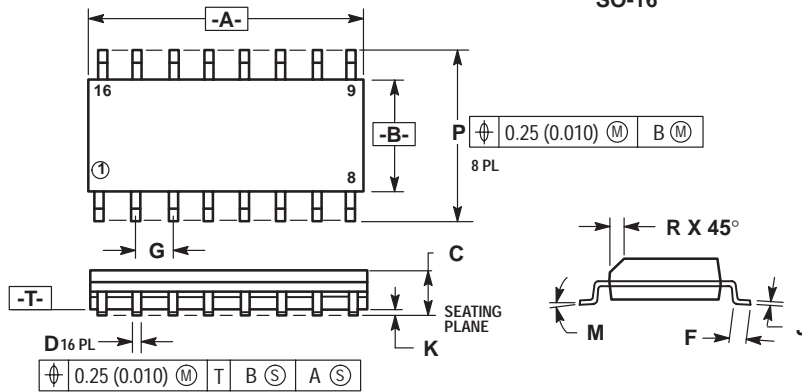
Case 751A-02 D Suffix 14-Pin Plastic SO-14



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIMENSION: MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

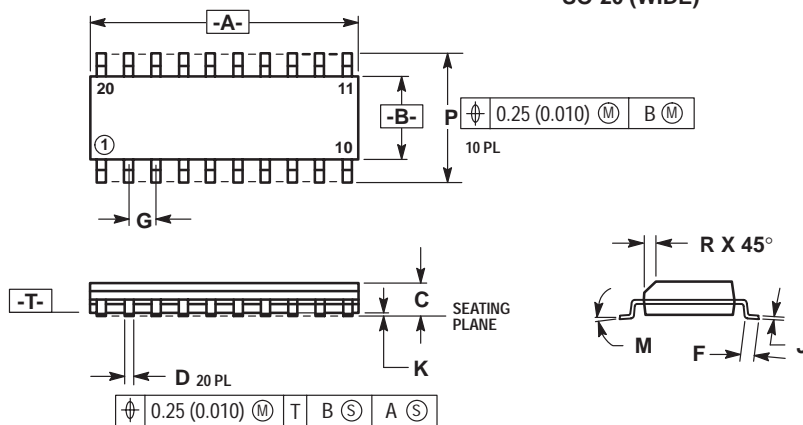
Case 751B-03 D Suffix 16-Pin Plastic SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Case 751D-03 DW Suffix 20-Pin Plastic SO-20 (WIDE)



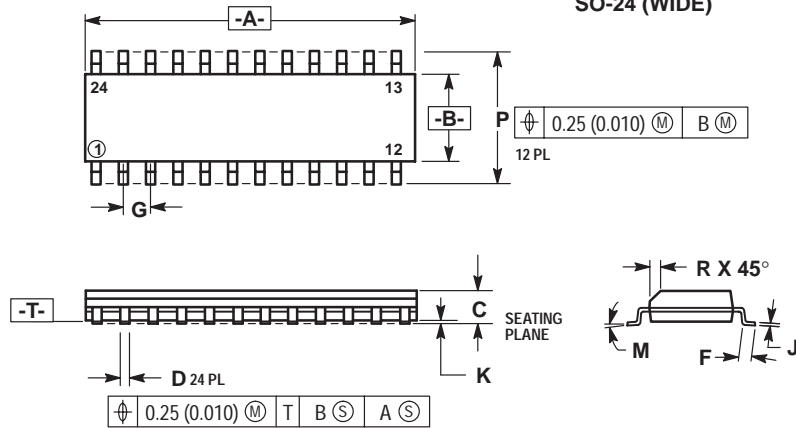
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PACKAGE OUTLINES

SOIC (continued)

Case 751E-03 DW Suffix 24-Pin Plastic SO-24 (WIDE)



NOTES:

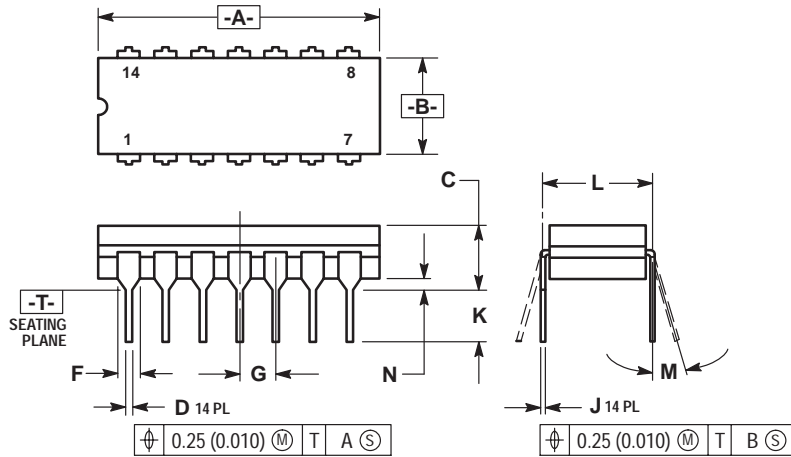
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751E-01 AND -02 OBSOLETE, NEW STANDARD 751E-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE

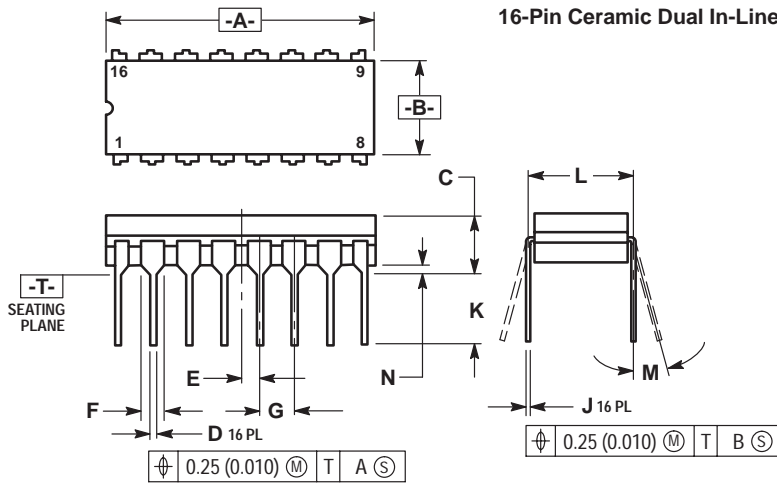
Case 632-08 J Suffix 14-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

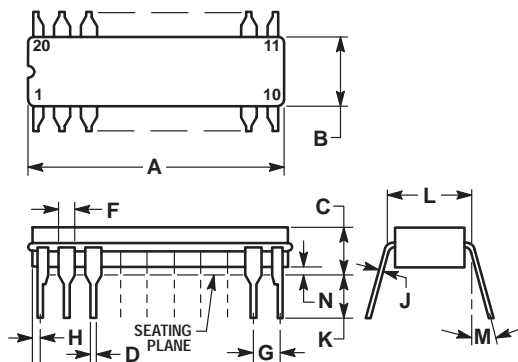
Case 620-09 J Suffix 16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

Case 732-03 J Suffix 20-Pin Ceramic Dual In-Line



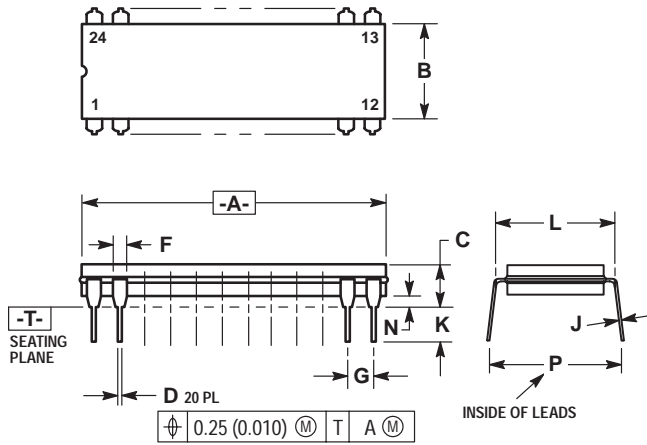
- NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

PACKAGE OUTLINES

CERAMIC DUAL IN-LINE (continued)

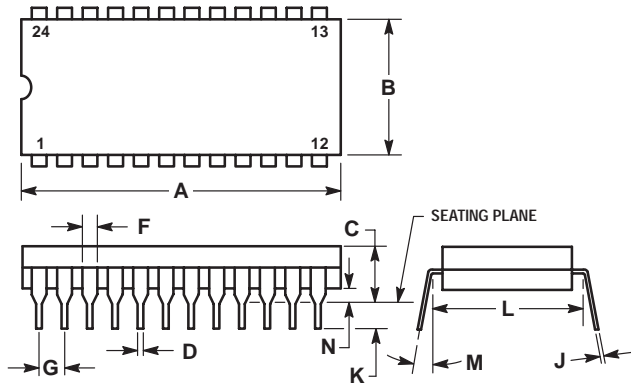
Case 758-01 J Suffix
24-Pin Ceramic Dual In-Line



- NOTES:
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

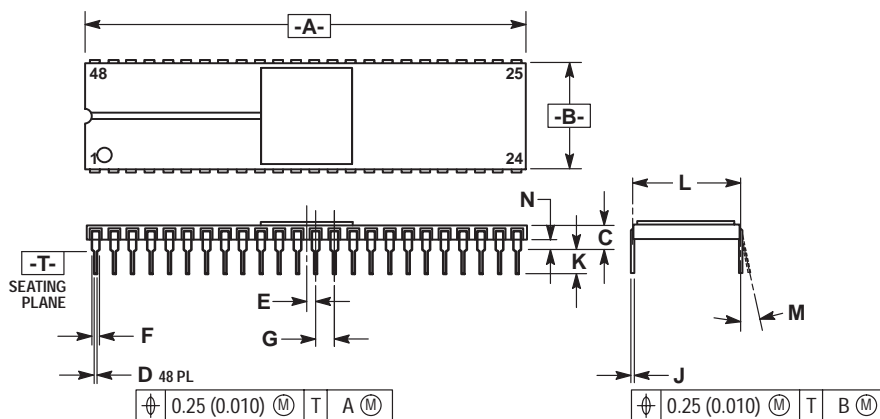
Case 623-05 J Suffix
24-Pin Ceramic Dual In-Line
(WIDE BODY)



- NOTES:
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

Case 740-03 J Suffix
48-Pin Ceramic Dual In-Line



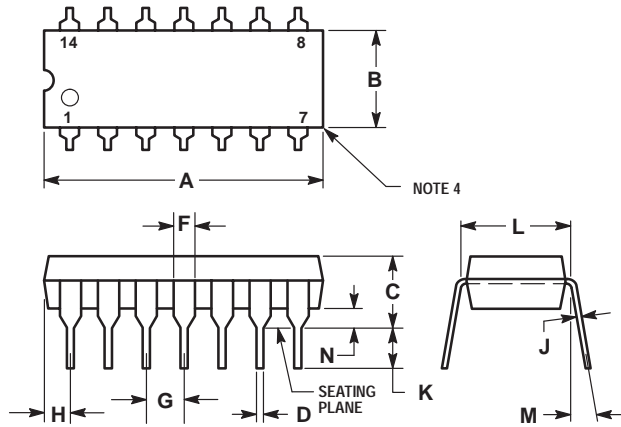
- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIM L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60.36	61.56	2.376	2.424
B	14.64	15.34	0.576	0.604
C	3.05	4.31	0.120	0.170
D	0.381	0.533	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.204	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

PACKAGE OUTLINES

PLASTIC

Case 646-06 N Suffix 14-Pin Plastic

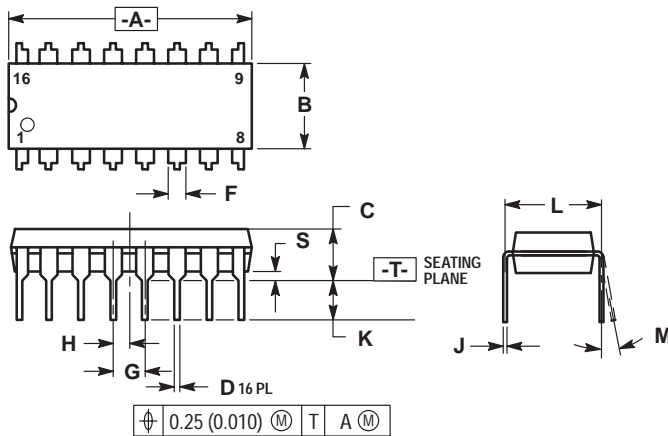


NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION 'L' TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION 'B' DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

Case 648-08 N Suffix 16-Pin Plastic

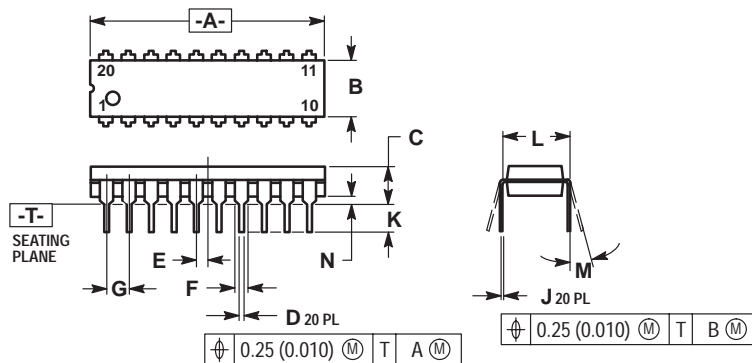


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION 'L' TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION 'B' DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.
- 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 738-03 N Suffix 20-Pin Plastic



NOTES:

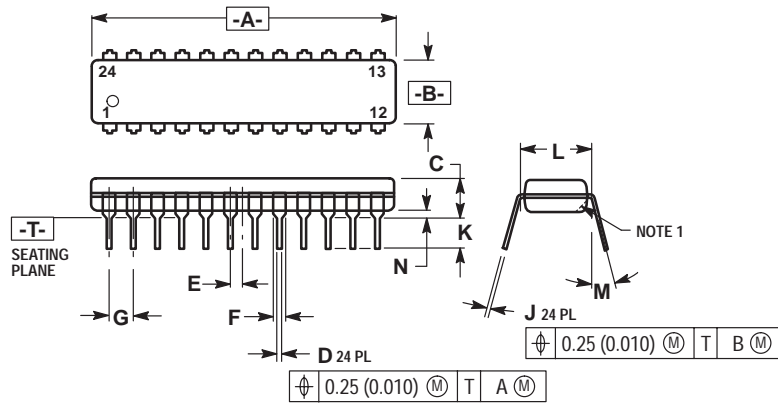
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION 'L' TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION 'B' DOES NOT INCLUDE MOLD FLASH.
- 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

PACKAGE OUTLINES

PLASTIC (continued)

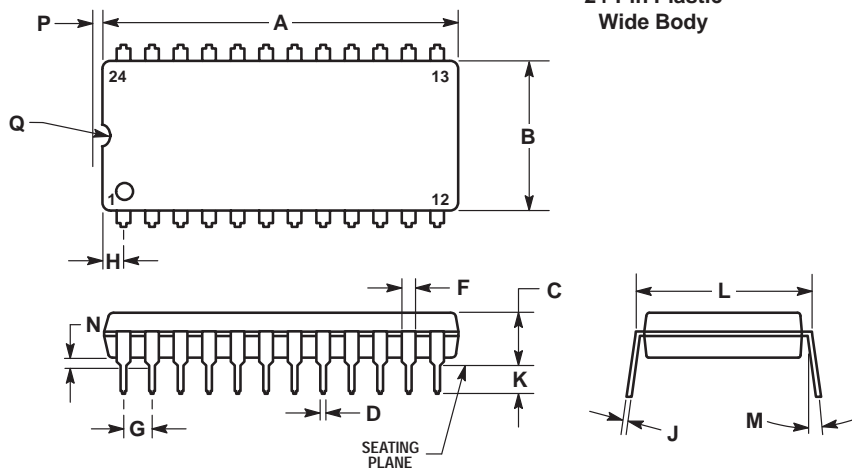
Case 724-03 N Suffix 24-Pin Plastic



- NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.01	0.020	0.040

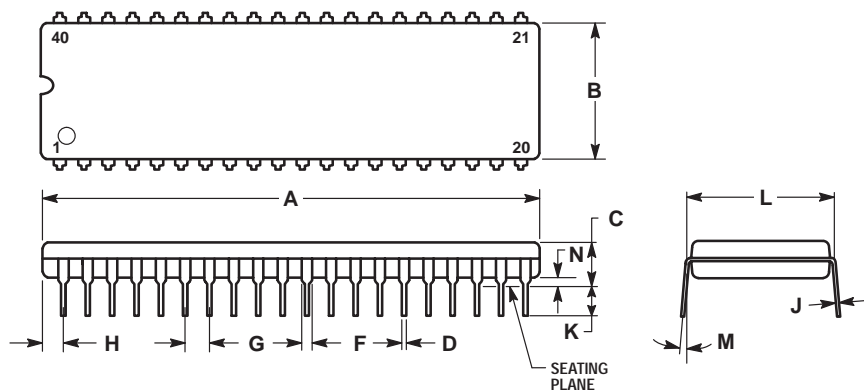
Case 649-03 N Suffix 24-Pin Plastic Wide Body



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. 649-02 OBSOLETE, NEW STD 649-03 SEE ISSUE "C" FOR REFERENCE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	— 10°		— 10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

Case 711-03 N Suffix 40-Pin Plastic



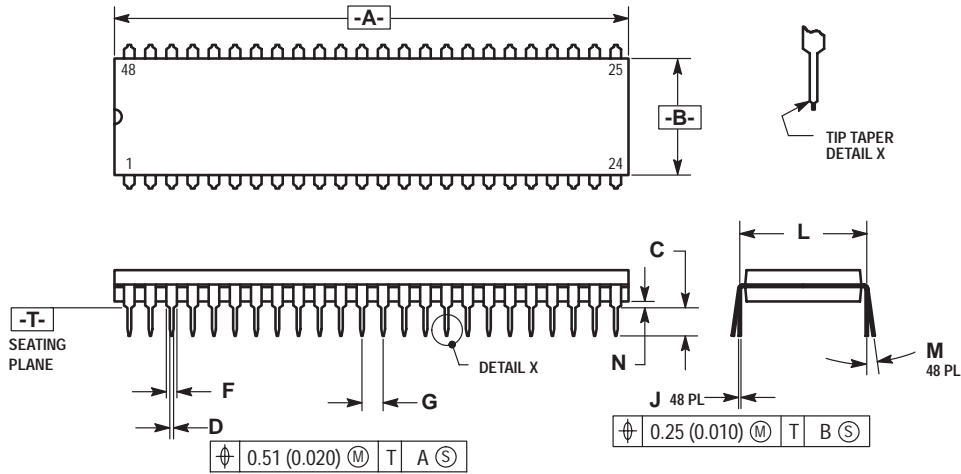
- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0° 15°		0° 15°	
N	0.51	1.02	0.020	0.040

PACKAGE OUTLINES

PLASTIC (continued)

Case 767-02 N Suffix 48-Pin Plastic



NOTES:

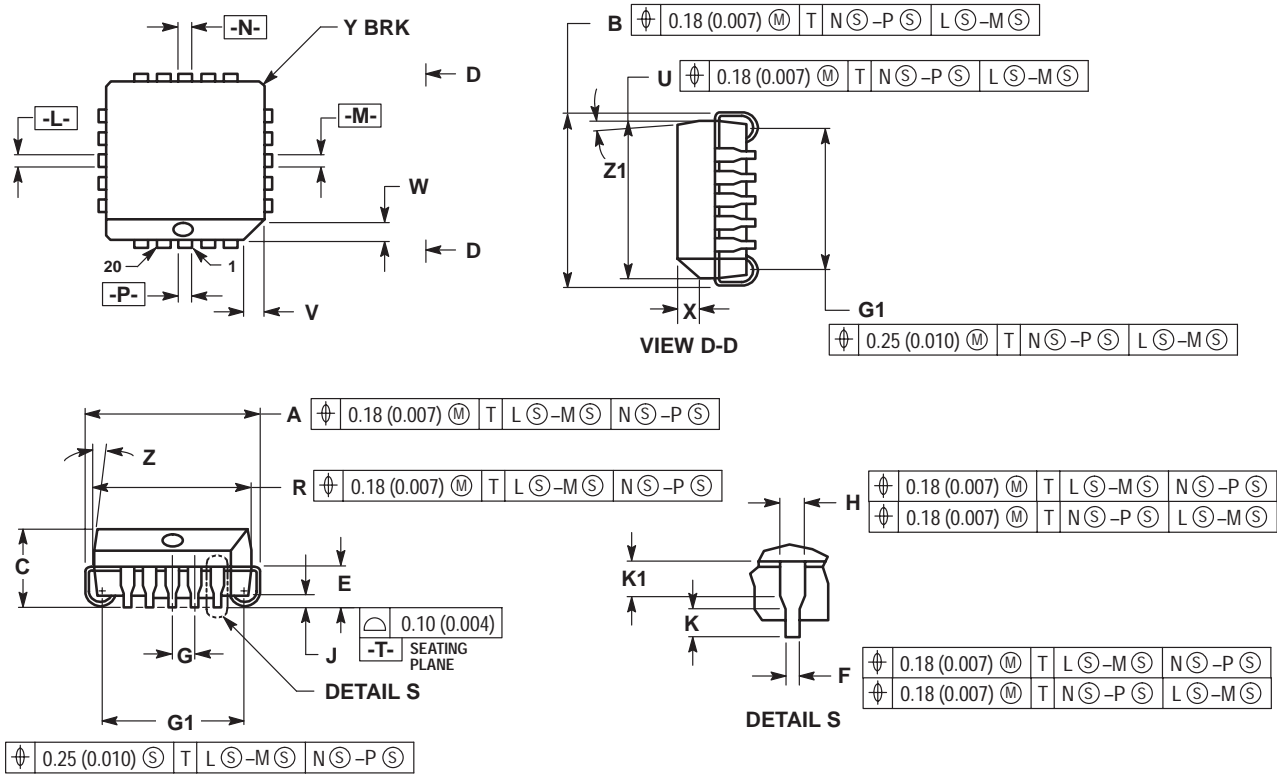
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).
5. 767-01 OBSOLETE. NEW STANDARD 767-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	61.34	62.10	2.415	2.445
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.55	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.79 BSC		0.070 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.81	0.115	0.150
L	15.24 BSC		0.600 BSC	
M	0°	0°	0°	0°
N	0.51	1.01	0.020	0.040

PACKAGE OUTLINES

PLCC

Case 775-02 FN Suffix
20-Pin Plastic



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

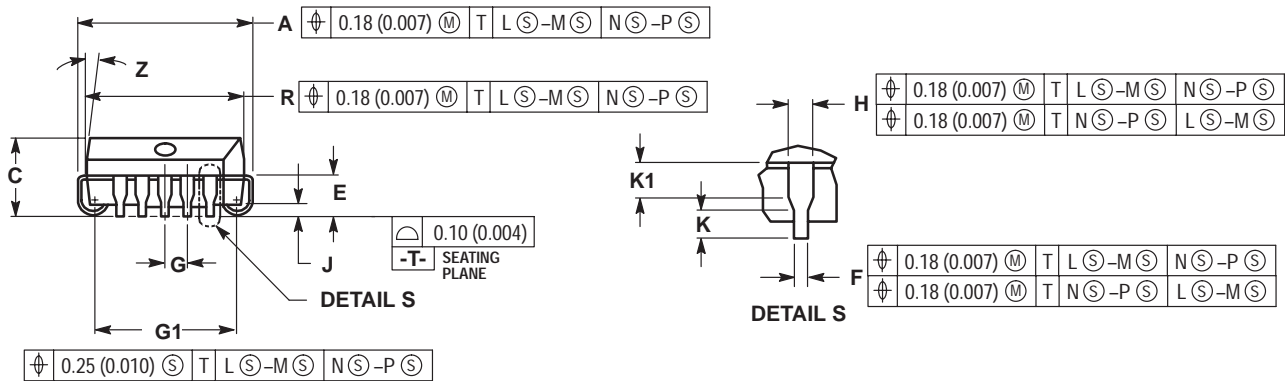
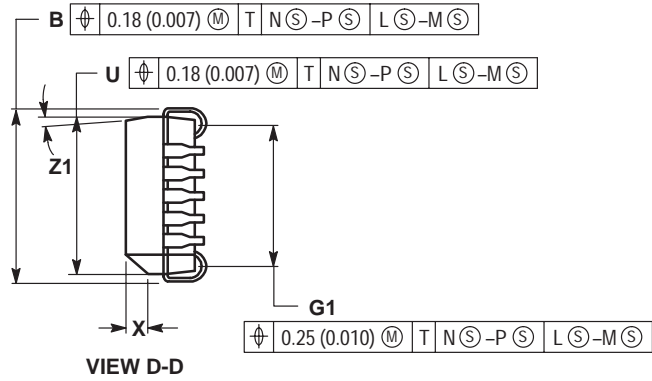
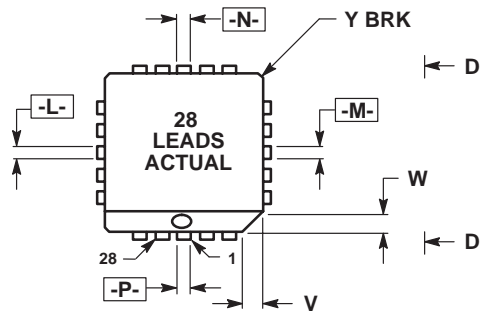
NOTES:

- DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- 775-01 IS OBSOLETE, NEW STANDARD 775-02.

PACKAGE OUTLINES

PLCC (continued)

Case 776-02 FN Suffix 28-Pin Plastic



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

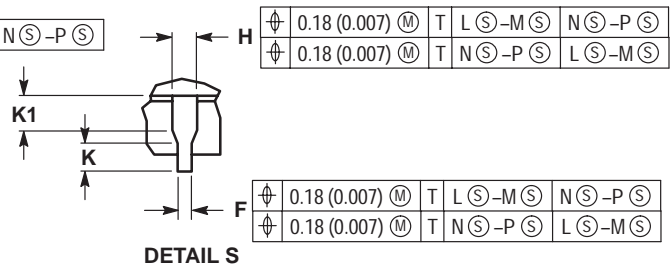
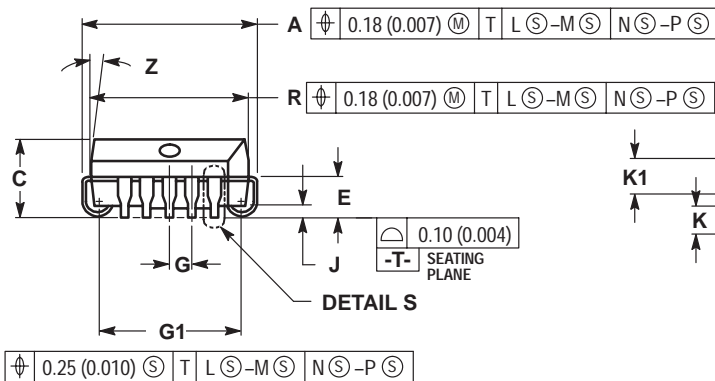
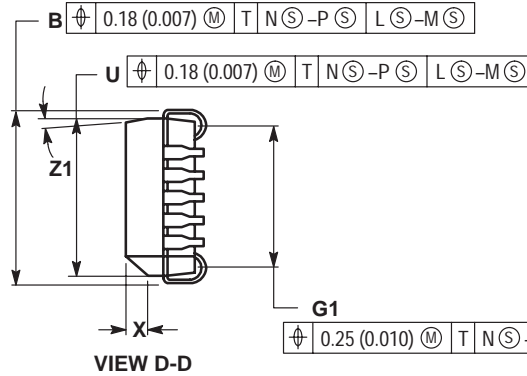
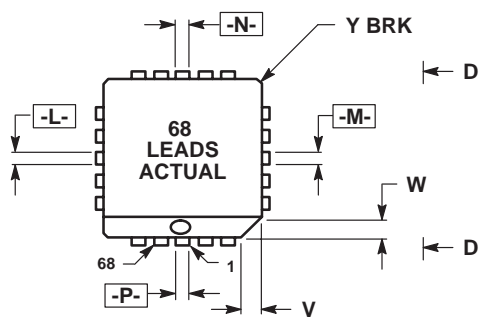
NOTES:

1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 776-01 IS OBSOLETE, NEW STANDARD 776-02.

PACKAGE OUTLINES

PLCC (continued)

Case 779-02 FN Suffix
68-Pin Plastic



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.02	25.27	0.985	0.995
B	25.02	25.27	0.985	0.995
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	24.13	24.28	0.950	0.956
U	24.13	24.28	0.950	0.956
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	23.12	23.62	0.910	0.930
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:

1. DUE TO SPACE LIMITATION, CASE 779-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 68 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. 779-01 IS OBSOLETE, NEW STANDARD 779-02.



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