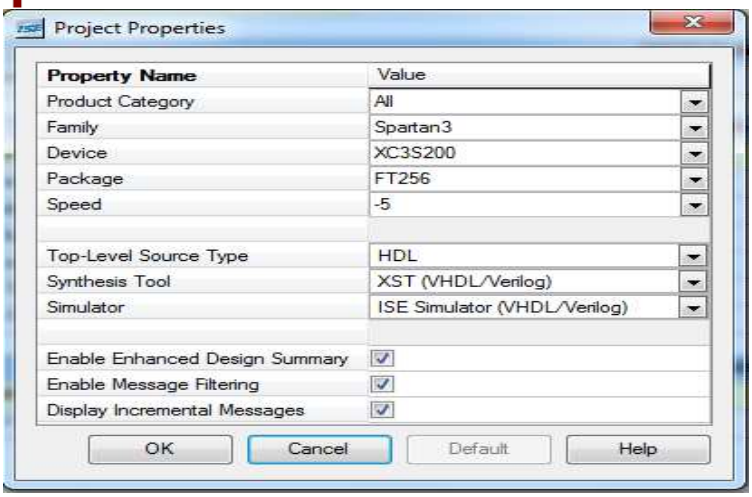
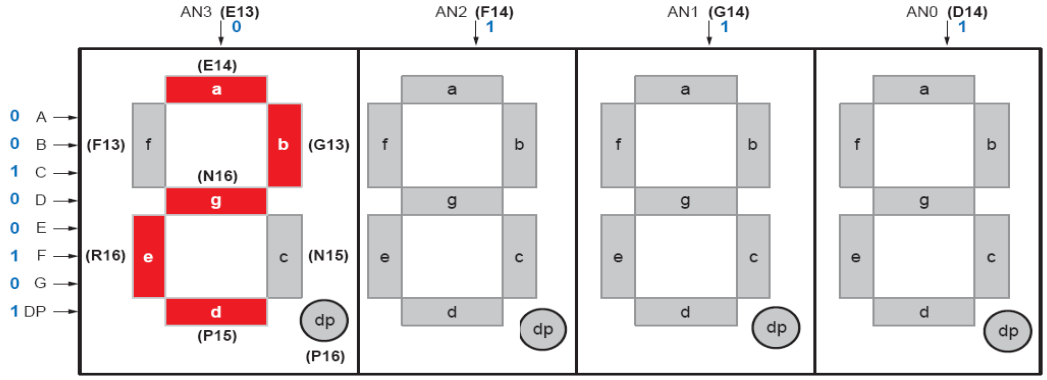
DATOS TARJETAS

Spartan-3 Starter Kit Board





Slider Switch Connections

Switch	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0
FPGA Pin	K13	K14	J13	J14	H13	H14	G12	F12

Push Button Switch Connections

Push Button	BTN3 (User Reset)	BTN2	BTN1	BTN0
FPGA Pin	L14	L13	M14	M13

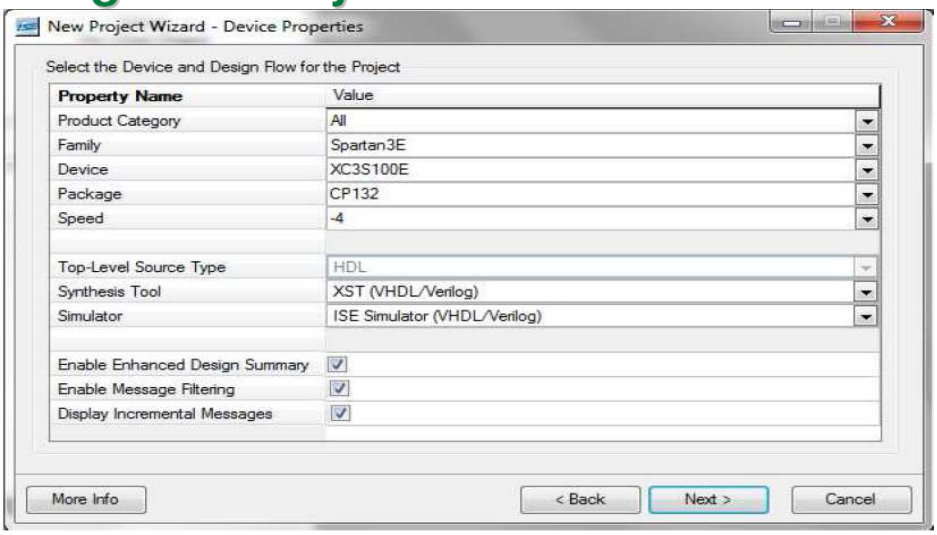
LED Connections to the Spartan-3 FPGA

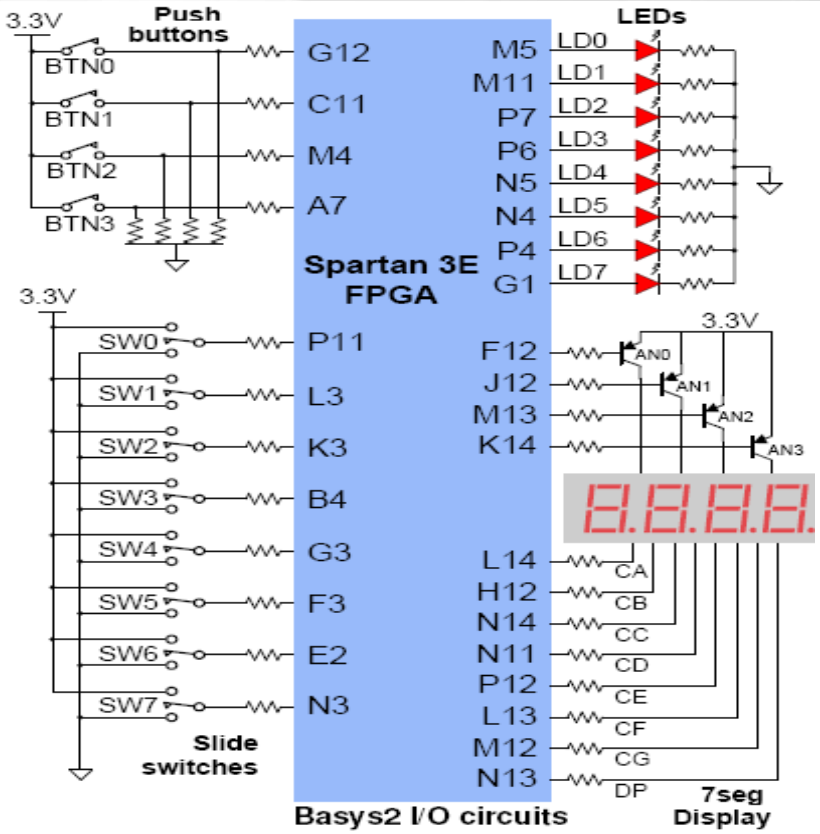
LED	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
FPGA Pin	P11	P12	N12	P13	N14	L12	P14	K12

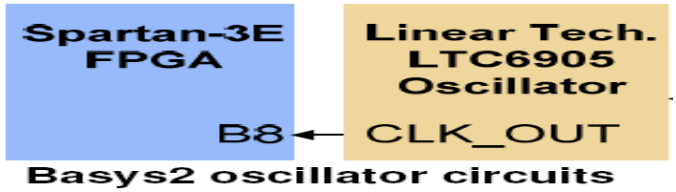
Clock Oscillator Sources

Oscillator Source	FPGA Pin
50 MHz (IC4)	T9

Digilent Basys2 Board

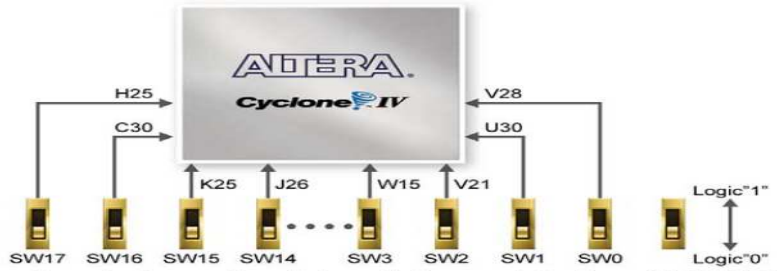






DE2i-150 Board

Device Family: Ciclone IV FPGA GX
Device: EP4CGX150DF31C7

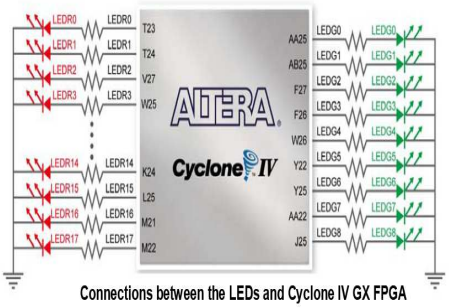


Connections between the slide switches and Cyclone IV GX FPGA

Signal Name	FPGA
SW[0]	V28
SW[1]	U30
SW[2]	V21
SW[3]	C2
SW[4]	AB30
SW[5]	U21
SW[6]	T28
SW[7]	R30
SW[8]	P30
SW[9]	R29
SW[10]	R26
SW[11]	N26
SW[12]	M26
SW[13]	N25
SW[14]	J26
SW[15]	K25
SW[16]	C30
SW[17]	H25

Pin Assignments for Push-buttons

Signal Name	FPGA
KEY[0]	AA26
KEY[1]	AE25
KEY[2]	AF30
KEY[3]	AE26

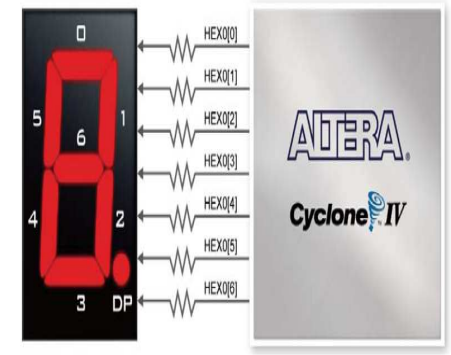


Connections between the LEDs and Cyclone IV GX FPGA

Pin Assignments for LEDs

Signal Name	*FPGA*
LEDR[0]	T23
LEDR[1]	T24
LEDR[2]	V27
LEDR[3]	W25
LEDR[4]	T21
LEDR[5]	T26
LEDR[6]	R25
LEDR[7]	T27
LEDR[8]	P25
LEDR[9]	R24
LEDR[10]	P21
LEDR[11]	N24
LEDR[12]	N21
LEDR[13]	M25
LEDR[14]	K24
LEDR[15]	L25
LEDR[16]	M21
LEDR[17]	M22
LEDG[0]	AA25
LEDG[1]	AB25
LEDG[2]	F27
LEDG[3]	F26
LEDG[4]	W26
LEDG[5]	Y22
LEDG[6]	Y25
LEDG[7]	AA22
LEDG[8]	J25

Signal Name	FPGA
HEX0[0]	E15
HEX0[1]	E12
HEX0[2]	G11
HEX0[3]	F11
HEX0[4]	F16
HEX0[5]	D16
HEX0[6]	F14
HEX1[0]	G14
HEX1[1]	B13
HEX1[2]	G13
HEX1[3]	F12
HEX1[4]	G12
HEX1[5]	J9
HEX1[6]	G10
HEX2[0]	G8
HEX2[1]	G7
HEX2[2]	F7
HEX2[3]	AG30
HEX2[4]	F6
HEX2[5]	F4
HEX2[6]	F10
HEX3[0]	D10
HEX3[1]	D7
HEX3[2]	E6
HEX3[3]	E4
HEX3[4]	E3
HEX3[5]	D5
HEX3[6]	D4
HEX4[0]	A14
HEX4[1]	A13
HEX4[2]	C7
HEX4[3]	C6
HEX4[4]	C5
HEX4[5]	C4
HEX4[6]	C3
HEX5[0]	D3
HEX5[1]	A10
HEX5[2]	A9
HEX5[3]	A7
HEX5[4]	A6
HEX5[5]	A11
HEX5[6]	B6
HEX6[0]	B9
HEX6[1]	B10
HEX6[2]	C8
HEX6[3]	C9
HEX6[4]	D8
HEX6[5]	D9
HEX6[6]	E9
HEX7[0]	E10
HEX7[1]	F8
HEX7[2]	F9
HEX7[3]	C10
HEX7[4]	C11
HEX7[5]	C12
HEX7[6]	D12



Connections between the 7-segment display HEX0 and Cyclone IV GX FPGA

Block diagram of the clock distribution